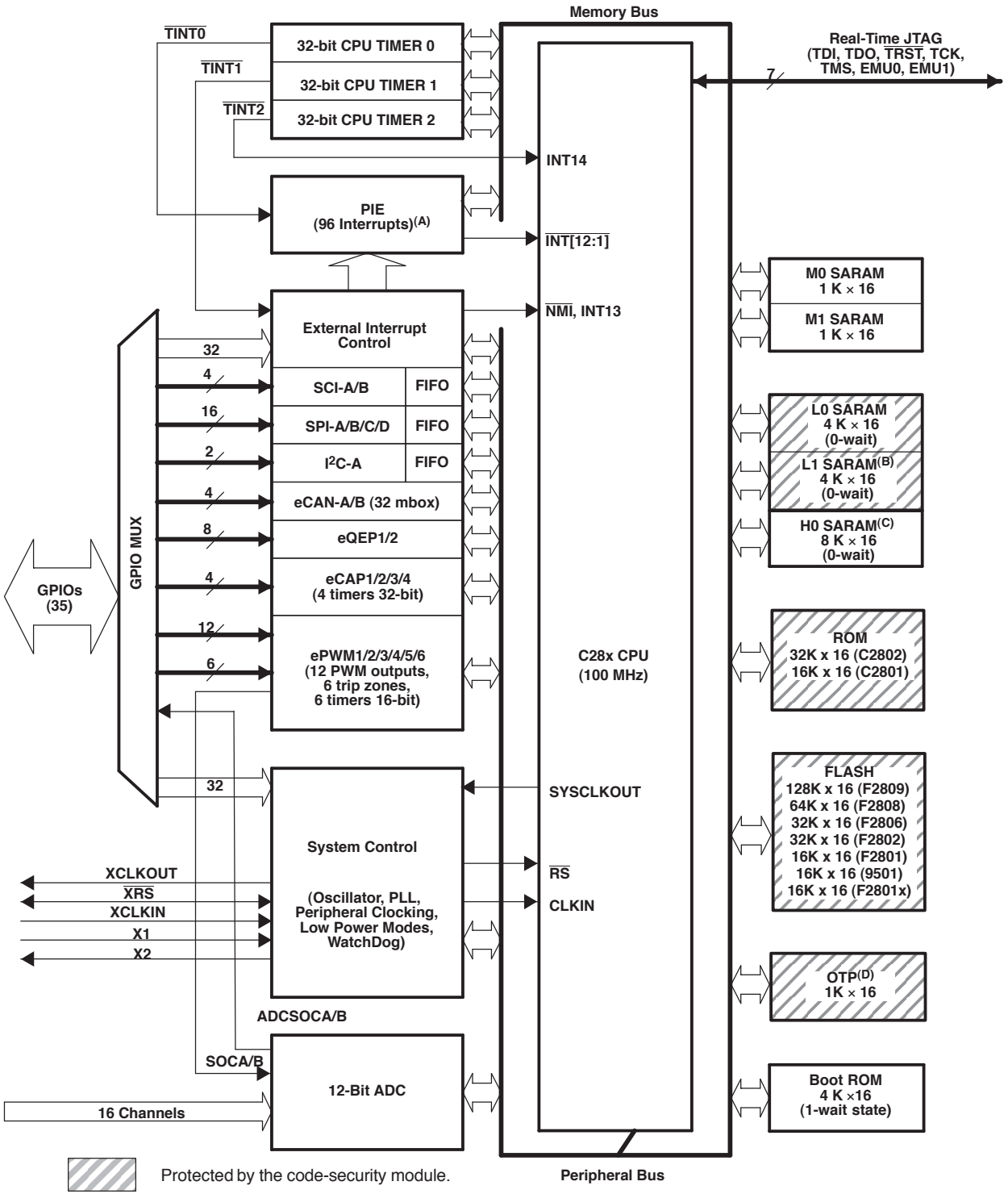
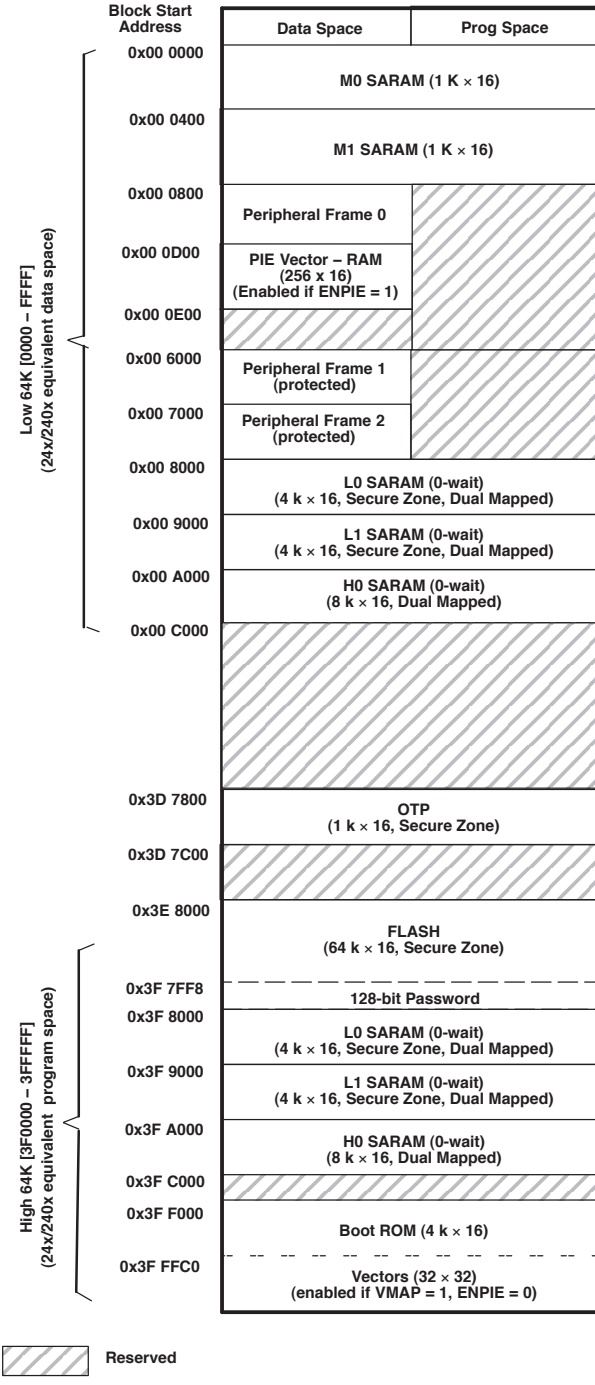
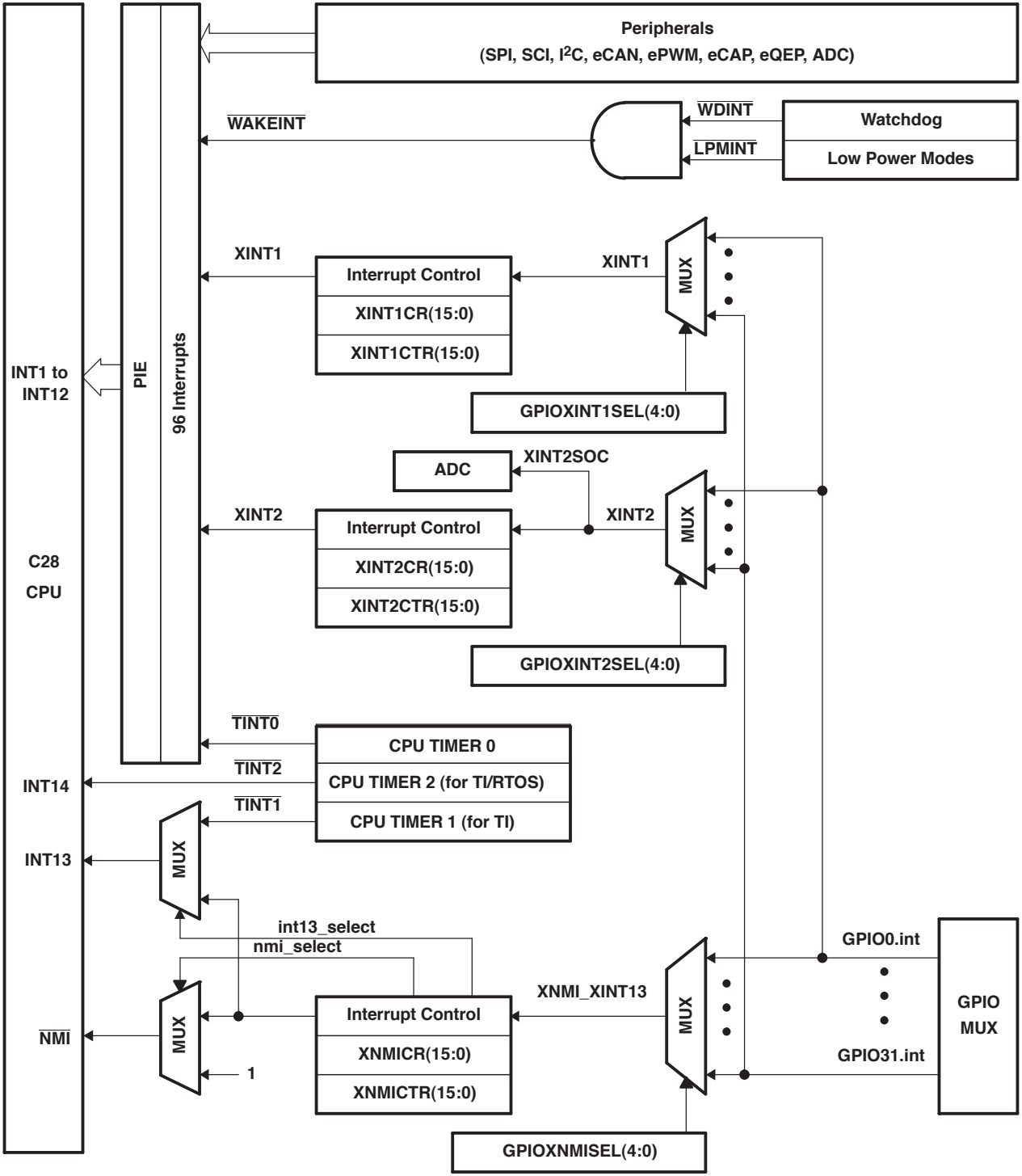
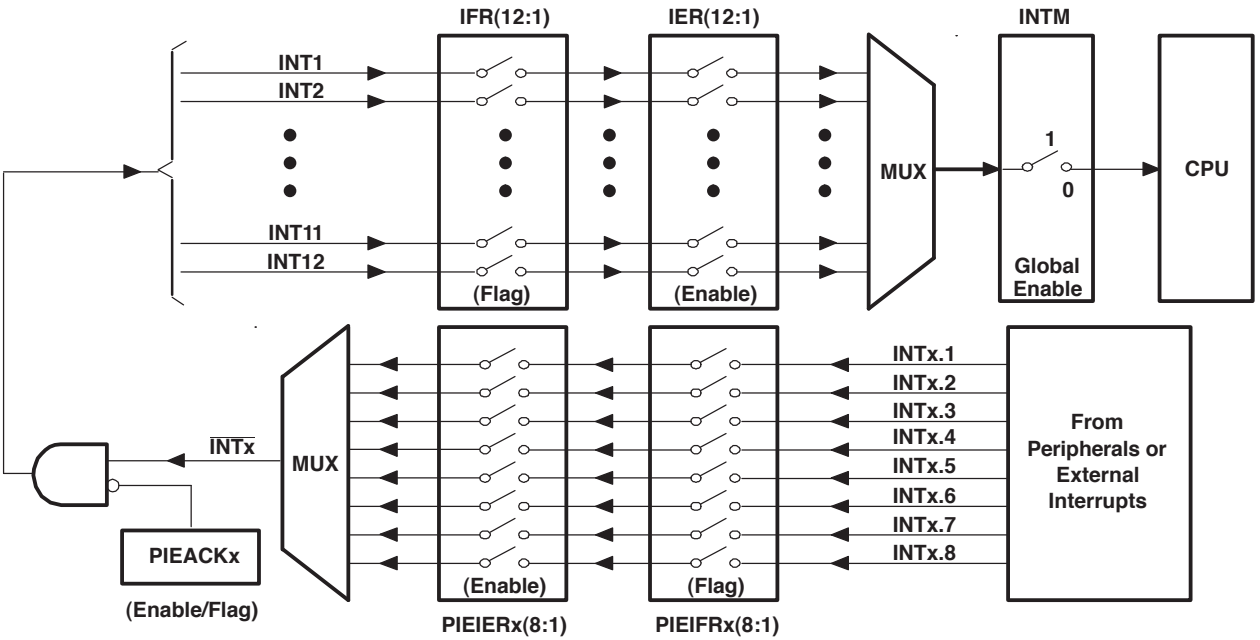
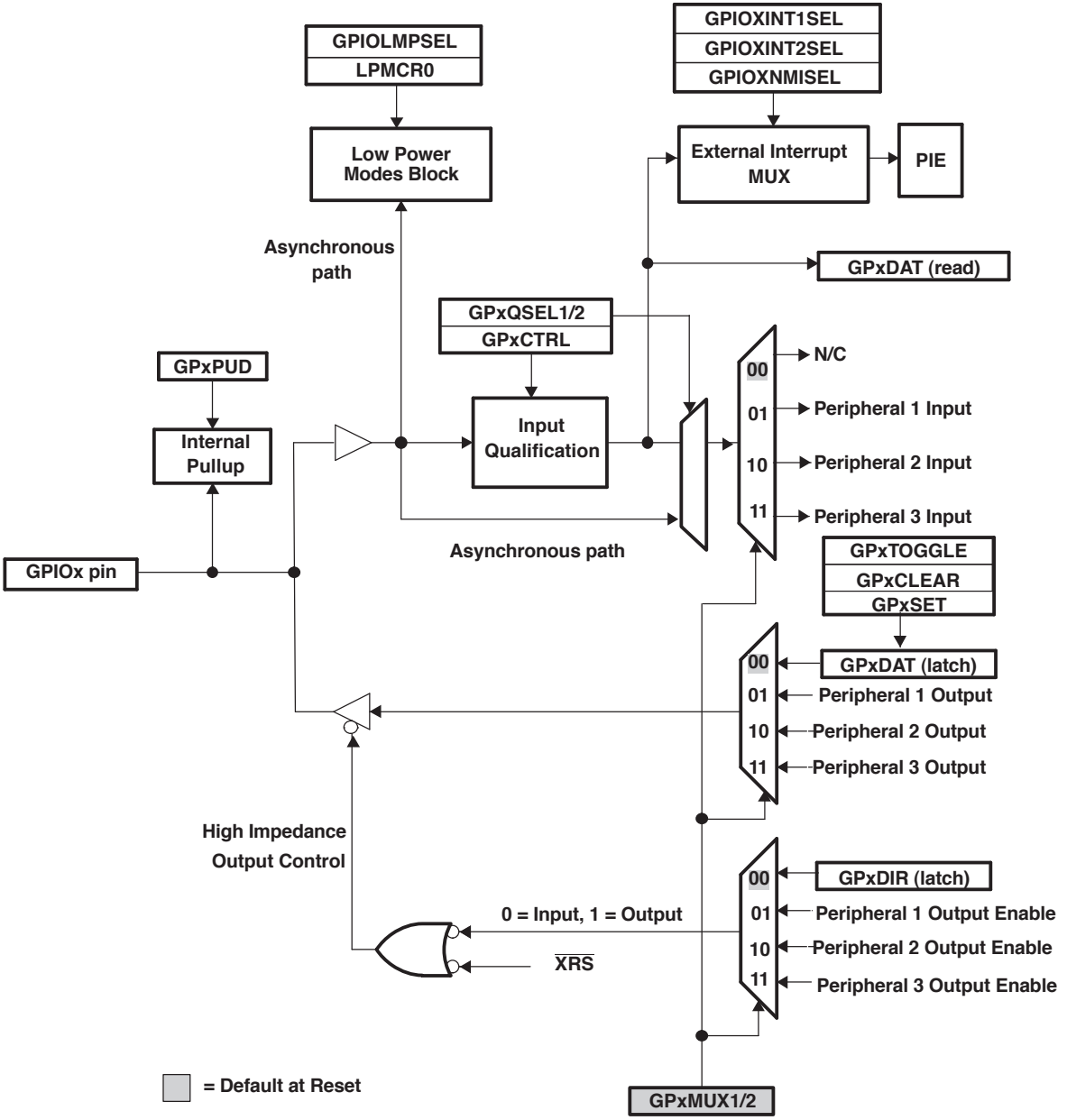
TDO 76
VSS 77
XRS 78
GPIO27/ECAP4/EQEP2S/SPISTEB 79
EMU0 80
EMU1 81
VDDIO 82
GPIO24/ECAP1/EQEP2A/SPISIMOB 83
TRST 84
VDD 85
X2 86
VSS 87
X1 88
VSS 89
XCLKIN 90
GPIO25/ECAP2/EQEP2B/SPISOMIB 91
GPIO28/SCIRXDA/TZ5 92
VDD 93
VSS 94
GPIO13/TZ2/CANRXB/SPISOMIB 95
VDD3VFL 96
TEST1 97
TEST2 98
GPIO26/ECAP3/EQEP2I/SPICLKB 99
GPIO32/SDAA/EPWMSYNCI/ADCSOCAO 100
GPIO12/TZ1/CANTXB/SPISIMOB 1
VSS 2
VDDIO 3
GPIO29/SCITXDA/TZ6 4
GPIO33/SCLA/EPWMSYNCO/ADCSOCBO 5
GPIO30/CANRXA 6
GPIO31/CANTXA 7
GPIO14/TZ3/SCITXDB/SPICLKB 8
GPIO15/TZ4/SCIRXDB/SPISTEB 9
VDD 10
VSS 11
VDD1A18 12
VSS1AGND 13
VSSA2 14
VDDA2 15
ADCINA7 16
ADCINA6 17
ADCINA5 18
ADCINA4 19
ADCINA3 20
ADCINA2 21
ADCINA1 22
ADCINA0 23
ADCLO 24
VSSAIO 25
TCK 75
TMS 74
TDI 73
GPIO23/EQEP1I/SPISTEC/SCIRXDB 72
GPIO22/EQEP1S/SPICLKC/SCITXDB 71
GPIO11/EPWM6B/SCIRXDB/ECAP4 70
VSS 69
VDD 68
GPIO21/EQEP1B/SPISOMIC/CANRXB 67
XCLKOUT 66
VDDIO 65
GPIO10/EPWM6A/CANRXB/ADCSOCBO 64
GPIO20/EQEP1A/SPISIMOC/CANTXB 63
VSS 62
GPIO9/EPWM5B/SCITXDB/ECAP3 61
GPIO8/EPWM5A/CANTXB/ADCSOCAO 60
VDD 59
GPIO7/EPWM4B/SPISTED/ECAP2 58
GPIO19/SPISTEA/SCIRXDB 57
GPIO6/EPWM4A/EPWMSYNCI/EPWMSYNCO 56
VSS 55
GPIO18/SPICLKA/SCITXDB 54
GPIO5/EPWM3B/SPICLKD/ECAP1 53
GPIO17/SPISOMIA/CANRXB/TZ6 52
GPIO4/EPWM3A 51
GPIO16/SPISIMOA/CANTXB/TZ5 50
VSS 49
GPIO3/EPWM2B/SPISOMID 48
GPIO0/EPWM1A 47
VDDIO 46
GPIO2/EPWM2A 45
GPIO1/EPWM1B/SPISIMOD 44
GPIO34 43
VDD 42
VSS 41
VDD2A18 40
VSS2AGND 39
ADCRESEXT 38
ADCREFP 37
ADCREFM 36
ADCREFIN 35
ADCINB7 34
ADCINB6 33
ADCINB5 32
ADCINB4 31
ADCINB3 30
ADCINB2 29
ADCINB1 28
ADCINB0 27
VDDAIO 26

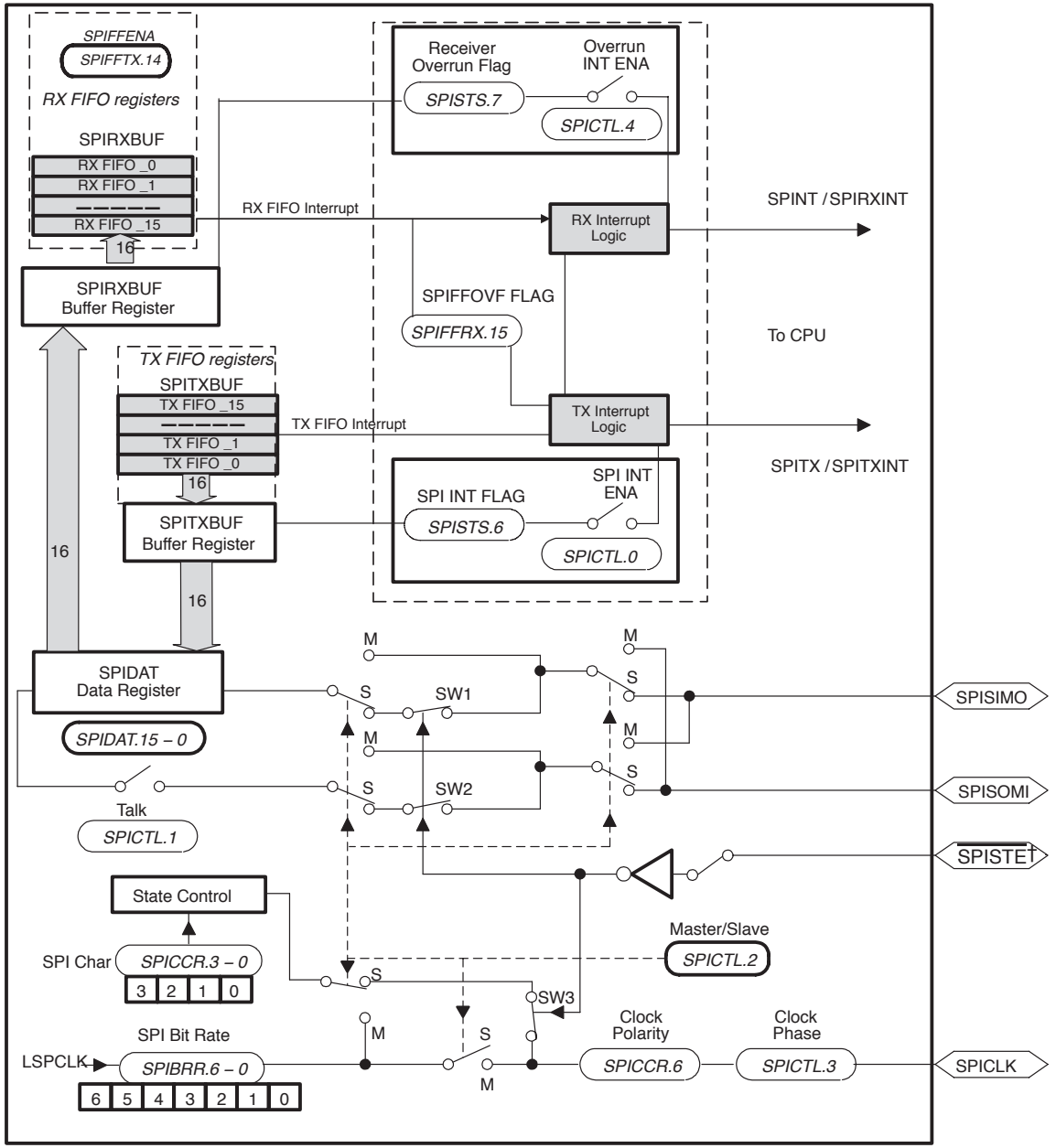

Memory Bus
TINT0
TINT1
TINT2
32-bit CPU TIMER 0
32-bit CPU TIMER 1
32-bit CPU TIMER 2
INT14
PIE
(96 Interrupts)(A)
INT[12:1]
NMI, INT13
External Interrupt
Control
32
4
SCI-A/B
FIFO
16
SPI-A/B/C/D
FIFO
2
I2C-A
FIFO
4
eCAN-A/B (32 mbox)
8
eQEP1/2
4
eCAP1/2/3/4
(4 timers 32-bit)
12
6
ePWM1/2/3/4/5/6
(12 PWM outputs,
6 trip zones,
6 timers 16-bit)
GPIO MUX
GPIOs
(35)
C28x CPU
(100 MHz)
Real-Time JTAG
(TDI, TDO, TRST, TCK,
TMS, EMU0, EMU1)
7
M0 SARAM
1 K × 16
M1 SARAM
1 K × 16
L0 SARAM
4 K × 16
(0-wait)
L1 SARAM(B)
4 K × 16
(0-wait)
H0 SARAM(C)
8 K × 16
(0-wait)
ROM
32K x 16 (C2802)
16K x 16 (C2801)
FLASH
128K x 16 (F2809)
64K x 16 (F2808)
32K x 16 (F2806)
32K x 16 (F2802)
16K x 16 (F2801)
16K x 16 (9501)
16K x 16 (F2801x)
OTP(D)
1K × 16
Boot ROM
4 K ×16
(1-wait state)
32
System Control
(Oscillator, PLL,
Peripheral Clocking,
Low Power Modes,
WatchDog)
SYSCLKOUT
RS
CLKIN
XCLKOUT
XRS
XCLKIN
X1
X2
ADCSOCA/B
SOCA/B
12-Bit ADC
16 Channels
Protected by the code-security module.
Peripheral Bus


Block Start Address
Data Space
Prog Space
0x00 0000
M0 SARAM (1 K × 16)
0x00 0400
M1 SARAM (1 K × 16)
0x00 0800
Peripheral Frame 0
0x00 0D00
PIE Vector – RAM (256 x 16) (Enabled if ENPIE = 1)
0x00 0E00
0x00 6000
Peripheral Frame 1 (protected)
0x00 7000
Peripheral Frame 2 (protected)
0x00 8000
L0 SARAM (0-wait) (4 k × 16, Secure Zone, Dual Mapped)
0x00 9000
L1 SARAM (0-wait) (4 k × 16, Secure Zone, Dual Mapped)
0x00 A000
H0 SARAM (0-wait) (8 k × 16, Dual Mapped)
0x00 C000
0x3D 7800
OTP (1 k × 16, Secure Zone)
0x3D 7C00
0x3E 8000
FLASH (64 k × 16, Secure Zone)
0x3F 7FF8
128-bit Password
0x3F 8000
L0 SARAM (0-wait) (4 k × 16, Secure Zone, Dual Mapped)
0x3F 9000
L1 SARAM (0-wait) (4 k × 16, Secure Zone, Dual Mapped)
0x3F A000
H0 SARAM (0-wait) (8 k × 16, Dual Mapped)
0x3F C000
0x3F F000
Boot ROM (4 k × 16)
0x3F FFC0
Vectors (32 × 32) (enabled if VMAP = 1, ENPIE = 0)
Low 64K [0000 – FFFF] (24x/240x equivalent data space)
High 64K [3F0000 – 3FFFFF] (24x/240x equivalent program space)
Reserved

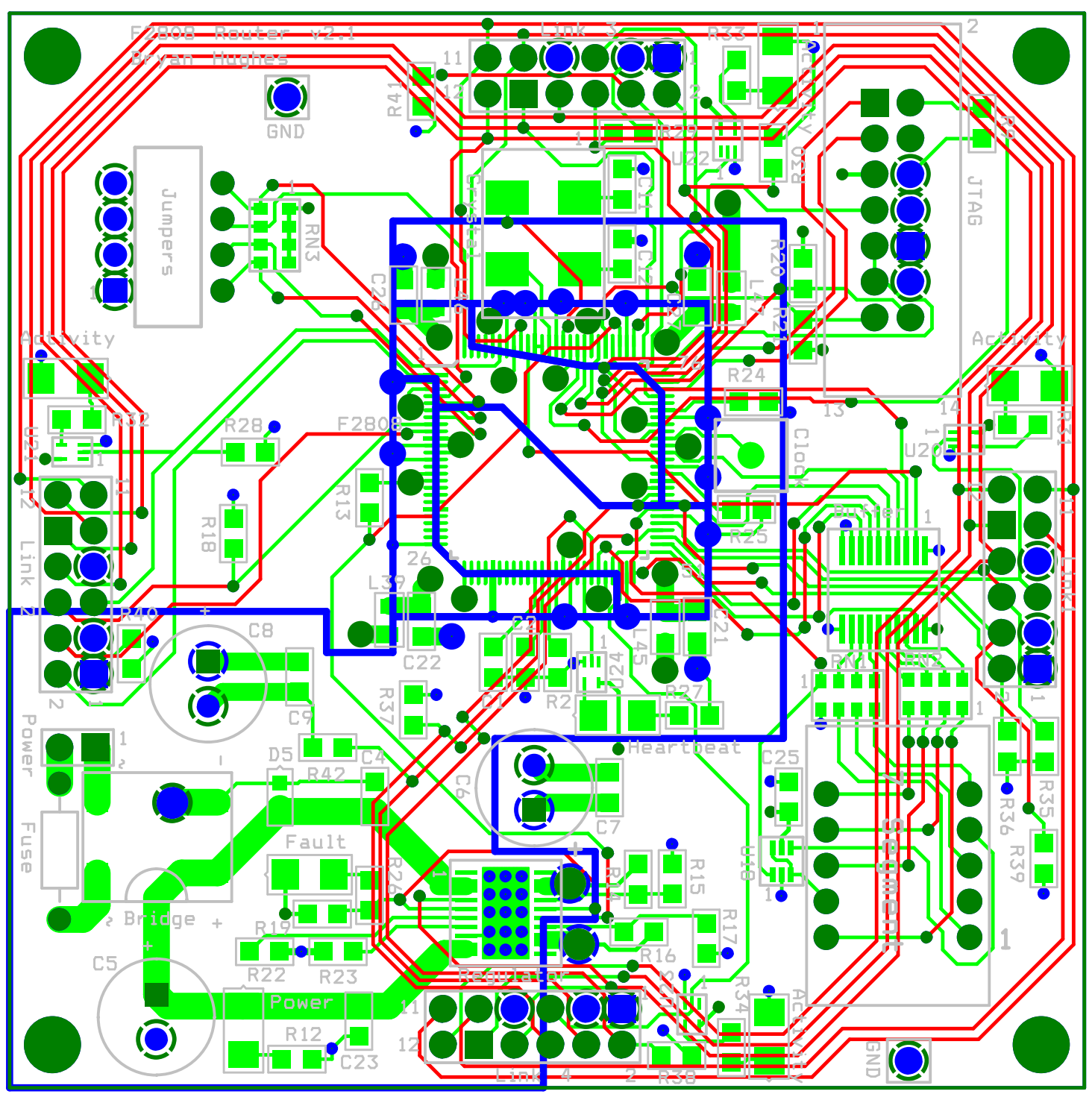

Peripherals
(SPI, SCI, I2C, eCAN, ePWM, eCAP, eQEP, ADC)
WAKEINT
WDINT
LPMINT
Watchdog
Low Power Modes
XINT1
Interrupt Control
XINT1CR(15:0)
XINT1CTR(15:0)
XINT1
MUX
GPIOXINT1SEL(4:0)
INT1 to
INT12
PIE
96 Interrupts
ADC
XINT2SOC
XINT2
Interrupt Control
XINT2CR(15:0)
XINT2CTR(15:0)
XINT2
MUX
GPIOXINT2SEL(4:0)
C28
CPU
TINT0
CPU TIMER 0
TINT2
CPU TIMER 2 (for TI/RTOS)
TINT1
CPU TIMER 1 (for TI)
INT14
INT13
MUX
int13_select
nmi_select
GPIO0.int
GPIO31.int
GPIO
MUX
XNMI_XINT13
MUX
NMI
MUX
1
Interrupt Control
XNMICR(15:0)
XNMICTR(15:0)
GPIOXNMISEL(4:0)

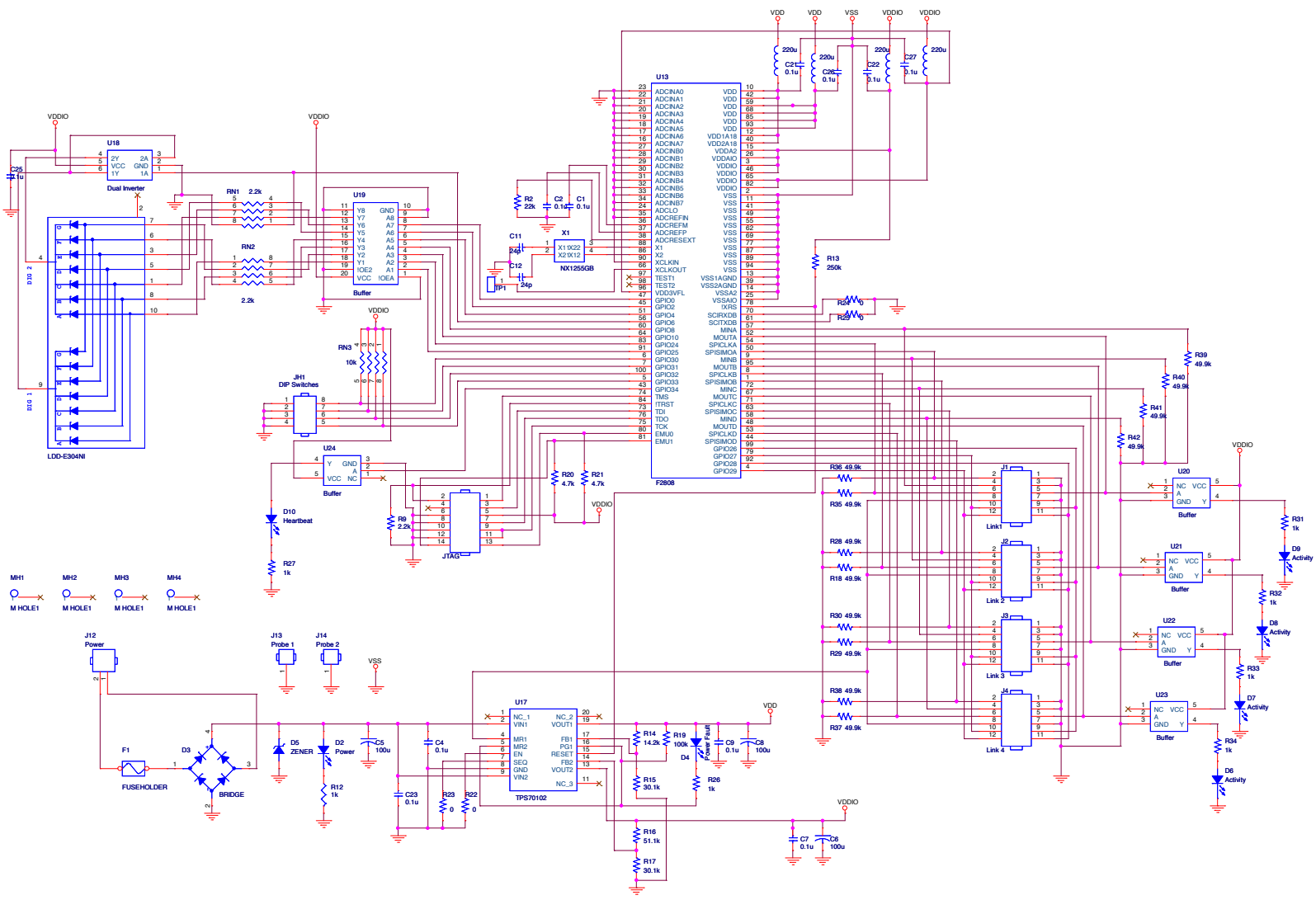

IFR(12:1)
IER(12:1)
INTM
INT1
INT2
INT11
INT12
(Flag)
(Enable)
MUX
1
0
Global Enable
CPU
INTx.1
INTx.2
INTx.3
INTx.4
INTx.5
INTx.6
INTx.7
INTx.8
From Peripherals or External Interrupts
INTx
MUX
PIEACKx
(Enable/Flag)
(Enable)
(Flag)
PIEIERx(8:1)
PIEIFRx(8:1)

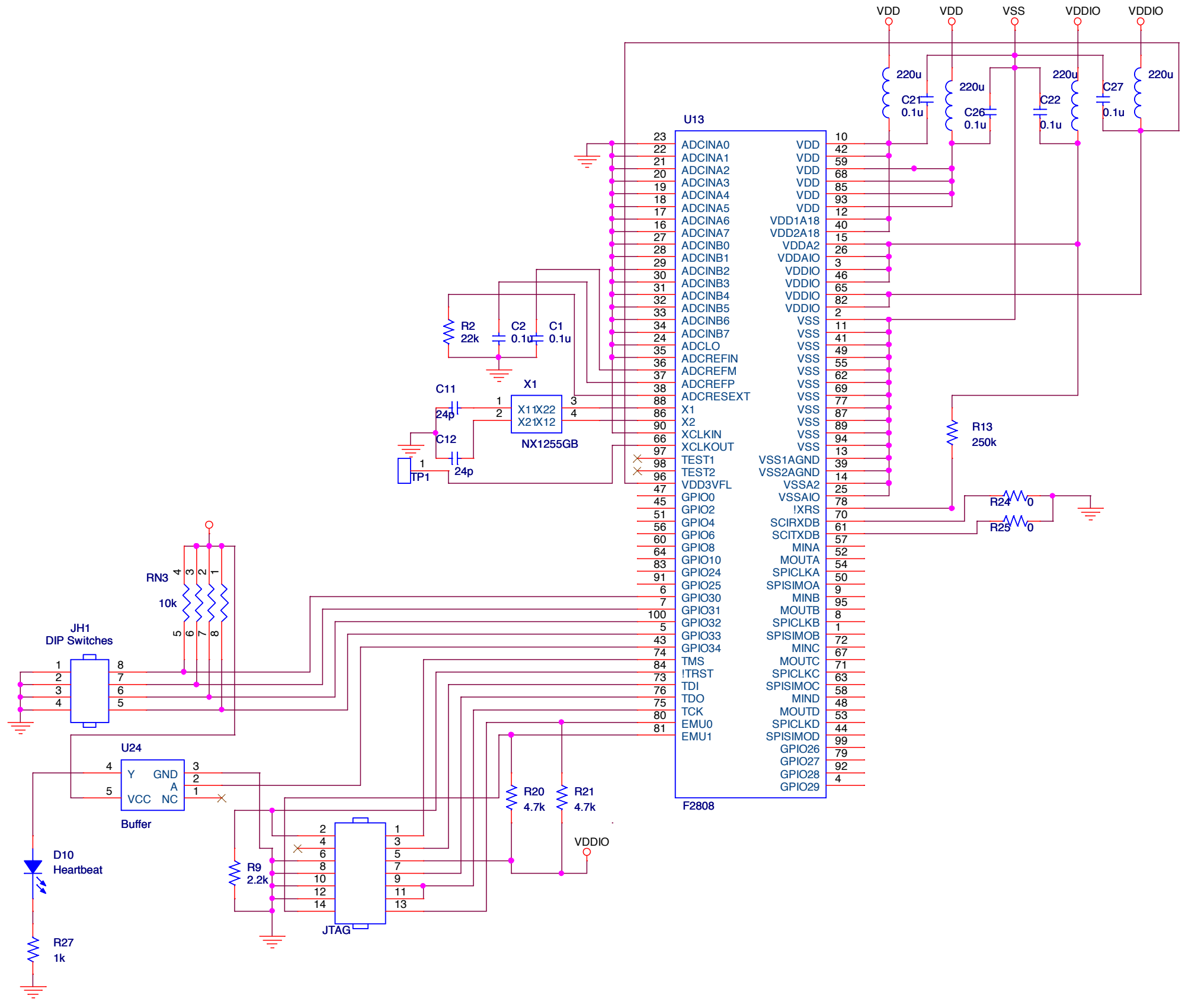

GPIOLMPSEL
LPMCR0
Low Power Modes Block
GPIOXINT1SEL
GPIOXINT2SEL
GPIOXNMISEL
External Interrupt MUX
PIE
Asynchronous path
GPxDAT (read)
GPxQSEL1/2
GPxCTRL
GPxPUD
Internal Pullup
Input Qualification
00
01
10
11
N/C
Peripheral 1 Input
Peripheral 2 Input
Peripheral 3 Input
GPIOx pin
Asynchronous path
GPxTOGGLE
GPxCLEAR
GPxSET
GPxDAT (latch)
Peripheral 1 Output
Peripheral 2 Output
Peripheral 3 Output
High Impedance Output Control
GPxDIR (latch)
0 = Input, 1 = Output
Peripheral 1 Output Enable
Peripheral 2 Output Enable
Peripheral 3 Output Enable
XRS
= Default at Reset
GPxMUX1/2

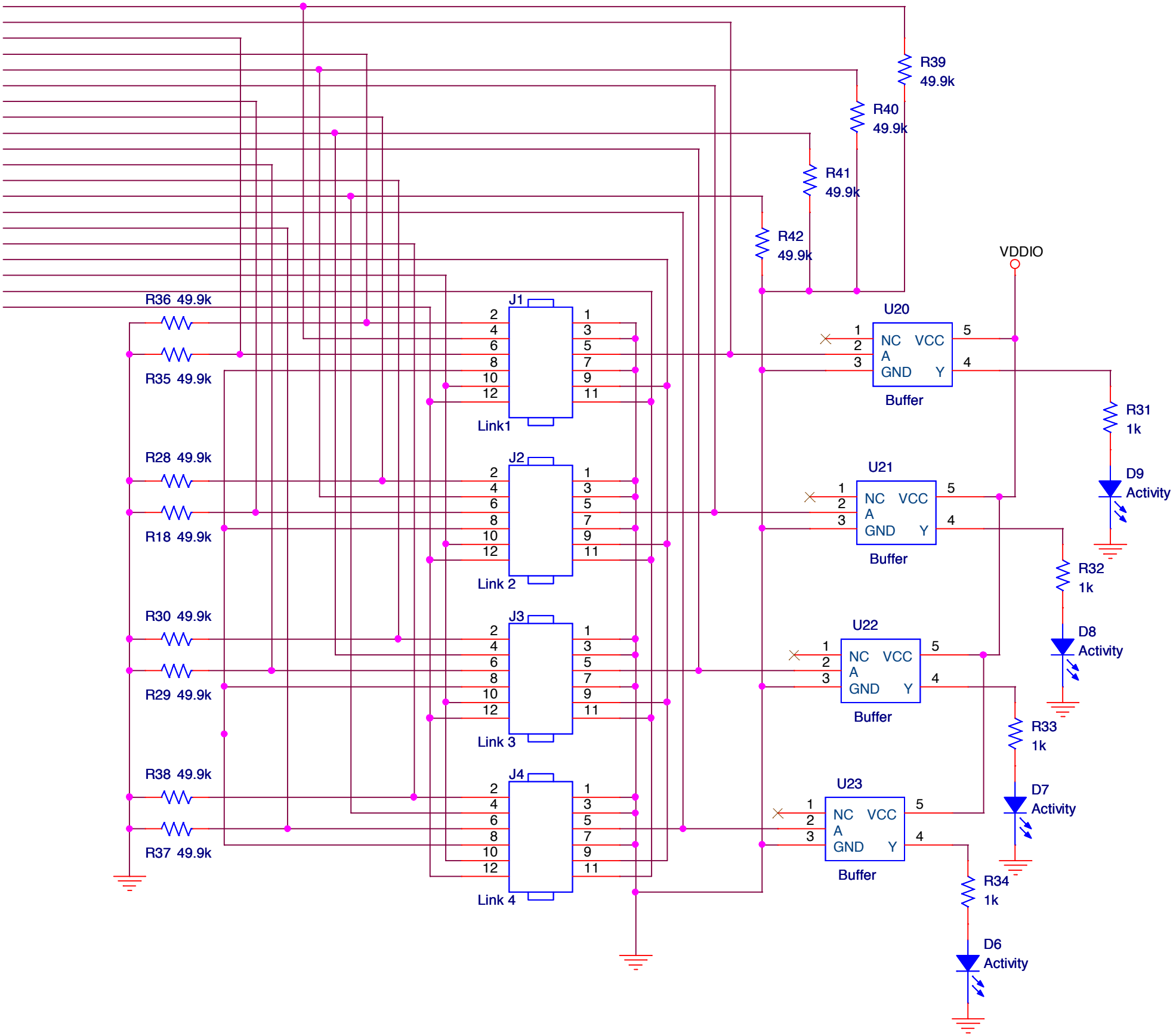


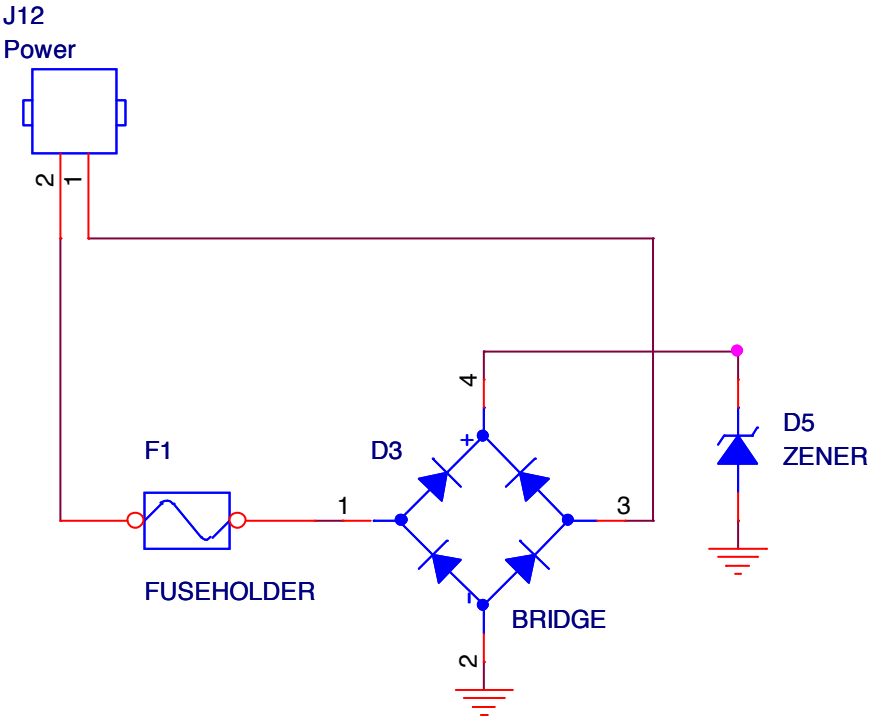
† $\overline{\text{SPISTE}}$ of a slave device is driven low by the master.

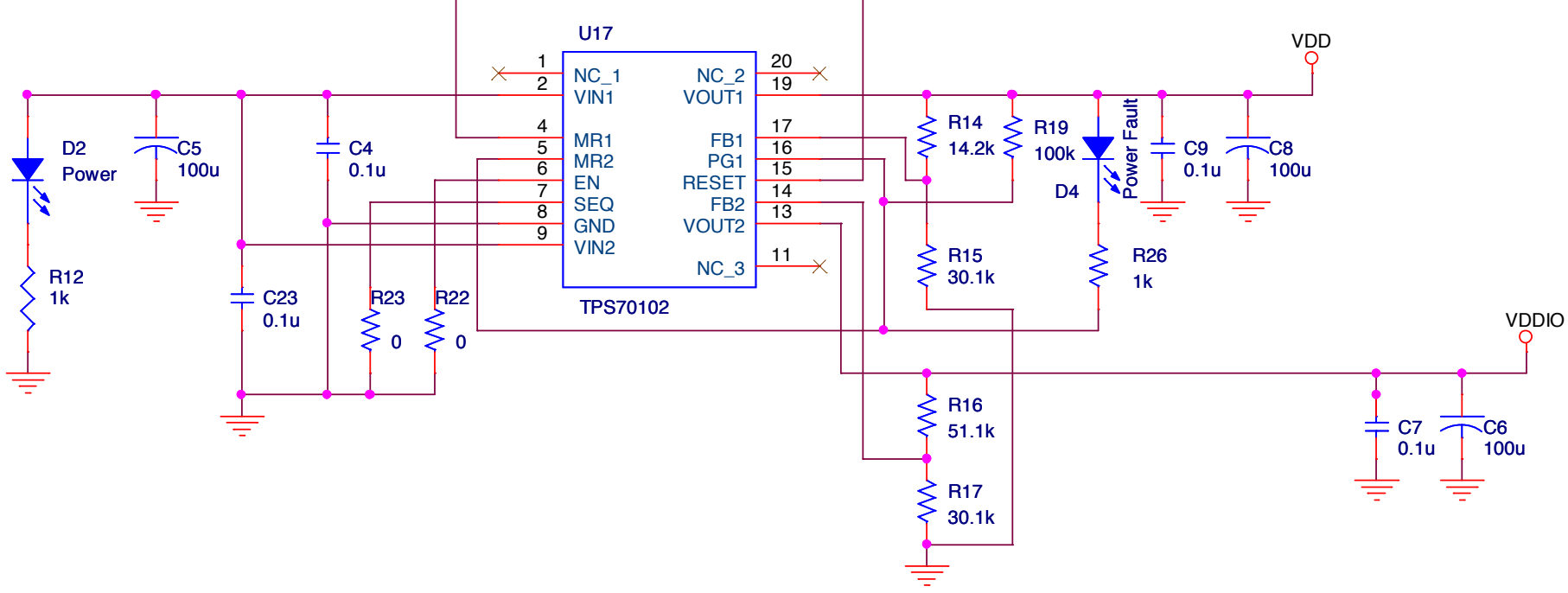

F2808 Router v2.1
Bryan Hughes
GND
Jumpers
RN3
Activity
R32
R28
F2808
R13
R18
Link
R40
C8
C9
Power
Fuse
D5
R42
C4
Fault
Bridge
R19
R22
R23
C5
Power
R12
C23
Link 3
R41
R33
R29
U22
R30
JTAG
Crystal
C26
R20
R21
R24
Clock
U20
Buffer
R25
L39
C22
R37
R2
R27
Heartbeat
C6
C7
R15
R17
R16
Regulator
R34
Link 4
R38
C25
U18
Segment
R36
R35
R39
Activity
GND

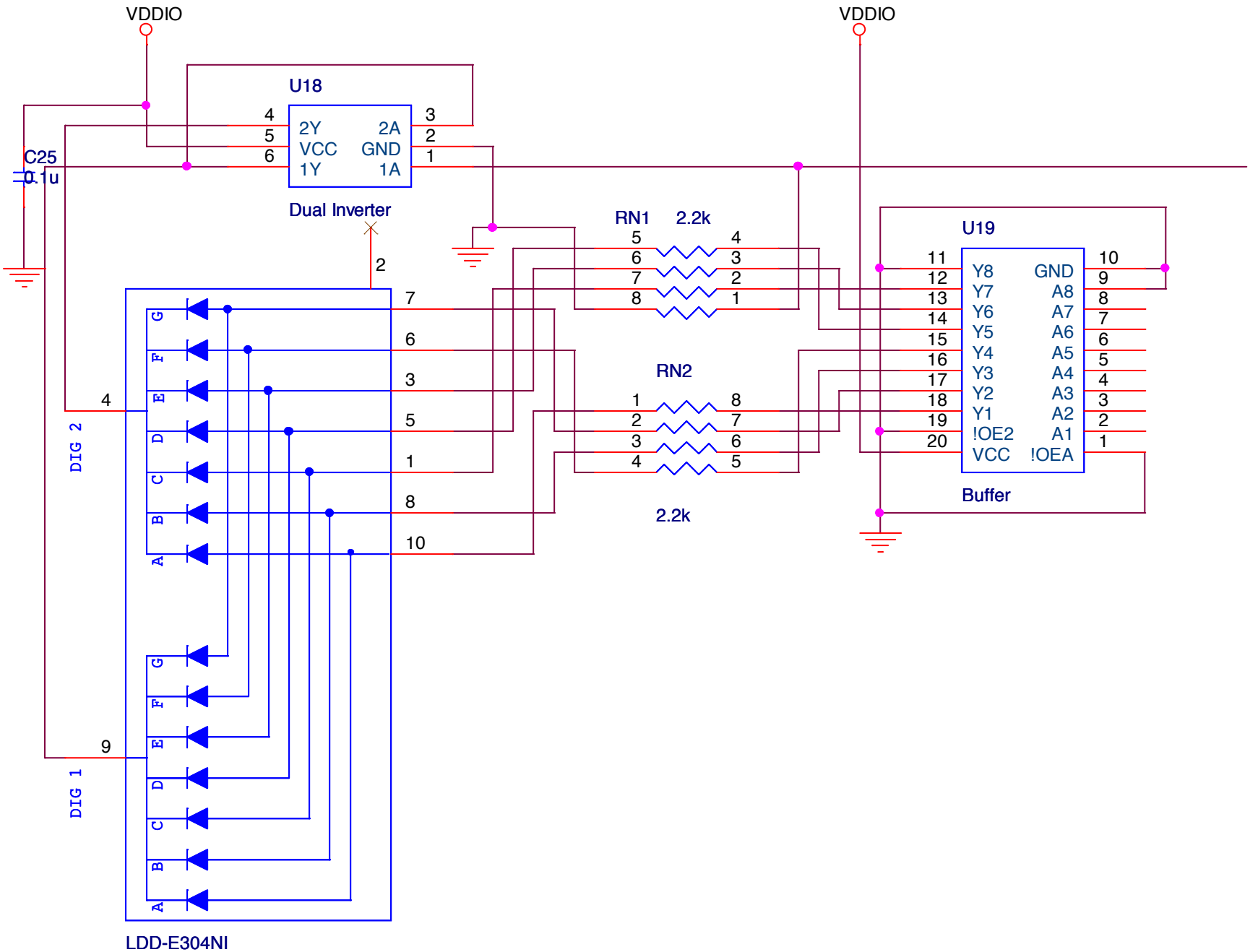

VDD
VDD
VSS
VDDIO
VDDIO
U13
F2808
U18
Dual Inverter
U19
Buffer
U24
Buffer
LDD-E304NI
JH1
DIP Switches
JTAG
U17
TPS70102
U20
U21
U22
U23
Buffer
Link1
Link2
Link3
Link4
J12
Power
J13
Probe 1
J14
Probe 2
F1
FUSEHOLDER
D3
BRIDGE
D5
ZENER
D2
Power
D4
Power Fault
D10
Heartbeat
D6
Activity
D7
Activity
D8
Activity
D9
Activity
X1
NX1255GB
TP1
MH1
MH2
MH3
MH4
M HOLE1


VDD
VDD
VSS
VDDIO
VDDIO
220u
C21
0.1u
220u
C26
0.1u
220u
C22
0.1u
C27
0.1u
220u
U13
ADCINA0
ADCINA1
ADCINA2
ADCINA3
ADCINA4
ADCINA5
ADCINA6
ADCINA7
ADCINB0
ADCINB1
ADCINB2
ADCINB3
ADCINB4
ADCINB5
ADCINB6
ADCINB7
ADCLO
ADCREFIN
ADCREFM
ADCREFP
ADCRESEXT
X1
X2
XCLKIN
XCLKOUT
TEST1
TEST2
VDD3VFL
GPIO0
GPIO2
GPIO4
GPIO6
GPIO8
GPIO10
GPIO24
GPIO25
GPIO30
GPIO31
GPIO32
GPIO33
GPIO34
TMS
!TRST
TDI
TDO
TCK
EMU0
EMU1
VDD
VDD
VDD
VDD
VDD
VDD
VDD1A18
VDD2A18
VDDA2
VDDAIO
VDDIO
VDDIO
VDDIO
VDDIO
VSS
VSS
VSS
VSS
VSS
VSS
VSS
VSS
VSS
VSS
VSS
VSS1AGND
VSS2AGND
VSSA2
VSSAIO
!XRS
SCIRXDB
SCITXDB
MINA
MOUTA
SPICLKA
SPISIMOA
MINB
MOUTB
SPICLKB
SPISIMOB
MINC
MOUTC
SPICLKC
SPISIMOC
MIND
MOUTD
SPICLKD
SPISIMOD
GPIO26
GPIO27
GPIO28
GPIO29
F2808
R2
22k
C2
0.1u
C1
0.1u
C11
24p
X1
X11X22
X21X12
NX1255GB
C12
24p
TP1
R13
250k
R24
0
R25
0
RN3
10k
JH1
DIP Switches
U24
Y
GND
A
VCC
NC
Buffer
D10
Heartbeat
R27
1k
R9
2.2k
JTAG
R20
4.7k
R21
4.7k
VDDIO


R39
49.9k
R40
49.9k
R41
49.9k
R42
49.9k
VDDIO
R36 49.9k
R35 49.9k
R28 49.9k
R18 49.9k
R30 49.9k
R29 49.9k
R38 49.9k
R37 49.9k
J1
Link1
J2
Link 2
J3
Link 3
J4
Link 4
U20
NC VCC
A
GND Y
Buffer
U21
NC VCC
A
GND Y
Buffer
U22
NC VCC
A
GND Y
Buffer
U23
NC VCC
A
GND Y
Buffer
R31
1k
D9
Activity
R32
1k
D8
Activity
R33
1k
D7
Activity
R34
1k
D6
Activity


J12
Power
2
1
F1
FUSEHOLDER
1
D3
4
+
-
3
2
BRIDGE
D5
ZENER


U17
1
2
4
5
6
7
8
9
20
19
17
16
15
14
13
11
NC_1
VIN1
MR1
MR2
EN
SEQ
GND
VIN2
NC_2
VOUT1
FB1
PG1
RESET
FB2
VOUT2
NC_3
TPS70102
VDD
VDDIO
D2
Power
C5
100u
C4
0.1u
C23
0.1u
R12
1k
R23
0
R22
0
R14
14.2k
R19
100k
D4
Power Fault
C9
0.1u
C8
100u
R15
30.1k
R26
1k
R16
51.1k
R17
30.1k
C7
0.1u
C6
100u


VDDIO
VDDIO
U18
2Y
VCC
1Y
2A
GND
1A
Dual Inverter
C25
0.1u
RN1
2.2k
RN2
2.2k
U19
Y8
Y7
Y6
Y5
Y4
Y3
Y2
Y1
!OE2
VCC
GND
A8
A7
A6
A5
A4
A3
A2
A1
!OEA
Buffer
DIG 2
DIG 1
LDD-E304NI