Bihar Engineering University, Patna
End Semester Examination -2023

Course: B.Tech	*Semester: IV*	*Time: 03 Hours*
Code: 100403	*Subject: Digital Electronics*	*Full Marks:70*

Instructions:-

(i) The marks are indicated in the right-hand margin.
*(ii) There are **NINE** questions in this paper.*
*(iii) Attempt **FIVE** questions in all.*
*(iv) Question No. **1** is compulsory.*

Q.1 ***Answer any seven Question only:*** **[2 x 7 = 14]**

(a) Convert the Decimal number (108.025) to their binary equivalent.
(b) Draw Truth table of JK flip flop.
(c) Draw the truth table and logic circuit of Half-adder.
(d) Write the difference between combinational & Sequential circuit.
(e) Draw timing diagram of SR flip-flop.
(f) Find 2's complement of 1011011.
(g) Number of 2:1 mux requires designing 256:1 mux is .....
(h) Add hexadecimal number 2ABC & 98F2.
(i) Discuss Universal gates.
(j) What is the use of K-map?

Q.2 Implement the following function using only NAND gate **[14]**
$F(A,B,C)=\sum m(0,1,2,3,7)$.

Q.3 (a) Realize XNOR logic function using NAND gate only. **[7]**
(b) Simplify $Y= ABC + AB\bar{C} + A\bar{B}C$ **[7]**

Q.4 A logic circuit has four inputs A,B,C,D and output Y. Y=1 when A & B are both 1,subjected to the condition that C and D are both low or both high. Design the logic circuit. **[14]**

Q.5 Explain Master-slave flip flop. What are race around condition?. How it can be circumvented with the help of Master-slave flip flop. **[14]**

Q.6 (a) Design 8 to 3 line Encoder circuit. **[7]**
(b) Implement NAND gate using TTL logic family. **[7]**

Q.7 Summarize the design procedure for a synchronous sequential circuit. **[14]**

Q.8 (a) Explain the working of R-2R Ladder DAC. **[7]**
(b) Design 3-bit binary counter using T flip-flop. **[7]**

Q.9 Write short notes on the following: **[7*2=14]**
(a) Binary Parallel Adder
(b) Digital IC logic families