Bihar Engineering University, Patna

End Semester Examination – 2023

Course: B.Tech.	*Semester-IV*	*Time: 03 Hours*
Code: 105401	*Subject: Computer Organization and Architecture*	*Full Marks: 70*

Instructions:-

(i) The marks are indicated in the right-hand margin.
*(ii) There are **NINE** questions in this paper.*
*(iii) Attempt **FIVE** questions in all.*
(iv) Question No. 1 is compulsory.

Q.1 ***Choose the correct option of the following (any seven only):*** **[2 x 7 = 14]**

(a) A pipeline stage
- (i) Is sequential circuit
- (ii) Is combination circuit
- (iii) Consists of both sequential and combinational circuit
- (iv) None of these

(b) A direct mapped cache memory with n blocks is nothing but which of the following set associative cache memory originations
- (i) 0-way set associative
- (ii) 1-way set associative
- (iii) 2-way set associative
- (iv) n-way set associative

(c) The performance of a pipelined processor suffers if
- (i) The pipeline stages have different delays
- (ii) Consecutive instruction are dependent on each other
- (iii) The pipeline stages share hardware resources
- (iv) All of these

(d) A computer with cache access time of 100 ns, a main memory access time of 1000 ns, and a hit ratio of 0.9 produces an average access time of
- (i) 250 ns
- (ii) 200 ns
- (iii) 190 ns
- (iv) None of these

(e) Which of the following has no practical usage?
- (i) SISD
- (ii) SIMD
- (iii) MISD
- (iv) MIMD

(f) A micro programmed control unit
- (i) Is faster than a hardwired control unit
- (ii)Facilitates easy implementation of new instructions
- (iii) Is useful when every small program is to be run
- (iv) Usually refers to the control unit of the microprocessor

(g) In memory- mapped I/O…….
- (i) The I/O devices and the memory share the same address space.
- (ii) The I/O device have a separate address space
- (iii) The memory and I/O device have an associated address space
- (iv) A part of the memory is specifically set aside for the I/O operation

(h) How many 128x8 bit RAMs are required to design 32 k x 32 bit RAM?
- (i) 512
- (ii) 128
- (iii)1024
- (iv) 32

(i) The stalling of the processor due to the unavailability of the instruction is called as
- (i) Control hazard
- (ii) Structural hazard
- (iii) Input hazard
- (iv) None of the above

(j) The addressing mode, where you directly specify the operand value is
- (i) Immediate
- (ii) Direct
- (iii) Definite
- (iv) Relative

Q.2 (a) What are the hazards in pipeline architecture? Explain its types with suitable example. **[7]**

(b) What is addressing mode? Why do computers use addressing mode techniques? Explain two modes with example, which do not use address fields. **[7]**

Q.3	(a)	A 4- way set associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4GB. Find the number of bits for TAG, SET, and WORD fields in the address generated by CPU.	[7]
	(b)	How is the virtual address mapped into physical address? What are the different methods of writing into cache?	[7]
Q.4	(a)	What are the different types of instruction formats?	[7]
	(b)	Discuss the different mapping techniques used in cache memories and their relative merits and demerits.	[7]
Q.5	(a)	Design a 4-bit carry –look ahead adder and explain its operation with an example.	[7]
	(b)	Consider a direct mapped cache with 8 cache blocks (numbered 0-7).If the memory block requests are in the following order 3, 5, 2, 8, 0, 63, 9, 16, 20, 17, 25, 18, 30, 24, 2, 63, 5, 82, 17, 24.What would be the status of cache blocks (block numbers residing in cache) at the end of the sequence.	[7]
Q.6	(a)	What is DMA? Describe how DMA is used to transfer data from peripherals.	[7]
	(b)	Differentiate between hardwired and micro programmed control unit. Explain each component of hardwired control unit organization.	[7]
Q.7	(a)	What do you mean by asynchronous data transfer? Explain strobe control and hand shaking mechanism.	[7]
	(b)	Show the systematic multiplication process of (20) x (-19) using Booth's algorithm	[7]
Q.8	(a)	The stage delays in a four stages pipeline are 800, 500, 400 and 300 picoseconds. The first stage (with delay 800 picoseconds) is replaced with a functionally equivalent design involving two stages with respective delays 600 and 350 picoseconds. What would be the throughput increases (in percentage) of the pipeline?	[7]
	(b)	Explain IEEE standard for floating point representation with example.	[7]

Q.9 Write short notes on ***any two*** of the following : **[7x2=14]**

(a) Paging
(b) Memory interleaving
(c) Privileged and non- privileged instructions
(d) Locality of reference