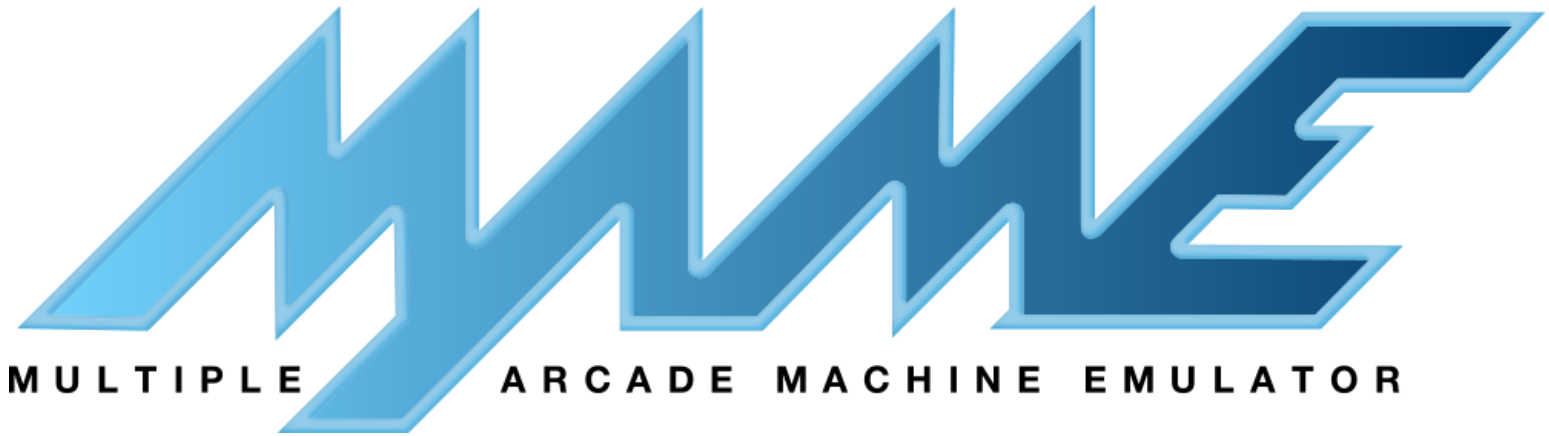
유부남이라도 철권 태그가 하고 싶어!

네코동 이정훈

2018.12

* 2018/11/23 캡쳐


MULTIPLE ARCADE MACHINE EMULATOR


STAGE-1
00'01"25
59
INSERT COIN
XIAOYU
BRYAN

Namco System 12

From Wikipedia, the free encyclopedia

The **Namco System 12** is an arcade system board released by Namco in late 1996. In hardware, it is an upgrade from Sony's PlayStation-based System 11, the MIPS R3000A microprocessor is 50% faster,[1] and the C76 sound processor is replaced by the H8/3002. [2]

PlayStation technical specifications

From Wikipedia, the free encyclopedia

Central processing unit (CPU) [edit]

LSI CoreWare CW33300-based core[1]

- MIPS R3000A-compatible 32-bit RISC CPU MIPS R3051 with 5 KB L1 cache, running at 33.8688 MHz.[2]
- The microprocessor was manufactured by LSI Logic Corp. with technology licensed from SGI.

Geometry Transfer Engine (GTE)

- Coprocessor that resides inside the main CPU processor, giving it additional vector math instructions used for 3D graphics, lighting, geometry, polygon and coordinate transformations – GTE performs high speed matrix multiplications.

GTE Coordinate Calculation Commands

COP2 0180001h - 15 Cycles - RTPS - Perspective Transformation (single)
COP2 0280030h - 23 Cycles - RTPT - Perspective Transformation (triple)
RTPS performs final Rotate, translate and perspective transformation on vertex V0. Before writing to the FIFOs, the older entries are moved one stage down. RTPT is same as RTPS, but repeats for V1 and V2. The "sf" bit should be usually set.

from NO$PSX Programming Specs (http://problemkaputt.de/psx-spx.htm)


STAGE 1
00'00"38
60
CREDIT 1
XIAOYU
KING


Non Interlace
Contrast :A0
Bright R :30
Bright G :30
Bright B :30


Interlace
Contrast :A0
Bright R :30
Bright G :30
Bright B :30


XIAOYU


XIAOYU


STAGE 1
00'02"85
58
XIAOYU
GUNJACK

GPU I/O Ports, DMA Channels, Commands, VRAM

GPU Command Summary

Commands/Packets consist of a 8bit command number (MSBs) and a 24bit parameter (LSBs), which are written as 32bit value to GP0 or GP1.

```
GP0(00h)                    - Nop?
GP0(01h,02h,80h,A0h,C0h)    - Direct VRAM Access
GP0(03h)                    - Unknown (does take up FIFO space!!!)
GP0(1Fh)                    - Interrupt Request (IRQ1)
GP0(20h..3Fh)               - Render Polygons
GP0(40h..5Fh)               - Render Lines
GP0(60h..7Fh)               - Render Rectangles
GP0(E1h..E6h)               - Rendering Attributes
GP1(00h..09h,10h,20h)       - Display Control (these via GP1 register)
```

Some GP0 commands require additional parameters, which are written (following to the command) as further 32bit values to GP0. The execution of the command starts when all parameters have been received (or, in case of Polygon/Line commands, when the first 3/2 vertices have been received).

from NO$PSX Programming Specs (http://problemkaputt.de/psx-spx.htm)

GPU I/O Ports, DMA Channels, Commands, VRAM

GPU I/O Ports (1F801810h and 1F801814h in Read/Write Directions)

Port	Name	Expl.
1F801810h-Write	GP0	Send GP0 Commands/Packets (Rendering and VRAM Access)
1F801814h-Write	GP1	Send GP1 Commands (Display Control) (and DMA Control)
1F801810h-Read	GPUREAD	Receive responses to GP0(C0h) and GP1(10h) commands
1F801814h-Read	GPUSTAT	Receive GPU Status Register

It (=GP0 only?) has a 64-byte (16-word) command FIFO buffer.

Optionally, Port 1F801810h (Read/Write) can be also accessed via DMA2.

GPU-related DMA Channels (DMA2 and DMA6)

Channel		Recommended for	
DMA2 in Linked Mode	-	Sending rendering commands	;GP0(20h..7Fh,E1h..E6h)
DMA2 in Continous Mode	-	VRAM transfers to/from GPU	;GP0(A0h,C0h)
DMA6	-	Initializing the Link List	;Main RAM

from NO$PSX Programming Specs (http://problemkaputt.de/psx-spx.htm)

Pete's PSX GPU Plugins

Pete's OpenGL2 PSX GPU	V 2.9	May 24, 2008	Win Emu plugin for modern cards
Pete's XGL2 Linux PSX GPU	V 2.9	May 24, 2008	Linux Emu plugin for modern cards
Pixel shaders		June 6, 2006	OGL2/XGL2 shader effect files
Pete's Windows PSX GPUs	V 1.77	May 24, 2008	Win Emu plugins (OGL/DX7/DX6)
P.E.Op.S./Pete's OpenGL Windows PSX GPU	V 1.78	April 01, 2009	Win Emu plugin (
P.E.Op.S./Pete's MesaGL Linux PSX GPU	V 1.78	April 01, 2009	Linux Emu plugin
P.E.Op.S. Soft GPU (Windows)	V 1.18b	May 25, 2008	Win Emu plugin (
P.E.Op.S. Soft GPU (Linux)	V 1.18	May 24, 2008	Linux Emu plugin
Linux GPU configs		July 17, 2008	Configuration too

Namco System 12

From Wikipedia, the free encyclopedia

- Main CPU: MIPS R3000A 32-bit RISC processor, @ 50.8032 MHz, Operating performance - 45 MIPS, Instruction Cache - 4 KiB
- BUS: 132 MB/s.
- OS ROM: 512 kibibytes
- Sound CPU: Hitachi H8/3002 @ 16.73735 MHz
- Additional Sound Chip: Namco C352 sample playback
- Main RAM: 2 megabytes
- Video VRAM: 2 megabytes
- Sound RAM: 512 kilobytes

PlayStation technical specifications

From Wikipedia, the free encyclopedia

Memory [edit]

- 2 MB main EDO DRAM[4]
- Additional RAM is integrated with the GPU (including a 1 MB framebuffer) and SPU (512 KB), see below for details.
- Cache RAM for CPU core and CD-ROM. See the relevant sections for details.
- Flash RAM support through the use of memory cards, see below.
- BIOS stored on 512 KB ROM


XIAOYU


XIAOYU


STAGE 1
00'03"28
58
CREDIT 1
XIAOYU
ANNA


STAGE 1
00'20"58
43
CREDITS 2
XIAOYU
HWOARANG