
DMAC
CPU
DMAC1 Req.
A Int. Req.
DMAC1 gets bus.
DMAC1 release bus.
DMAC1 Data 1 Transfer
DMAC1 Req.
B Int. Req.
DMAC1 gets bus.
DMAC1 release bus.
DMAC1 Data 2 Transfer
DMAC1 Req.
DMAC1 gets bus.
DMAC1 release bus.
DMAC1 Data 3 Transfer
DMAC1 Req.
DMAC1 gets bus.
DMAC1 release bus.
DMAC1 Data 4 Transfer
DMAC2 Req.
DMAC1 Req.
DMAC2 gets bus.
DMAC2 Data 1 Transfer
DMAC2 Data 2 Transfer
DMAC2 release bus.
DMAC1 gets bus.
DMAC1 release bus.
DMAC1 Data 5 Transfer
DMAC2 Req.
DMAC2 gets bus.
DMAC2 Data 1 Transfer
DMAC2 release bus.
DMAC2 Data 2 Transfer
IF & Decode
Operand Fetch
Execution
Result Write
Interrupt Housekeeping for B
IF & Decode
ISR B
Operand Fetch
ISR B
Execution
ISR B
Result Write
ISR B
IF & Decode
Operand Fetch
Execution
Result Write
Another Insruction from Main Program
Interrupt Housekeeping for A
IF & Decode
ISR A
Operand Fetch
ISR A
Execution
ISR A
Result Write
ISR A
0
30
40
50
100
160
170
210
260
310
510
560
570
610
710
760
820
870
880
920
1020
1230
1430
1640

Some Important Points:

- In DMA operations, the processor is at a lower bus priority level than DMAC's. (Please check slide 5.23). That means If a Direct Memory Access Controller (DMAC) is requested before another DMAC has finished, control switches to the requested DMAC instead of the CPU. (Check transition at 710ns from timeline)
- ISR execution follows a same stage-based process as regular instructions, including fetch and decode, operand fetch, execution, result write. (Nothing different than main program instruction)
- After executing the Interrupt Service Routine (ISR) and returning with the Return from Interrupt (RTI) instruction, the CPU proceeds to the next regular instruction even if there is a pending interrupt. (Check transition at 1020ns from timeline, as you can see before the processing Interrupt A, a main program instruction executed)

a)

Word	**Finish Time**
First	100 ns
Second	210 ns
Third	310 ns
Fourth	560 ns
Fifth	760 ns

b) DMAC2's completed first attempt at 710 ns
c) DMAC2's completed second attempt at 1020 ns
d) ISR A completed at 1640 ns
e) ISR B completed at 920 ns