Istanbul Technical University

Department of Computer Engineering

BLG 322E - COMPUTER ARCHITECTURE

Assignment 1

Due Date: Wednesday, February 28, 2024, 23:59.

- Please **write and draw neatly**.
- You may draw the circuits by hand. Please use a ruler and draw neatly.
- Please **write your full name** (first name and last name) **and Student ID** at the top of your solution.
- Please show ALL work. Answers with no supporting explanations or work will not receive any partial credit. Your homework is not just a final report of your results; we want to see your steps. Upload all the papers you worked on to get to the solution.
- **Submissions:** Submit your solution as a PDF file to Ninova before the deadline.
- **No late submissions** will be accepted. Do not send your solutions by e-mail. We will only accept files that have been uploaded to the official Ninova e-learning system before the deadline. Do not risk leaving your submission to the last few minutes.
- **Consequences of plagiarism:** Any cheating will be subject to disciplinary action.

If you have any questions, please e-mail **Altay Ünal (unal21@itu.edu.tr).**

QUESTION:

You will design a pipeline that will execute the arithmetic operation $|A_i - C_i| * B_i + |B_i - A_i|$ where A, B, and C are arrays that consist of 8-bit signed integers represented by 2's complement. In this design, you are allowed to use the following:

- 5 adder/subtracter circuits
- 1 multiplication circuit
- 2 D flip flops
- 2 XOR circuits
- Pipeline registers

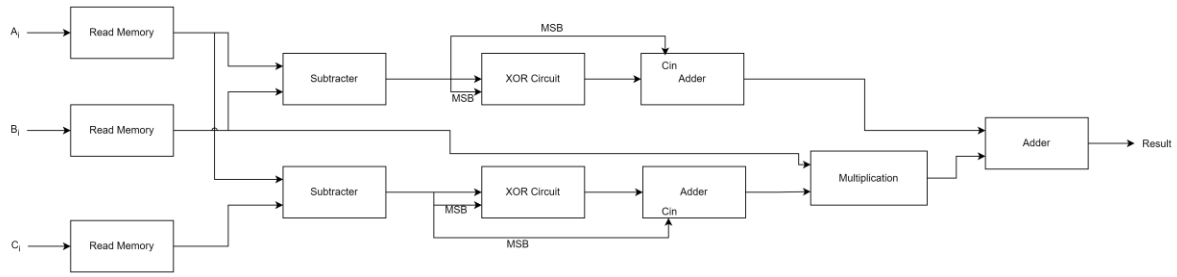

Figure 1: The circuit performing the given operation.

The sequential circuit for this operation is given in Figure 1. Do not show the internal structure of the adder/subtracter, show it only as a block. Assume that the circuits you use in your design have the following delays:

- Memory access time: **50 ns**
- Register delay: **5 ns**
- D flip flop delay: **5 ns**
- 8-bit adder/subtracter propagation delay: **25 ns**
- 16-bit adder/subtracter propagation delay: **40 ns**
- Multiplication circuit propagation delay: **35 ns**
- XOR circuit delay: **10 ns**

a) Design and draw the optimum pipeline structure in terms of primarily speedup and secondarily the waiting time for the first result. Fully label all devices and show the lengths of the pipeline registers. **(50 pts)**

b) What is the cycle time of your pipeline? **(10 pts)**

c) Using the pipeline, how long does it take to execute the task on only the first element? **(15 pts)**

d) If the pipeline was not used, the time required to complete one task would be calculated as the total delay of the combinatorial circuit elements on the longest path in the designed structure. What speedup does this pipeline achieve when it executes a task on an array having

  a. an infinite number of elements? (**5 pts)**

  b. 5 elements? **(5 pts)**

e) What is the theoretical maximum speedup of your pipeline? **(15 pts)**

(Note: Theoretical maximum speedup and the speedup on an infinite number of elements are NOT the same thing. Read the lecture notes carefully.**)**