

# Computer Architecture

BLG 322E

## Homework 1 Report

KAAN KARATAŞ

karatask20@itu.edu.tr

Faculty of Computer and Informatics Engineering

Department of Computer Engineering

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# 1. A - Pipeline Design

The optimum pipeline design wanted in question A is given below:

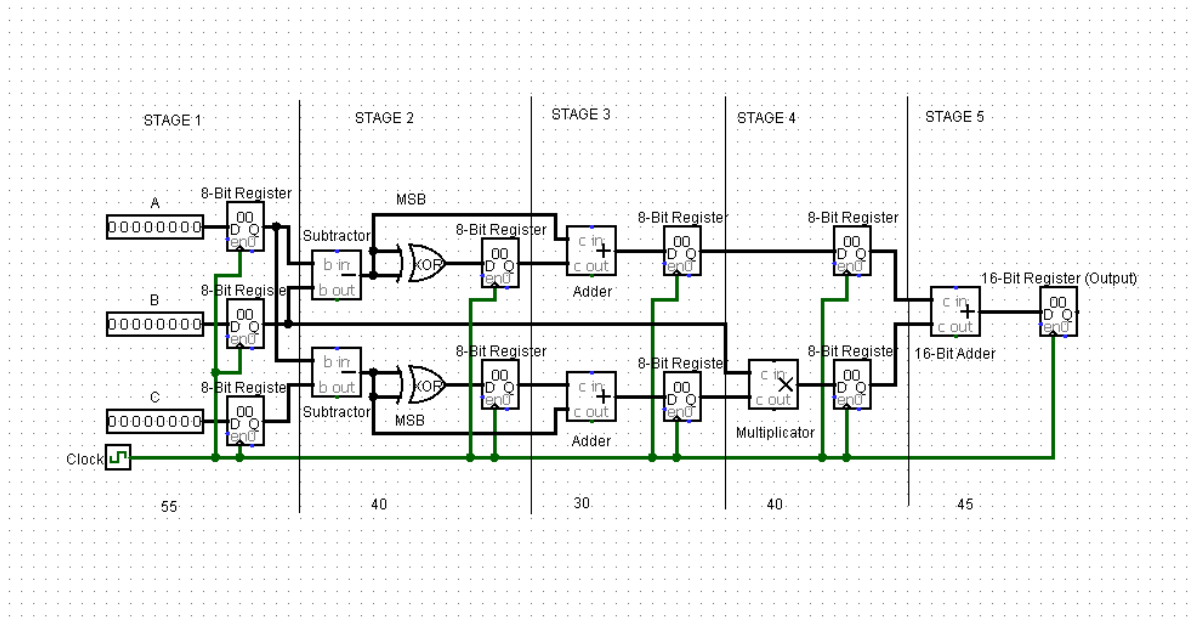


Figure 1.1: pipeline

Priority is primarily given to Speedup and then secondarily first result waiting time. The longest path is through memory access (50 ns), Register (5 ns), 8-bit Subtractor (25 ns), XOR Gate (10 ns), Register (5 ns), 8-bit Adder (25 ns), Register (5 ns), Multiplier (35 ns), Register, 16-bit Adder (40), and an Output Register (5 ns).

This operation is divided to 5 small and balanced stages to optimize Speedup. The duration of operations have been tried to be calculated small in order to improve the performance of the pipeline as it is dependent on the slowest clock cycle.

## 2. Calculations

### 2.1. B - Cycle Time

The cycle time of the pipeline is determinant on the stage that takes the longest time. As seen on the pipeline design, the slowest stage is Stage 1 (memory access stage) with a duration of 55 ns.

### 2.2. C - First Element Operation Time

As the pipeline consists 5 stages with a cycle time of 55 ns, the time that takes for the first element to be finished is  $5 * 55 = 275$ .

### 2.3. D - Speedup Calculation

#### 2.3.1. a. Infinite Elements

For the case with infinite number of elements, the speedup can be calculated using formula:  $S_{lim_{n \rightarrow \infty}} = \frac{t_n}{t_p}$ . "tn" corresponds to time of an element without pipelining, "tp" corresponds to time with pipelining. Thus, the result is:

$$\frac{185}{55} = 3.\overline{36}$$

#### 2.3.2. b. 5 Elements

For the case with infinite number of elements, the speedup can be calculated using formula:  $\frac{t_n * n}{(n+k-1) * t_p}$ . "tn" corresponds to time of an element without pipelining, "tp" corresponds to time with pipelining. n is number of elements and k is number of stages in the pipeline. Thus, the result is:

$$\frac{185 * 5}{55 * 9} = 1.\overline{86}$$

### 2.4. E - Theoretical Maximum Speedup

Theoretical maximum speedup occurs when tasks overlap perfectly, and each stage operates in parallel on distinct elements. In this ideal situation, the theoretical maximum speedup aligns with the number of stages in the pipeline. Thus, in this instance, the theoretical maximum speedup is 5.