# ISTANBUL TECHNICAL UNIVERSITY

## COMPUTER ENGINEERING DEPARTMENT

# BLG 242E
# LOGIC CIRCUITS LABORATORY
# EXPERIMENT REPORT

| | | |
|---|---|---|
| **EXPERIMENT NO** | : | 4 (MAKEUP) |
| **EXPERIMENT DATE** | : | 15/05/2023 |
| **LAB SESSION** | : | FRIDAY - 14.00 |
| **GROUP NO** | : | G08 |

## GROUP MEMBERS:


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**SPRING 2023**

# Contents

# 1 INTRODUCTION

Throughout this experiment, the C.A.D.E.T. was tested while an S-R Latch without enable (NOR), an S-R Latch with enable (NAND), aD flip flop, a counter and a pulse generator circuits were designed and built. According to the circuits, truth tables were produced, and the outcomes were compared to the C.A.D.E.T. unit. The experiments' primary goal was to create and examine data storage elements: latches and flip-flops.

# 2 MATERIALS AND METHODS

Tools used on this experiment:

- C.A.D.E.T
- 7400 series ICs
- Oscilloscope
  - 74xx00 - Quadruple 2-input Positive NAND Gates
  - 74xx02 - Quadruple 2-input Positive NOR Gates
  - 74xx04 - Hex Inverters
  - 74xx75 - Quadruple Bistable D Type Latches
  - 74xx165 - 8-Bit Parallel Input/Serial Output Shift Register

# 3 EXPERIMENT

## 3.1 Part 1

An S-R latch without enable input is implemented with only NOR gates.

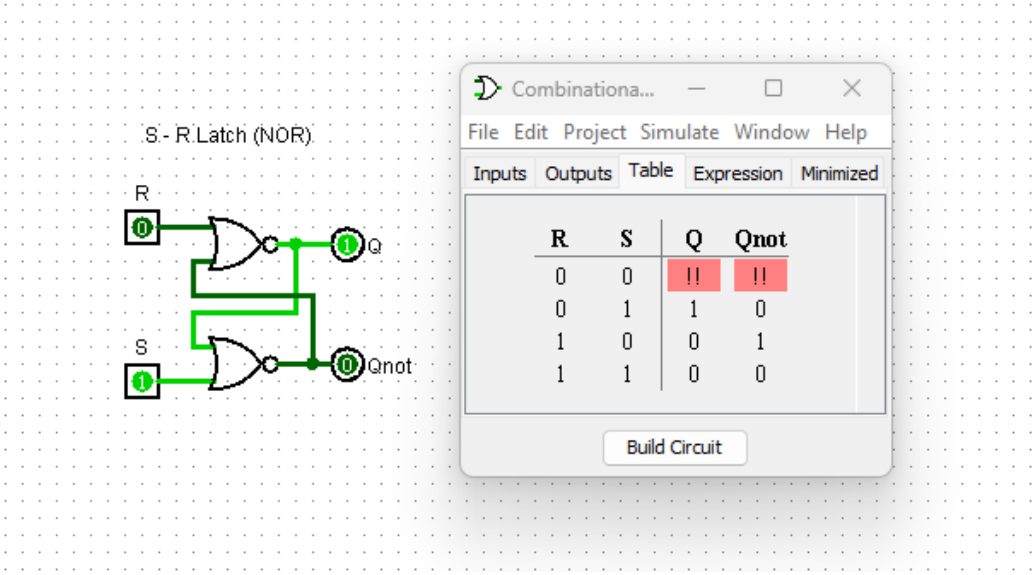


Figure 1: S-R Latch (NOR) Circuit

| R | S | Q | $Q_{not}$ |
|---|---|---|---|
| 0 | 0 | Q | $Q_{not}$ |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0(INVALID) | 0(INVALID) |

Truth Table of S-R latch without enable

## 3.2 Part 2

An S-R latch with enable input is implemented with only NAND gates.

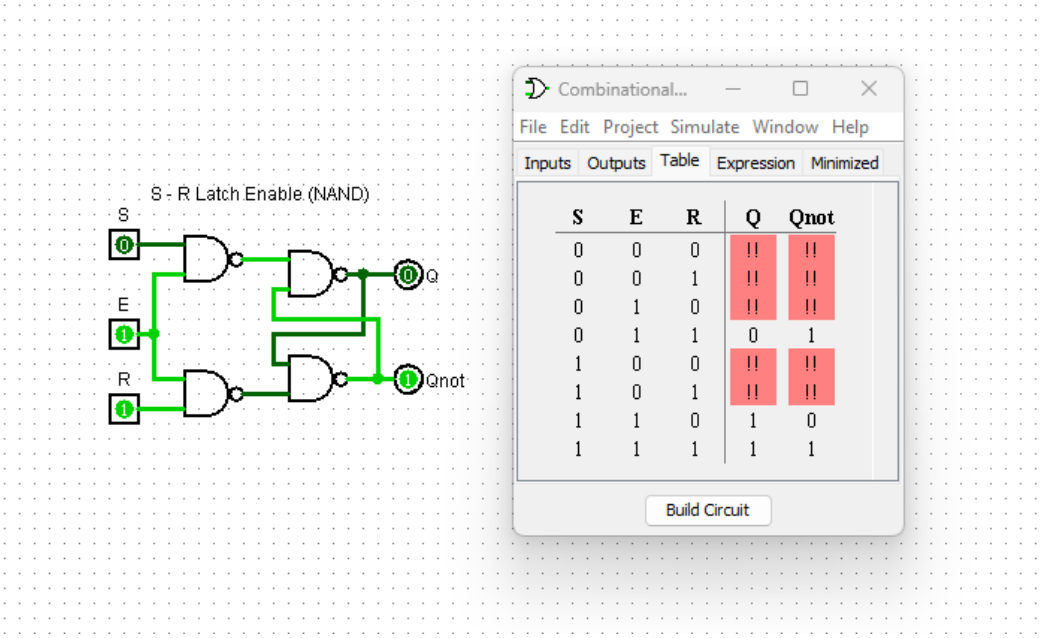


Figure 2: S-R Latch Enable (NAND) Circuit

| E | S | R | Q | $Q_{not}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | Q | $Q_{not}$ |
| 0 | 0 | 1 | Q | $Q_{not}$ |
| 0 | 1 | 0 | Q | $Q_{not}$ |
| 0 | 1 | 1 | Q | $Q_{not}$ |
| 1 | 0 | 0 | Q | $Q_{not}$ |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0(INVALID) | 0(INVALID) |

Truth Table of S-R Latch with enable

## 3.3 Part 3

A negative edge triggered D type flip-flop is implemented using D latches. (And a bonus positive edge triggered)

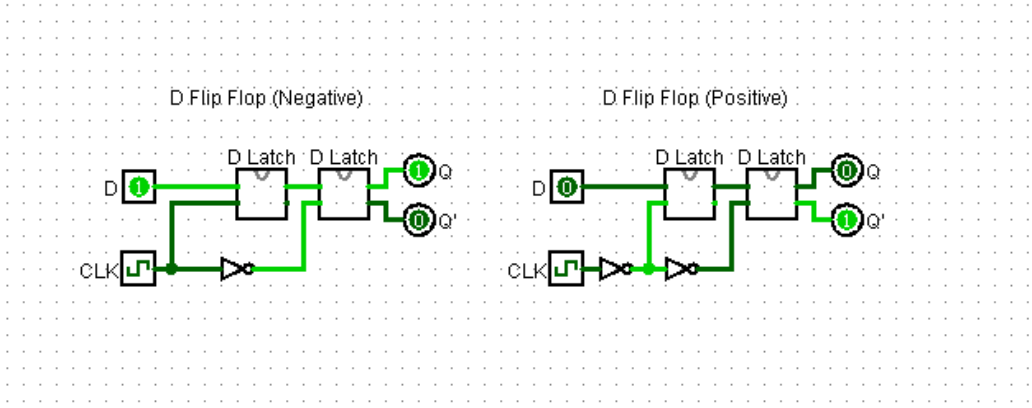


Figure 3: D Flip Flop Circuit

| CLK | D | Q | $Q_{not}$ |
|---|---|---|---|
| ↑ | 0 | Q | $Q_{not}$ |
| ↑ | 1 | Q | $Q_{not}$ |
| ↓ | 0 | 0 | 1 |
| ↓ | 1 | 1 | 0 |

Truth Table of negative edge triggered D type flip-flop

## 3.4 Part 4

In this section, a pulse generator is implemented using a shift register. After the circuit is built, various outputs are generated.

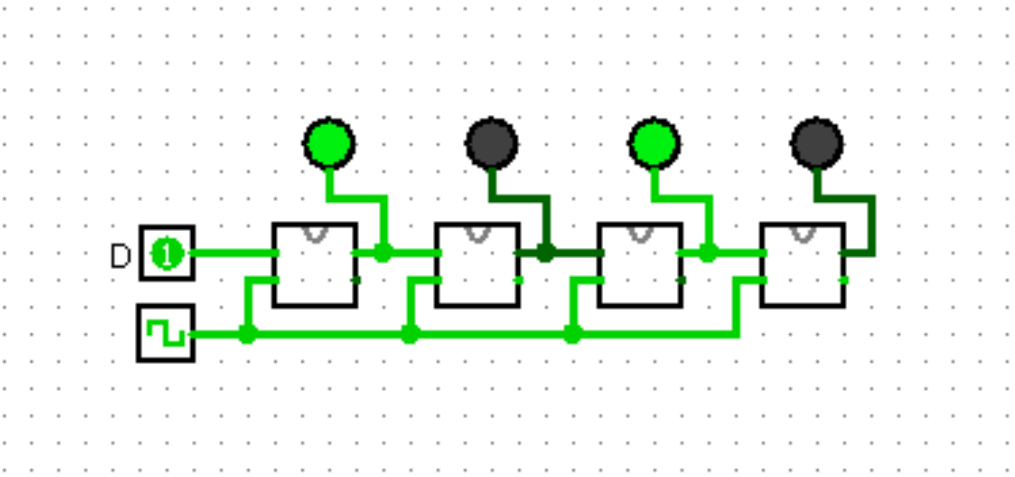


Figure 4: Shift Register Circuit

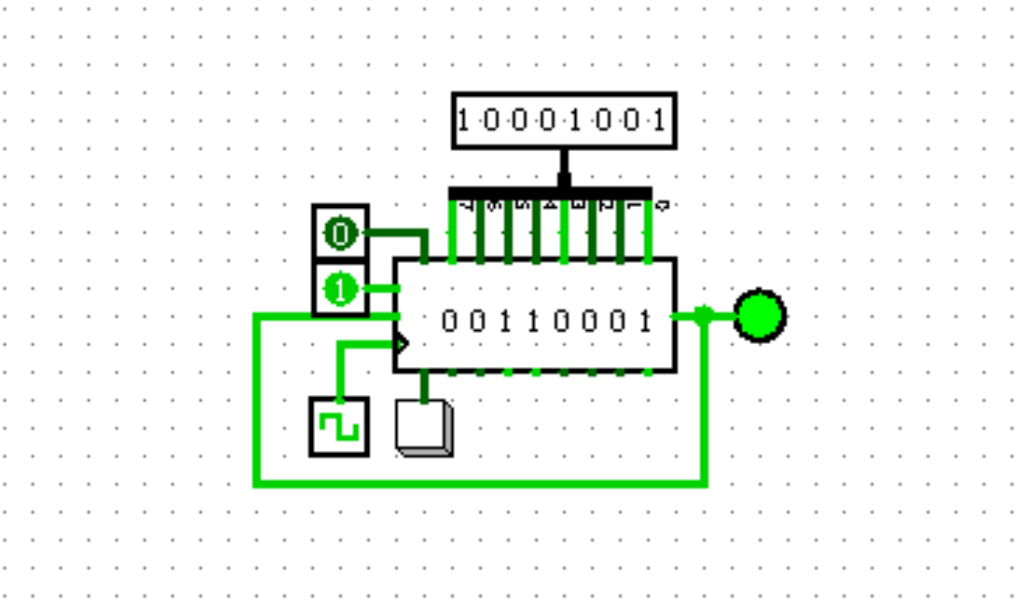


Figure 5: Pulse Generator Circuit

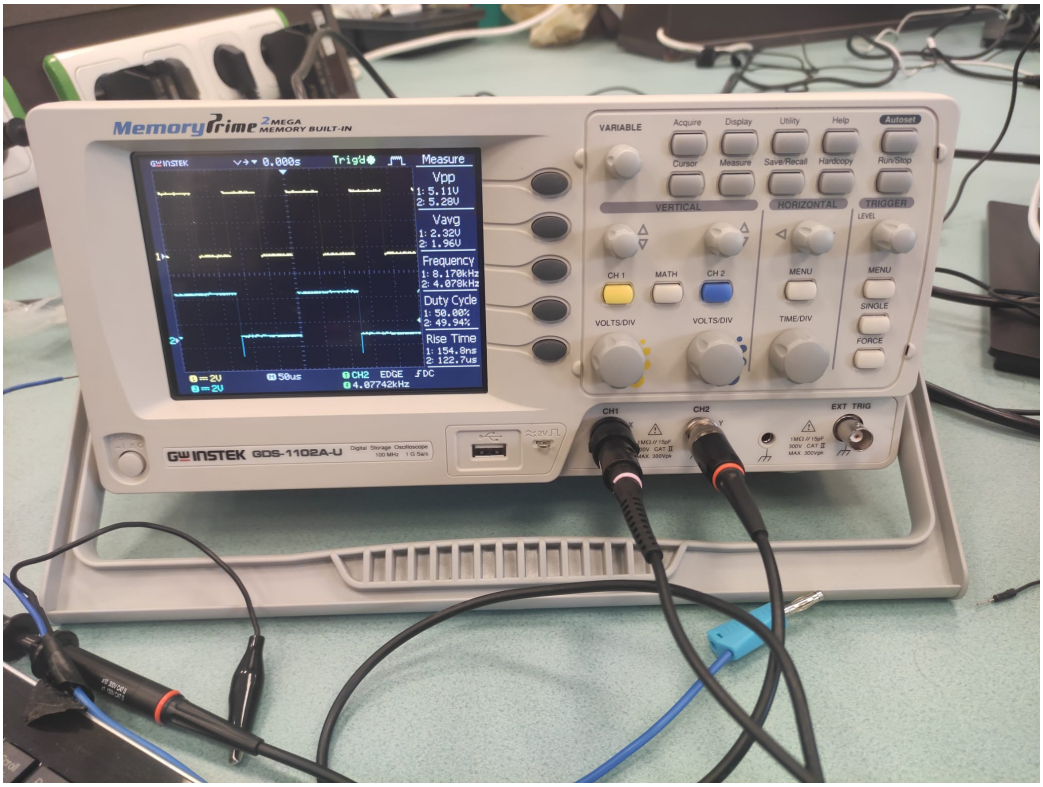


Figure 6: 1/2 Oscilloscope

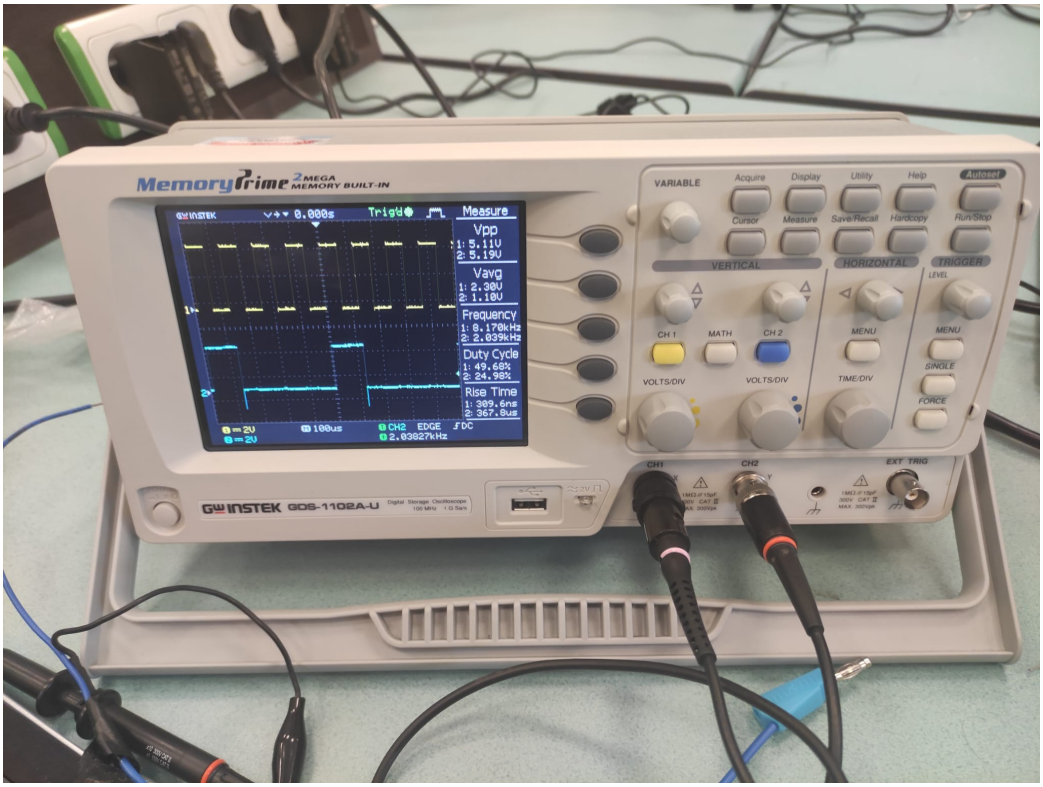


Figure 7: 1/4 Oscilloscope

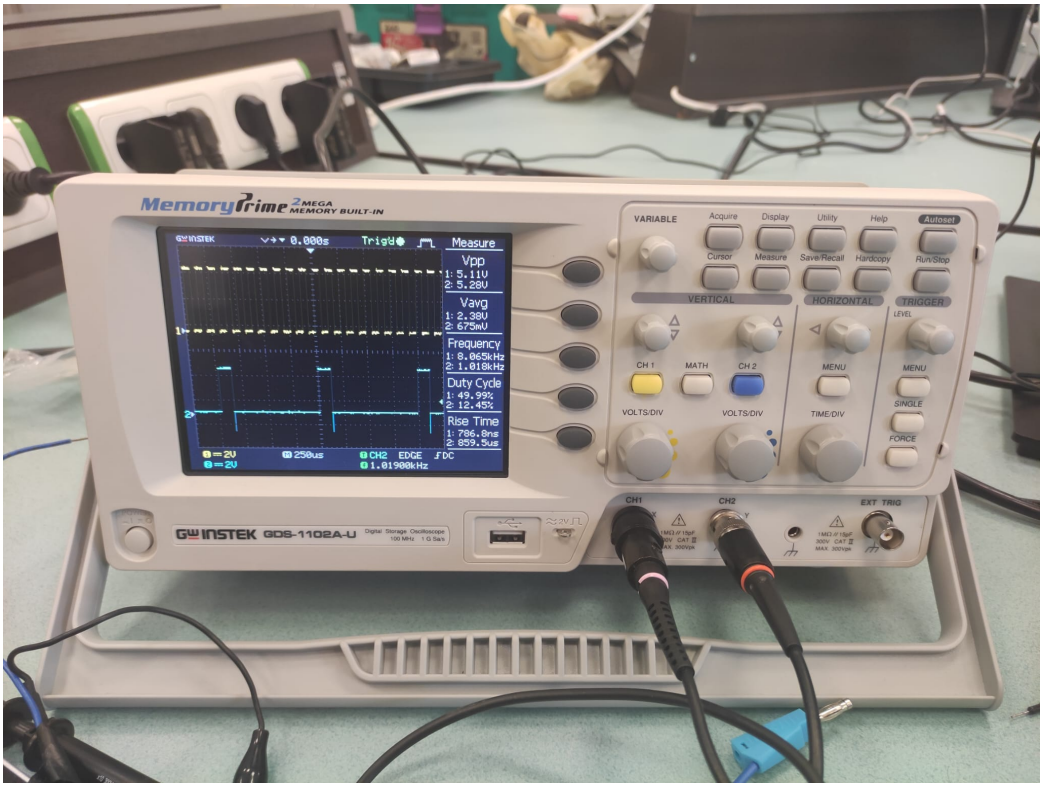


Figure 8: 1/8 Oscilloscope

### 3.5 Part 5

In this part, a circular counter that counts from 0 to 5 is implemented.

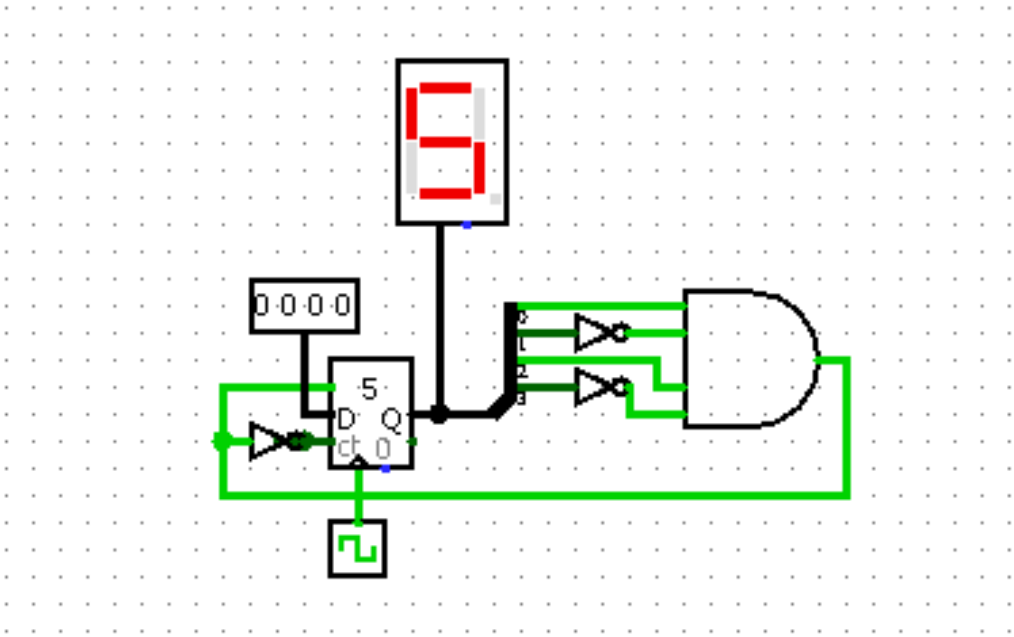


Figure 9: Counter To 5 Circuit

# 4 RESULTS

Every circuit design is implemented using Logisim. The intended outputs are obtained when the circuits are configured with all of the provided functionalities. An S-R Latch, S-R Latch (enable), D type flip flop, counter and pulse generator circuits are obtained. The circuits' outcomes were consistent with their truth tables.

# 5 DISCUSSION

In the experiment, we learnt to implement an S-R Latch, and create an S-R Latch with a different gate and adding additional enable input. After that, D flip flop and other specified circuits are implemented.

# 6 CONCLUSION

Although this week's experiment was considerably hard, We completed the experiment without facing many issues. We had the chance to fully grasp how flip-flops, shifters and pulse generators work and had the opportunity to build and test them.