



Verilog HDL True Dual-Port RAM with Single Clock

Table 1. True Dual-Port RAM with a Single Clock Port Listing

Related Links

This example describes a 64 bit x 8 bit synchronous, true dual-port RAM design with any combination of independent read or write operations in the same clock cycle in Verilog HDL. The design unit dynamically switches between read and write operations with the write enable input of the respective port. Synthesis tools are able to detect RAM designs in the HDL code and automatically infer the `altsyncram` or `altdpram` functions depending on the target device architecture.

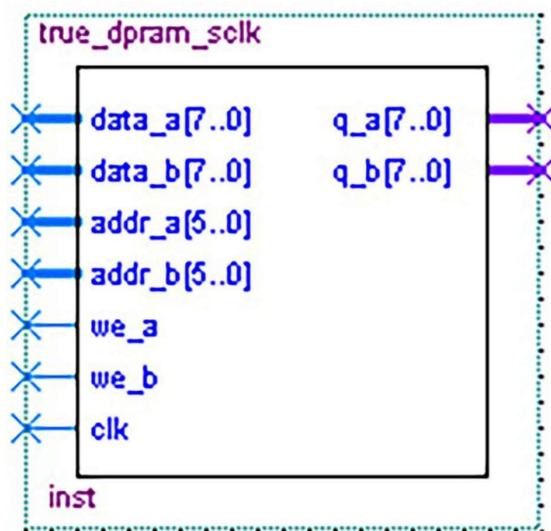


Figure 1. True Dual-Port RAM with a Single Clock Top-Level Diagram

Download the files used in this example:

- [Download true_dpram_sclk_v.zip](#) ›
- [Download True Dual Port RAM with a Single Clock README File](#) ›

Table 1. True Dual-Port RAM with a Single Clock Port Listing

Port Name	Type	Description
dataa[7:0], datab[7:0]	Input	8 bit data inputs of port A and port B
addr_a[5:0], addr_b[5:0]	Input	6 bit address inputs of port A and port B
we_a, we_b	Input	Write enable inputs of port A and port B
clk	Input	Clock input
q_a[7:0], q_b[7:0]	Output	8 bit data outputs of port A and port B

Related Links

- Recommended HDL coding styles chapter of the Intel® Quartus® Prime software user guide ›
- How to use Verilog HDL examples ›

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