Workshop on FPGA-based Accelerated Cloud Computing @ ASAP 2018

Register at: https://goo.gl/forms/8Wm1imRkVezJf0bK2

🕐 July 13rd 2018 from 9am to 6pm

📍 Co-located with the ASAP 2018 conference at Politecnico di Milano, Milan, Italy

Introduction

The increasing computational requirements of next-generation Cloud and High-Performance Computing (HPC) applications are pushing the adoption of accelerated computing based on heterogeneous architectures into mainstream as traditional CPU technology is unable to keep pace. FPGA accelerators complement CPU-based architectures and deliver significant performance- and power-efficiency improvements. In this regard, Xilinx FPGAs are now available on the Amazon Elastic Compute Cloud (EC2) F1 instances, which are designed to accelerate data centre workloads, including machine learning inference, data analytics, video processing, and genomics. These are available in two different sizes that include up to eight Virtex UltraScale+ VU9P FPGAs. Furthermore, Amazon Web Services offers the SDAccel Development Environment for cloud acceleration, enabling the user to easily and productively develop accelerated algorithms and then efficiently implement and deploy them onto the heterogeneous CPU-FPGA system. The high performance and high level of scalability offered by F1 instances, paired with the power and ease of use of Xilinx SDAccel, is very appealing for the development of high-performance FPGA-based accelerated solutions and will be the focus of this tutorial.

Organizers

Cathal McCabe - Xilinx University Program, Xilinx Ireland
Lorenzo Di Tucci - Politecnico di Milano
Marco Rabozzi - Politecnico di Milano
Marco D. Santambrogio - Politecnico di Milano

Preliminary schedule

9.00 - 12.00 - Introduction and fundamentals
- Introduction to FPGA-based acceleration
- Xilinx SDAccel development framework
- AWS EC2 F1 platform, and use cases.

12.00 - 13.00 - Lunch

13.00 - 18.00 - Lab session
- Connecting to an AWS EC2 F1 instance,
- Using an AWS F1 instance to accelerate complex workloads,
- Developing and optimizing AWS F1 applications with SDAccel
- Optimizing host and FPGA code, and
- Integrating IP into SDAccel-based code.