Chisel Bootcamp @ ASAP 2018

Registration Link https://goo.gl/forms/qGBAeiiXwD4JMkcr1

Introduction

Chisel (Constructing Hardware In a Scala Embedded Language) is a Berkeley Hardware Construction DSL written in Scala that aims at changing the way electronic system design takes place. Beside the opportunity to design circuits, Chisel allows to design *circuit generators*: programs that automatically generate designs from a high level of parameters and constraints. By doing this, Chisel wants to leverage the hard work of design experts while at the same time raising the level of abstraction. Furthermore, Chisel integrates multiple aspects from modern programming languages that are missing in HDLs like Verilog and VHDL as object-oriented programming, functional programming support and type inference.
Starting from an introduction to Scala, this full-day bootcamp will provide the motivations behind Chisel as well as its fundamentals with both a theoretical and hands-on session. The attendee will be guided into the creation of a new chisel project, showing how to design and test exploiting the potentiality of this language.

Date/Time

July 9th 2018 from 9am to 6pm

Organizers

[David Donofrio](#) - Lawrence Berkeley National Laboratory
[Lorenzo Di Tucci](#) - Politecnico di Milano
Davide Conficconi - Politecnico di Milano
Alessandro Comodi - Politecnico di Milano
[Marco D. Santambrogio](#) - Politecnico di Milano

Schedule

09 - 13:

- Chisel: History and Motivation
- A Basic Introduction to Scala
- Fundamentals - Exposing all (most) of Verilog using Chisel
- Project creation
- Testing Environment

13 - 14 : Lunch

14 - 18 : Hands-on session