Politecnico di Milano

P2CWeek: EUC & ISPA 2014

POLITECNICO DI MILANO

Contents

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Other information

- Expected duration of the tutorial: full day
- Morning: lectures and demos
- Afternoon: hands-on exercises

Organizer short bio - Simone Campanoni is a research associate in Computer Science at Harvard University working with Prof. David Brooks and with Prof. Gu-yeon Wei. His work focuses on the boundary between hardware and software, relying on dynamic compilation, run-time optimizations and virtual execution environments for investigating opportunities on auto-parallelization. He is the author of the HELIX research project (http://helix.eecs.harvard.edu) and the ILDJIT compilation framework (http://ildjit.sourceforge.net).

P2Cweek: ISPA & EUC

About P2C

Parallel and Pervasive Week (P2CWeek) is a premier event covering very important aspects of computing systems. By bringing together two international conferences (EUC and ISPA), and several workshops, P2CWeek allows attendees to benefit from a wide range of topics covering the state of the art in computing systems and architectures research and development.
The P2C week will be held in Milan from Monday 25 August to Friday 29 August 2014.

One registration, two conferences and workshops

Registered attendees will be allowed to attend sessions in the other conference and tutorials for free: EUC 2014, ISPA 2014. Please note that symposia and workshops may require separate registration.

Welcome to EUC

Embedded and ubiquitous computing is an exciting paradigm that promises to provide computing and communication services to the end users all the time and everywhere. Its systems are now invading in every aspect of our daily life and promise to revolutionize our life much more profoundly than elevators, electric motors or even personal computer evolution ever did. The emergence of this technology is a natural outcome of research and technological advances in a variety of areas including embedded systems, pervasive computing and communications, wireless networks, mobile computing, distributed computing and agent technologies.
EUC 2014 is the next event, in a series of highly successful International Conferences on embedded and Ubiquitous Computing (EUC), previously held as ICDCS-ECS04 (Tokyo, Japan, March 2004), EUC-04 (Aizu, Japan, August 2004), EUC-05 (Nagasaki, Japan, December 2005), EUC-06 (Seoul, Korea, August 2006), EUC-07 (Taipei, Taiwan, December 2007), EUC-08 (Shanghai, China, December 2008), EUC-09 (Vancouver, Canada, August 2009), EUC-10 (Hong Kong,China, December 2010), EUC-11 (Melbourne, Australia, October 2011), EUC-12 (Paphos, Cyprus, December 2012) and EUC-13 (Zhangjiajie, China, November 2013).

EUC 2014 will take place in Milan, Italy and it is part of the **P2CWeek 2014** (Parallel and Pervasive Computing Week) event. The conference will be held from 26 August 2014 to 28 August 2014.

Welcome to ISPA

ISPA-14 (12th IEEE International Symposium on Parallel and Distributed Processing with Applications) is a forum for leading work on parallel and distributed computing and networking, including architecture, compilers, runtime systems, applications, reliability, security, parallel programming models and much more. During the symposium, scientists and engineers in both academia and industry are invited to present their work on concurrent and parallel systems (multicore, multithreaded, heterogeneous, clustered systems, distributed systems, grids, clouds, and large scale machines).
The 12th ISPA follows the tradition of previous successful ISPA conferences, ISPA-03 (Aizu, Japan), ISPA-04 (Hong Kong), ISPA-05 (Nanjing, China), ISPA-06 (Sorrento, Italy), ISPA-07 (Niagara Falls, Canada), ISPA-08 (Sydney, Australia), ISPA-09 (Chengdu, China), ISPA-10 (Taipei, Taiwan), ISPA-11 (Busan, Korea), ISPA-12 (Madrid, Spain) and ISPA-13 (Melbourne, Australia). It will feature session presentations, workshops, tutorials and keynote speeches. ISPA-14 is sponsored by IEEE Technical Committee on Scalable Computing (TCSC) and IEEE Computer Society.
The objective of ISPA-14 is to provide a forum for scientists and engineers in academia and industry to exchange and discuss their experiences, new ideas, research results, and applications about all aspects of parallel and distributed computing and networking. It will feature session presentations, workshops, tutorials **and keynote speeches.**

Venue

Milan
With a population of about 1.3 million, Milan, the capital of Lombardy, is located in the Po Valley, not far from the Alps with the great lakes (Lake Como, Lake Maggiore, Lake Lugano) to the North.
Milan is considered the Italian economic and finance center, with the headquarters of the Stock Exchange and of many of the most important industrial and financial businesses of the Country.
It is also the Italian symbol of fashion and design: it hosts many of the main Italian fashion maisons and international design fairs, such as "Settimana della Moda" (Milan Fashion Week) and the "Salone Internazionale del Mobile"(Milan Furniture Fair); also, a Design School operates at Politecnico di Milano.
Milan hosts the "Teatro alla Scala", considered the temple of lyrics all over the world, and several prose theatres such as the "Piccolo Teatro" founded by **Giorgio Strehler.**
In Milan are located the headquarters of the main daily newspapers (Il Corriere della Sera, Il Sole 24 Ore) and many of the main Italian publishers (Mondadori, Feltrinelli, Garzanti, Rizzoli).
The city offers to visitors the possibility to admire a wide range of monuments, museums and buildings reflecting the vestiges of history and culture left by many people who lived here. The ancient Roman remains are preserved at the Colonne di San Lorenzo, whereas the Romanesque can be admired at Sant'Ambrogio, Sant'Eustorgio or San Simpliciano Basilicas. The Duomo is one of the largest cathedrals in the world and the most important example of Gothic architecture in Italy.
The Castello Sforzesco, built on the wishes of the Duke Francesco Sforza, nowadays hosts the **Michelangelo's** "Pietà Rondanini" and several museums. The church of Santa Maria delle Grazie hosts the famous masterpiece "The Last Supper" by **Leonardo da Vinci** - declared part of the World Heritage by UNESCO.
The city has always participated actively to the National History since its origins, contributing to the purposes and the aims that led to reunification of Italy in the 18th century. Some distinguished people, who gave a significant contribution to Italian culture, lived in Milan, such as **Leonardo da Vinci** (who lived in Milan from 1482 to 1500), the poet and novelist Alessandro Manzoni, the musician **Arturo Toscanini**, the writer **Carlo Emilio Gadda**, the film director **Luchino Visconti**. Two Nobel prizes operated in Milan: **Giulio Natta** (1963, in chemistry) and **Dario Fo** (1997, in literature).
Expo 2015 is the next scheduled Universal Exposition and between May 1st and October 31st 2015 will be hosted in Milan. The Expo goal is not only to show the latest advances in technology, but also to welcome and to interpret the new challenges that human mankind faces nowadays. A theme of Expo 2015 will be "Feeding the planet, energy for life".

Politecnico di Milano
Politecnico di Milano is one of the most outstanding universities in Europe, ranked 28th in the world and 9th in Europe among technical universities, according to the QS World University Ranking – Engineering & Technology 2013. Founded in 1863, Politecnico di Milano is the largest school of architecture, design and engineering in Italy, with three main campuses located in Milan and five more branches around the Lombardy region.
Many important scientists and architects studied and taught here, among them **Achille Castiglioni**, **Gio Ponti**, **Gae Aulenti**, **Renzo Piano** and **Aldo Rossi**, both Pritzker Prize in 1990 and 1998 respectively, and Giulio Natta, Nobel Prize in Chemistry in 1963.
Research linked to didactics is a priority commitment that allows Politecnico di Milano to achieve high quality results also at an international level, developing a fruitful relationship with business and productive world by means of experimental research and technological transfer.
Politecnico takes part in several research and training projects collaborating with the most qualified European universities, together with national and international companies and institutions.

static ones. This workshop aims at bringing together experts to discuss current technologies and trends in the reconfigurable computing area. This tutorial tends to focus on different topics/objectives of the design of computing systems to include reconfigurability as an explicit design concept. Current tools seem to lack a framework for system design where run-time adaptability, provided by dynamic hardware reconfiguration, becomes pivotal to computing system design.
In this tutorial we will present cutting-edge research aiming at developing techniques and tools that analyze the structure and performance of the application, map it according to the capabilities of the underlying implementation platform, and provide a dynamically reconfigurable system implementation, e.g. through both micro-reconfiguration and module-based reconfiguration.

ILDJIT: Hands-On ILDJIT 2.0 for Static and Dynamic Program Analysis and Transformation

ILDJIT is a mature, open source, publicly available compilation framework that includes both static and dynamic compilers. Examples of well known benchmark suites supported by ILDJIT are SPEC CPU2000, SPEC CPU2006, MiBench and PARSEC. ILDJIT provides a plugin-based framework for static, as well as dynamic tasks like code translation, code analysis, code optimization, runtime instrumentation and memory management. Its plugin-based framework allows users to easily customize execution both at installation time and at run-time (by dynamically loading and unloading plugins without perturbing execution). Moreover, its multi-threaded design allows novel introspection of parallel compilation strategies to reduce overheads and dynamically optimize running code on today's x86 multi-core systems.
The framework provides a rich intermediate language (IR), which users can exploit inside their own extensions. ILDJIT allows users to choose which extensions to execute at static time and which ones to execute at runtime. In order to simplify the implementation of high level code analysis, IR includes both simple RISC-like instructions (e.g. load, store, add) and high level operations. High level operations include both classic thread synchronization tasks, such as wait for another thread, create thread, memory barriers and memory management tasks, such as create a new array, free a piece of memory and create a new aligned piece of memory.
ILDJIT supports the CIL language, which includes the full information of the source language by having a rich set of metadata. Nowadays, several source languages are successfully translated to CIL including C, C++, C#, Java, Python and LISP. Hence, by providing the full support of the complex CIL language, ILDJIT is able to manage, analyze and optimize all of the above languages. Users of ILDJIT do not need to handle unnecessary details of the source language used because they can rely on the IR of ILDJIT to perform their tasks.
We believe ILDJIT is useful to anyone interested in compilers and computer architecture research. It provides a platform for dynamically introspecting and performing code transformations on CIL bytecode programs. These management environments are emerging as the dominant front for run-time execution because of their platform-independent interoperability. In this tutorial, we demonstrate how users can exploit the ILDJIT framework for research-specific purposes. We will compare and contrast the ease of using ILDJIT relative to more commonly known tools like Pin and Dynamo. We will also demonstrate the ease of using ILDJIT relative to its CIL counterparts like Mono, DotNet and DotGNU that, while robust, are not well suited for research purposes. Design and development of software includes the monitoring of its runtime behaviors (e.g. for performance or memory usage evaluation), which depend on both the underlying platform and the compilation process. On the other hand, the design of new hardware includes evaluation of both its performance and power consumption while running software that expose typical workloads. Hence, both software and hardware evaluation need runtime analysis, which should also include static or dynamic software transformations.

Workshops and Tutorials

Workshops

Xilinx Workshop

During this Xilinx University Program professor workshop, attendees will have an opportunity to learn about the latest Xilinx technology, devices, and trends, and will gain practical experience of working with Xilinx Vivado, IP Integrator, and Vivado HLS to create designs for Xilinx Zynq All Programmable SOC devices. There will also be an opportunity to network with Xilinx University Program staff and find out about the Xilinx University Program. Topics covered will include an introduction to Xilinx 7 series devices and technology, an overview of the new Vivado design flow, System Design using IP Integrator, Embedded design for the Xilinx Zynq SOC (based on the ARM Cortex A9 dual core processor), and higher level design using Vivado High Level Synthesis. Hands-on labs using the Xilinx ZyBo Zynq development board will cover hardware design, software design for the ARM Cortex A9, custom IP, hardware and software debugging, creation of hardware accelerators using Vivado high level synthesis.

More info: http://www.xilinx.com/university/workshops/workshop-schedule.htm

Intel Workshop

Experimenting with electronics using Arduino is fun, but what if you need more software and networking capabilities ? There's a board for that : the Intel Galileo. It's an Intel based linux PC with analogic and digital IO, plus USB and other typical PC ports. During this workshop, we'll see how to code for Internet of Things using Intel Galileo. Any linux compatible language can be used. We'll also brainstorm to find the best IoT project ideas. Should you want to see the technical details and get ready, Open Source Courseware can be found at : http://intel-software-academic-program.com/pages/courses#iot

Speaker bio: Trained as a biologist, Paul Guermonprez worked for 8 years in the biotech field as a software developer and bioinformatician. He then joined Intel Software as an application engineer to optimize parallel software in the biotech and medical field. After 5 years, Paul took in charge the Intel Software Academic Program for the EMEA-Russia geo. The Academic program is developing technical collaborations with professors and students to make software fun and innovative. Various aspects of the program include : Hardware seeding programs, workshops, contests, mentorship. Topics covered : Internet of Things, HPC, mobile programming, perceptual computing

CHANGE Workshop

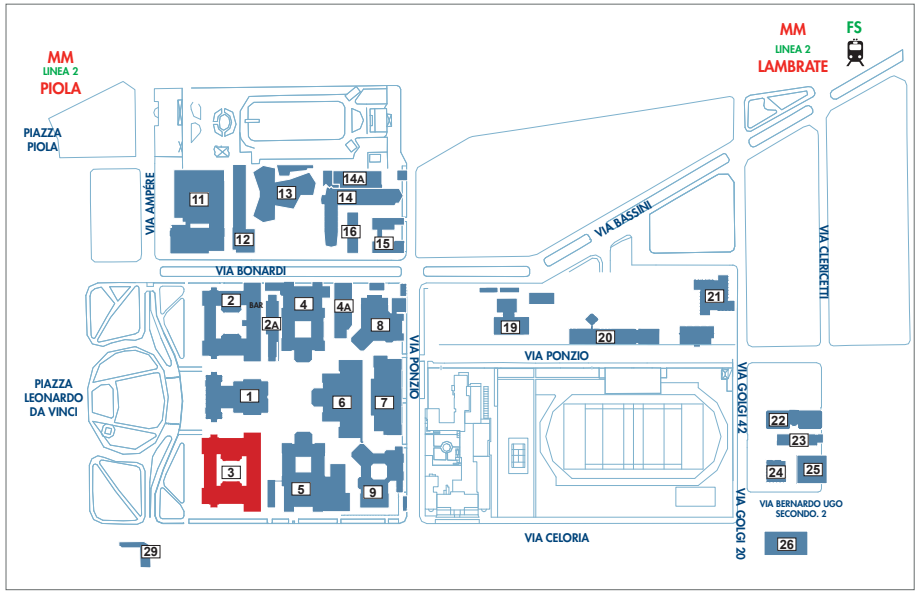
International Workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (CHA'N'GE). Its objective is to bring together researchers and industry from all over the world for a wide ranging discussion of self-aware adaptive systems, including, but not limited to: system architectures, self-aware operating systems, autonomous self-aware computer architecture, dynamic reconfiguration, applications, embedded processors, adaptive algorithm and distributed self-training algorithms, biologically inspired systems, surveys and/or prospective papers in self-aware computing systems, etc.

Tutorials

On how to efficiently exploit reconfiguration aspects from your design - The FASTER tool chain

Extending the functionality and the lifetime of products requires the addition of new functionality to track and satisfy the customer's needs and market and technology trends. While adaptability of software components is straightforward, products include hardware accelerators –for reasons of performance and power efficiency- that also need to adapt to the new requirements. Hardware solutions can achieve high performance, and software solutions can easily adapt to the new set of threats, but neither can achieve flexibility and high performance at the same time. Reconfigurable logic allows the definition of new functions to be defined in hardware units, combining hardware speed and efficiency, with ability to adapt and cope in a cost effective way with expanding functionality, changing environmental requirements, improvements in system features, changing protocols and data-coding standards, etc. However, designing, implementing and verifying reconfigurable hardware systems is harder compared to

Conference venue
Politecnico di Milano
P.za Leonardo da Vinci 32,
Building 3
20133 Milano



Public transports in Milano
The public transportation system within the city of Milano is run by ATM (Azienda Trasporti Milanesi). It consists of buses, cable cars (TRAM) and subway (METRO).

By visiting the **ATM website** you can create personalized itineraries.
www.atm.it/en

A urban network ticket costs € 1, 50 and it is valid for 75 minutes on all lines but it can not be used twice on the subway

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Ulf Witkowski,
South Westphalia University, Germany

at the University of California, Irvine. He received a PhD from the University of Illinois at Urbana-Champaign (1989). His research interests are in embedded systems design automation, computer architecture, optimizing compilers, system specification techniques, distributed embedded systems, and brain-inspired architectures and computing. He has received numerous best paper awards and is coauthor of 7 books. Professor Dutt served as EiC of ACM TODAES (2003-2008) and as AE for ACM TECS and IEEE TVLSI. He has served on the steering, organizing, and program committees of several premier CAD and Embedded System Design conferences and workshops, and serves or has served on the advisory boards of ACM SIGBED, ACM SIGDA, ACM TECS and IEEE ESL. Professor Dutt is a Fellow of the IEEE, an ACM Distinguished Scientist, and recipient of the IFIP Silver Core Award.

Dealing with a World of Data: A Systems Perspective

H. Peter Hofstee
IBM Austin Research Laboratory
Abstract - Increasingly Big Data computing is being applied to some of the world's most difficult, most urgent problems. This talk will describe the nature of Big Data computing and present technology that has been developed to allow Big Data computing systems to address these challenges. We discuss the design of systems for Big Data and their corresponding middleware and look at how both of these might evolve and challenge the current thinking about Big Data systems. Finally we motivate shared-memory heterogeneous architectures in this context and we discuss the coherent attach processor interface on Power 8 as a concrete example of how to achieve a system-level benefit.

Short bio - H. Peter Hofstee currently works at the IBM Austin Research Laboratory on workload-optimized and hybrid systems. Peter has degrees in theoretical physics (MS, Rijks Universiteit Groningen, Netherlands) and computer science (PhD, California Inst. of Technology). At IBM Peter has worked on microprocessors, including the first CMOS processor to demonstrate GHz operation (1997), and he was the chief architect of the synergistic processor elements in the Cell Broadband Engine, known from its use in the Sony Playstation 3 and the Roadrunner supercomputer that first broke the 1 Petaflop Linpack benchmark. His interests include VLSI, multicore and heterogeneous microprocessor architecture, security, system design and programming. Peter is an IBM master inventor with over 100 patents.

On how to design smart energy-efficient buildings

Donatella Sciuto
Politecnico di Milano
Abstract - Smart spaces are environments such as apartments, offices, museums, hospitals, schools, malls, university campuses, and outdoor areas that are enabled for the cooperation of objects (e.g., sensors, devices, appliances) and systems that have the capability to self-organize themselves, based on given policies. Since they can be used for an efficient management of the energy consumption of buildings, there is a growing interest for them, both in academia and industry. Unfortunately, nowadays, these systems are still designed manually with ad-hoc solutions. As a consequence, a huge effort has to be spent for each new smart building. Within this context, aim of this work is to propose a methodology to automate the design process of such smart spaces. The paper presents an overview of the design flow implemented to support the design of scalable architectures for energy aware smart spaces.

Short bio - Donatella Sciuto received her Laurea in Electronic Engineering from Politecnico di Milano and her PhD in Electrical and Computer Engineering from the University of Colorado, Boulder. She is currently Vice Rector of the Politecnico di Milano and Full Professor in Computer Science and Engineering. She is in the Board of Governors of the Bank of Italy. Her main research interests cover the methodologies for the design of embedded systems and multicore systems, from the specification level down to the implementation of both the hardware and software components, including reconfigurable and adaptive systems. She has published over 200 scientific papers. She is a Fellow of IEEE and has been President of the IEEE Council of Electronic Design Automation for the past two years. She has been in the executive and program committees of different conferences and journals in the area of Electronic Design Automation.

Keynotes

Real-time Graph Exploration on Large-scale Distributed Memory Machines

Fabrizio Petrini
IBM TJ Watson Research Center
Abstract - The trend of "big data growth" presents enormous challenges, but it also presents incredible scientific and business opportunities. Together with the data explosion, we are also witnessing a dramatic increase in data processing capabilities, thanks to new powerful parallel computer architectures and more sophisticated algorithms. In this talk we describe the algorithmic design and the optimization techniques that led to the unprecedented processing rate of 15.3 trillion edges per second on 64 thousand BlueGene/Q nodes, that allowed the in-memory exploration of a petabyte-scale graph in just a few seconds. We believe that these techniques can be successfully applied to a broader class of graph algorithms.

Short bio - Fabrizio Petrini is the manager of the High Performance Analytics Department of the IBM TJ Watson Research Laboratory. His research interests include various aspects of multi-core processors and supercomputers, including high-performance interconnection networks, network interfaces, fault tolerance, and data-intensive computing algorithms for mining large data sets. He is the recipient of numerous awards for DOE, IEEE and ACM, including best paper awards from the international conference on supercomputing (SC 2003), the international supercomputing conference (ISC 2009), and the international parallel and distributed processing symposium (IPDPS 2003 and 2014).

Internet of Things : From hacking to industrialization

Paul Guermonprez
Intel Corporation
Abstract - Hobbyists have been playing with internet of things for years. They hack existing devices or 3D print their own and connect them via internet. As IoT demand is increasing, we need to find proper tools and methods to develop high quality IoT products, while maintaining the creativity of the hobbyist. The Intel Software Academic Program is working with universities to help and develop innovative student projects. We'll see what methods they use and results they achieve. Short bio - After 8 years in the biotech field, Paul Guermonprez joined Intel to optimize parallel software. He is now developing technical collaboration with universities all over Europe, Middle East, Africa and Russia

Towards Sentient Chips: Self-Awareness through On-Chip Sensemaking

Nikil Dutt
Center for Embedded Computer Systems (CECS)
Abstract - While the notion of self-awareness has a long history in biology, psychology, medicine, engineering and (more recently) computing, we are seeing the emerging need for self-awareness in the context of complex many-core chips that must address the (often conflicting) challenges of resiliency, energy, heat, cost, performance, security, etc. in the face of highly dynamic operational behaviors and environmental conditions. In this talk I will present the concept of CyberPhysical-Systems-on-Chip (CPSoC), a new class of sensor-actuator rich many-core computing platforms that intrinsically couples on-chip and cross-layer sensing and actuation to enable self-awareness. Unlike traditional MultiProcessor Systems-on-Chip (MPSoCs), CPSoC is distinguished by an intelligent co-design of the control, communication, and computing system that interacts with the physical environment in real-time in order to modify the system's behavior so as to adaptively achieve desired objectives and Quality-of-Service (QoS). The CPSoC design paradigm enables self-awareness (i.e., the ability of the system to observe its own internal and external behaviors such that it is capable of making judicious decision) and (opportunistic) adaptation using the concept of cross-layer physical and virtual sensing and actuations applied across different layers of the hardware/software system stack. The closed loop control used for adaptation to dynamic variation -- commonly known as the observe-decide-act (ODA) loop -- is implemented using an adaptive, reflexive middleware layer. The learning abilities of CPSoC provide a unified interface API for sensor and actuator fusion along with the ability to improve autonomy in system management. The CPSoC paradigm is the first step towards a holistic software/hardware effort to make complex chips "sentient".

Short bio - Nikil Dutt is a Chancellor's Professor of CS, Cognitive Sciences, and EECS

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  Donatella Sciuto, Politecnico di Milano, Italy
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  Aurelio Morales, Universidad Nacional de Ingenieria, Peru

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  Florian Letombe, Synopsys, France
  Sanghamitra Roy, Utah State University, USA
  Pablo Sanchez, Universidad de Cantabria, Spain
  Alper Sen, Bogazici University, Turkey
  Francesco Stefanni, University of Verona, Italy
  Eli Bozorgzadeh, University of California, USA

- **Self-adaptive and reconfigurable computing**

  Fabio Campi, Simon Fraser University, Canada
  João Cardoso, University of Porto, Portugal
  Apostolas Dollas, Technical University of Crete, Greece
  Dietmar Fey, University of Erlangen-Nuremberg, Germany
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  Jim Torresen, University of Oslo, Norway
  Pedro Trancoso, University of Cyprus, Cyprus
  Steve Wilton, UBC, Canada

- **Applications for Embedded and Ubiquitous Computing**

  Luc Bouganim, INRIA, France
  Stefan Henkler, OFFIS, Germany
  Xenofon Koutsoukos, Vanderbilt Univ., Canada
  Dimosthenis Kyriazis, National Tech. Univ. of Athens, Greece
  José Rufino, Univ. of Lisboa, Portugal
  Eric Senn, Univ. of South Brittany, France
  Frank Singhoff, Univ. of Western Brittany, France
  Oleg Sokolsky, Univ. of Pennsylvania, USA
  Frank Sill Torres, Univ. Federal Minas Gerais, Brasil
  Paul Townend, Univ. of Leeds, United Kingdom

Present and Future directions in the Reconfigurable Computing Domain

Nuno Paulino, Jo‹o Canas Ferreira, and Jo‹o M. P. Cardoso. Trace-Based Reconfigurable Acceleration with Data Cache and External Memory Support

Benedikt Janssen, Jones Yudi Mori Alves Da Silva, Osvaldo Navarro, Diana Goehringer, Michael Huebner. Future Trends on Adaptive Processing Systems

Max Tottenham, Paul Grigoras, Gabriel Coutinho and Wayne Luk. Elastic management of reconfigurable accelerators

Fault tolerance and simulation in the multicore era

Lars Schor, Iuliana Bacivarov, Luis Gabriel Murillo, Pier Stanislao Paolucci, Frederic Rousseau, Ashraf El Antably, Robert Buecs, Nicolas Fournel, Rainer Leupers, Devendra Rai, Lothar Thiele, Laura Tosoratto, Piero Vicini, and Jan Weinstock. EURETILE Design Flow: Dynamic and Fault Tolerant Mapping of Multiple Applications onto Many-Tile Systems

Thomas Bruckschloegl, Oliver Oey, Michael Rueckauer, Timo Stripf and Juergen Becker. A Hierarchical Architecture Description for Flexible Multicore System Simulation

Dimitris Theodoropoulos, Dionisios Pnevmatikatos, Stavros Tzilis, Ioannis Sourdis. The DeSyRe Runtime support for Fault-tolerant Embedded MPSoCs

POSTER SESSION

41. Fernando Adolfo Escobar Juzga, Jimmy Fernando Tarrillo, Xin Chang and Carlos Valderrama. Hardware Managers with File System Support for Faster Dynamic Partial Reconfiguration

28. Elena Baralis, Luca Cagliero, Tania Cerquitelli, Silvia Chiusano, Paolo Garza, Luigi Grimaudo and Fabio Pulvirenti. Misleading generalized itemset mining in the cloud

29. Ying Liu, Vamis Xhagjika, Vladimir Vlassov and Ahmad Al-Shishtawy. BwMan: Bandwidth Manager for Elastic Services in the Cloud

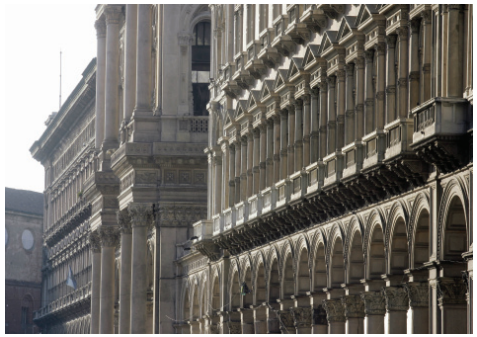
36. Jean-Claude Charr, Rapha'l Couturier, Ahmed Fanfakh and Arnaud Giersch. Dynamic Frequency Scaling for Energy Consumption Reduction in Distributed MPI Programs

43. Hovhannes Harutyunyan and Ankit Malani. Efficient Multicast Algorithms for Mesh and Torus Networks

13. Beilei Sun, Xi Li, Zhu Zongwei, Chao Wang and Xuehai Zhou. Kernel-User Space Separation in DRAM Memory

24. Pawan Kumar. Multi-threaded Direction Preserving Preconditioners

25. Qi Zhong and Jing Wang. Object-centric Bank Partition for Reducing Memory Interference in CMP Systems



39. Alberto Scolari, Filippo Sironi, Donatella Sciuto and Marco Domenico Santambrogio. A Survey on Recent Hardware and Software-Level Cache Management Techniques

5. Akiyoshi Wakatani. GPGPU Implementation of Nearest Neighbor Search with Product Quantization

9. Xia Liu, Fangfei Yu and Ligang Sun. Image Edge Detection Based on Contourlet Transform Combined With the Model of Anisotropic Receptive Fields

ISPA Sessions

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44. Alejandro Chac—n, Santiago Marco-Sola, Antonio Espinosa, Paolo Ribeca and Juan Carlos Moure. FM-index on GPU: a cooperative scheme to reduce memory footprint

6. Sandra Catalan, Jorge González-Domínguez, Rafael Mayo Gual and Enrique S. Quintana-Orti. Analyzing the Energy Efficiency of the Memory Subsystem in Multicore Processors

47. Shuichi Oikawa. Virtualizing Storage as Memory for High Performance Storage Access

15. Filippo Seracini, Xiang Zhang, Tajana Rosing and Ingolf Krueger. A Proactive Customer-Aware Resource Allocation Approach for Data Centers

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19. Pawel Gepner, Victor Gamayunov, Wieslawa Litke, Ludovic Sauge and Cyril Mazauric. Evaluation of Intel Xeon E5-2600v2 based cluster for Technical Computing workloads

22. David Apar'cio, Pedro Ribeiro and Fernando Silva. Parallel Subgraph Counting for Multicore Architectures

42. Jiri Dokulil and Siegfried Benkner. Automatic tuning of a parallel pattern library for heterogeneous systems with Intel Xeon Phi

18. Leisheng Li, Yingrui Wang, Zhitao Ma and Rong Tian. petaPar: A Scalable Petascale Framework for Meshfree/Particle Simulations

Applications

2. Hakim Mabed and Julien Bourgeois. A Shape-Shifting Distributed Meta-Algorithm for Modular Robots

31. Songbin Liu, Xiaomeng Huang, Yufang Ni, Haohuan Fu and Guangwen Yang. A high performance compression method for climate data

27. Jianhang Huang, Weiguo Wu and Qian Li. A Utility-Maximizing Tasks Assignment Method for Rendering Cluster System

35. Alessandro A. Nacci, Vincenzo Rana, Donatella Sciuto and Marco D. Santambrogio. An open-source, efficient and parameterizable hardware implementation of the AES algorithm

Cloud, social netoworks and service oriented architectures

8. Xiao Chen, Chengyin Liu and Cong Liu.E Efficient Routing Algorithms Combining History and Social Predictors in Mobile Social Networks

45. Altino Sampaio and Jorge Barbosa. Estimating Effective Slowdown of Tasks in Energy-Aware Clouds

14. Anna Kobusinska, Mateusz Holenko, Piotr Zierhoffer and Dariusz Wawrzyniak. The impact of service semantics on the consistent recovery in SOA

33. Daniele Buono, Tiziano De Matteis and Gabriele Mencagli. A High-Throughput and Low-Latency Parallelization of Window-based Stream Joins on Multicores

Runtime management and resource optimization in heterogeneous computing systems

Davide Gadioli, Simone Libutti, Giuseppe Massari, Edoardo Paone, Michele Scandale, Patrick Bellasi, Gianluca Palermo, Vittorio Zaccaria, Giovanni Agosta, William Fornaciari, Cristina Silvano. OpenCL Application Auto-Tuning and Run-Time Resource Management for Multi-Core Platforms

F. Spada, A. Scolari, G. C. Durelli, R. Cattaneo, D. N. Pnevmatikatos, G. N. Gaydadjiev, O. Pell, A. Brokalakis, W. Luk, D. Pau, D. Stroobandt, D. Sciuto, M. D. Santambrogio FPGA-based design using the FASTER toolchain: the case of STM Spear development board

Gianluca C. Durelli, Marcello Pogliani, Antonio Miele, Antonios Motakis, Christian Plessl, Heinrich Riebler, Marco D. Santambrogio, Gavin Vaz, Cristiana Bolchini. Runtime Resource Management in Heterogeneous System Architectures: the SAVE Approach

Eoghan O'Neill, John McGlone, J.G.F Coutinho, Andrew Doole, Carmelo Ragusa, O. Pell, P. Sanders. Cross Resource Optimisation of Database Functionality Across Heterogeneous Processors

- **Smart mobile systems and Social Media**

Reinhard Keil, UPB, Germany
Mischa van Oijen, Atos, Netherlands
Zhiwen Yu, NWPU, China
Florian Mueller, RMIT, Australia
Hong Lu, Intel, USA
Yin Zhu, HKUST, Hong Kong, China
Yu Zheng, MSRA, China
James She, Hong Kong University of Science and Technology, Hong Kong, China
Markus Holtmanns, NVIDIA, Finland

- **Power-Aware Computing**

Philipp Hartmann, OFFIS, Germany
Eugenio Villar, University of Cantabria, Spain
Sotirios Xydis, NTUA, Greece
Massimo Poncino, Politecnico di Torino, Italy
Morteza Biglari-Abhari, University of Auckland, New Zealand
Leandro Fiorin, IBM-NL, Netherland
Gang Quan, Florida International University, USA
Snorre Aunet, Norwegian University of Science and Technology, Norway
Nikos Bellas, University of Thessaly, Greece
Maryline Chetto, IUT de Nantes - IRCCyN Research Institute, France

- **Security for Distributed Systems**

Liang Zhenkai, National University of Singapore, Singapore
Johannes Kinder, Royal Holloway University of London, United Kingdom
Andrea Lanzi, Università degli Studi di Milano, Italy
Aristide Fattori, Università degli Studi di Milano, Italy
Corrado Leita, Symantec Research, Ireland
Nick Nikiforakis, KU Leuven, The Netherlands
Asia Slowinska, Vrije Universiteit Amsterdam, The Netherlands
Michalis Polychronakis, Columbia University, USA
Christian Platzer, TU Wien, Austria
Konrad Rieck, University of Göttingen, Germany

- **Fault Tolerance and Reliability / Dependability**

Osman Unsal, BSC, Spain
Yanos Sazeides, University of Cyprus, Cyprus
Dimitrios Gizopoulos, University of Athens, Greece
Theo Ungerer, University of Ausburg, Germany
Luigi Carro, Federal University of Rio Grande do Sul, Brazil
Cristiana Bolchini, Politecnico di Milano, Italy
Matteo Sonza Reorda, Politecnico di Torino, Italy
Giorgio di Natale, LIRMM, France
Fabrizio Lombardi, Northeastern University, USA
Rishad Shafik, University of Southampton, United Kingdom

- **Distributed systems and smart sensing**

Marian Verhelst, KU Leuven, Belgium
Jose M. Moya, Technical University of Madrid, Spain
Riku Jantti, Aalto University, Finland
Jose L. Rojo, King Juan Carlos University, Spain
Monica Vallejo, National University of Colombia, Colombia
Joaquin Sitte, Queensland University of Technology, Australia
Naoyuki Kubota, Tokyo Metropolitan University, Japan
Jong-Hwan Kim, KAIST, Republic of Korea
Jacques Penders, Sheffield Hallam University, United Kingdom
Gurvinder S. Virk, University of Gävle, Sweden

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Center for Advanced Computational Technologies of the National Nanotechnology Laboratory and the University of Salento, Italy

Edgar Gabriel,

Sotirios Ziavras,
New Jersey Institute of Technology

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Ronald Petrlic,
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Amiya Nayak,
University of Ottawa

Kamesh Madduri,
The Pennsylvania State University

Martine Wedlake,
IBM

Suren Byna,
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Stefano Chessa,
Department of Computer Science, University of Pisa

Ruay-Shiung Chang,
National Dong Hwa University

Subhash Saini,
NASA

Oliver Theel,
Carl von Ossietzky University of Oldenburg, Germany

Rodolfo Azevedo,
University of Campinas

HPC applications

331. Antonios Motakis, Alvise Rigo Platform device assignment to KVM-on-ARM Virtual Machines via VFIO

Future Airborne WSN
S. Capone, R. Brama, N. Accettura, D. Striccoli, G. Boggia. An Energy Efficient and Reliable Composite Metric for RPL Organized Networks

L. Francioso, C. De Pascali, E. Pescini, M. G. De Giorgi, A. Ficarella, P. Siciliano. Aircraft distributed flow turbulence sensor network with embedded flow control actuators

Francesco Bandiera, Angelo Coluccia, Giuseppe Ricci, Fabio Ricciato, Danilo Spano. TDOA localization in asynchronous WSN

R. Brama, P. Tundo, S.Capone, V. Giampa, L. Francioso, C. De Pascali, M.G. De Giorgi, S. Campilongo, A. Malvasi. Investigating Flows Dynamics with Wireless Pressure Sensors Network

Smart Homes and Buildings Energy Management
Alessandro A. Nacci, V. Rana, D. Sciuto. A Perspective Vision on Complex Residential Building Management Systems

Edoardo Patti, Andrea Acquaviva, Vittorio Verda, Dario Martellacci, Enrico Macii. Towards a software infrastructure for district energy management

Mario Caruso, Adriano Cerocchi. On the black-box stand-by recognition strategies in smart home environments

Marcel Mathis, Aliaksei Andrushevich, Andreas Rumsch, Alexander Klapproth. Improving the recognition performance of NIALM algorithms through technical labeling

Smart and distributed embedded systems
17. Paulo Pires, Everton Cavalcante, Thomaz Barros, Flavia Delicato, Thais Batista and Bruno Costa. A Platform for Integrating Physical Devices in the Internet of Things

22. Hanshang Li, Ling Wang, Shuo Pang and Massood Towhidnejad. A Cross-Layer Design for Data Collecting of the UAV-Wireless Sensor Network System

53. Monica A Vallejo, Jose L Ayala and Joaquin Recas. A Link Quality Estimator for Power-Efficient Communication over On-Body Channels

11. Xiao Chen, Zhen Jiang, Kaiqi Xiong and Jian Shen. Practical Routing Protocol for Impromptu Mobile Social Networks

Mobile Devices
Ruben Braojos, Ivan Beretta, Jeremy Constantin, Andreas Burg, David Atienza. A Wireless Body Sensor Network For Activity Monitoring With Low Transmission Overhead

M. Ferroni, A. Cazzola, F. Trov˜, D. Sciuto, M. D. Santambrogio. On Power and Energy Consumption Modeling for Smart Mobile Devices

Pietro Mercati, Andrea Bartolini, Francesco Paterna, Luca Benini, Tajana Simunic Rosing. An On-line Reliability Emulation Framework

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6. Huseyin Yigitler, Riku Jantti and Reino Virrankoski. pRoot: An Adaptable Wireless Sensor-Actuator Hardware Platform

14. Jean-Christophe Morgre, Jean-Philippe Diguet and Johann Laurent. Mobile Augmented Reality System for marine navigation assistance

15. Florian Adamsky, Syed Ali Khayam, Rudolf JŠger and Muttukrishnan Rajarajan. Who is going to be the next BitTorrent Peer Idol?

16. Aicha Ben Salem, Seifeddine Bouallegue and Kaouther Sethom. A QoS based Resource Allocation in Femtocell Networks

36. Vincenzo Rana, Francesco Bruschi, Marco Paolieri, Donatella Sciuto and Marco Domenico Santambrogio. On How to Efficiently Implement Regular Expression Matching on FPGA-based Systems

45. Taha Abdelmoutaleb Cherfia, Kamel Barkaoui and Fa•za Belala. A BRS-Based Modeling Approach for Context-Aware Systems: A Case Study of Smart Car System

46. Ali El Attar, Rida Khatoun and Marc Lemercier. Trimming Approach of Robust Clustering for Smartphone Behavioral Analysis

48. Essayas Woldu, Mingkun Yang, Gustav Cedersjš, Zain Ul-Abdin, Jorn W Janneck, Veronica Gaspes and Bertil Svensson. Realizing Efficient Execution of Dataflow Actors on Manycores

51. Yu Sun and Wei Zhang. Improve Energy Efficiency with Dynamic Compiler-Directed Function Unit Power Control

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18. Ioannis Christoforakis and George Kornaros. Runtime Adaptation of Embedded Tasks with a-priori Known Timing Behavior Utilizing On-line Partner-Core Monitoring and Recovery

33. Boris HŸbener, Gregor Sievers, Thorsten Jungeblut, Mario Porrmann and Ulrich RŸckert. CoreVA: A Configurable Resource-efficient VLIW Processor Architecture

49. Mohamad Hammam Alsafrjalani and Ann Gordon-Ross. Dynamic Scheduling for Reduced Energy in Configuration-Subsetted Heterogeneous Multicore Systems

19. Mehrdad Bagheri and Gert Jervan. Fault-tolerant scheduling of mixed-critical applications on multi-processor platforms

Resource- and Context-Aware Methods for Efficient Execution of Embedded and Ubiquitous Software Systems
39. Matteo Ferroni, Andrea Damiani, Alessandro A. Nacci, Donatella Sciuto and Marco Domenico Santambrogio. cODA: An Open-Source Framework to Easily Design Context-Aware Android Apps

12. Laurent Lemarchand, Isaac Armah-Mensah and Jean-Philippe Babau. Dynamic Server Configuration for Multiple Streaming in a Home Network

55. Sangsoo Park. Task-I/O Co-Scheduling for Pfair Real-Time Scheduler in Embedded Multi-Core Systems

52. Yiqiang Ding and Wei Zhang. Hop-based Priority Scheduling to Improve Worst-Case Inter-Core Communication Latency

Mechanisms and Design Technologies for Future Embedded and Ubiquitous Software Systems
21. Yi Zhang, Nan Guan and Wang Yi. Understanding the Dynamic Caches on Intel Processors: Methods and Applications

24. Mohamad Hammam Alsafrjalani, Pablo Viana and Ann Gordon-Ross. Minimum Effort Design Space Subsetting for Configurable Caches

41. Kiril Georgiev and Vania Marangozova-Martin. MPSoC Zoom Debugging: A Deterministic Record-Partial Replay Approach

27. Ferry Pramudianto, Beatriz Avila, Prof. Dr.Mathias Jarke and Marco Jahn. Extending Semantic Device Discovery with Synonym of Terms

Applications of Ubiquitous Embedded Systems
7. Yuyan Sun, Xinyun Zhou, Limin Sun and Shuixian Chen. Vehicle activity analysis based on ANPR system

29. Vlado Altmann, Jan Skodzik, Peter Danielis, Johannes Mueller, Frank Golatowski and Dirk Timmermann. A DHT-based Scalable Approach for Device and Service Discovery

43. Hai Nam Tran, Frank Singhoff, StŽphane Rubini and Jalil Boukhobza. Instruction cache in hard real-time systems: modeling and integration in scheduling analysis tools with AADL

37. Arash Vahidi. The monotonic separation kernel

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Blair Fort, Andrew Canis, Jongsok Choi, Nazanin Calagar, Ruolong Lian, Stefan Hadjis, Yu Ting Chen, Mathew Hall, Bain Syrowik, Tomasz Czajkowski, Stephen Brown, Jason Anderson. Automating the Design of Processor/Accelerator Embedded Systems with LegUp High-Level Synthesis

Paolo Burgio, Andrea Marongiu, Philippe Coussy and Luca Benini. A HLS-based toolflow to design next-generation heterogeneous many-core platforms with shared memory

Razvan Nane, Vlad-Mihai Sima, Cuong Pham-Cuoq, Fernando Goncalves, Koen Bertels. High-Level Synthesis in the Delft Workbench Hardware/Software Co-design Tool-Chain

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329. Yves Lhuillier, Jean-Marc Philippe, Alexandre Guerre, Michał Kierzynka, Ariel Oleksiak Parallel architecture benchmarking: from embedded computing to HPC, a FiPS project perspective

330. Patrick Knocke, Ralph Gšrgen, Jšrg Walter, Domenik Helms, Wolfgang Nebel Using early power and timing estimations of massively heterogeneous computation platforms to create optimized

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Etienne Rivière,
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Edson Borin ,
University of Campinas

Xiaofang Wang,
Department of Electrical and Computer Engineering at Villanova University

Tania Cerquitelli,
Politecnico di Torino

Rafael Santos,
National Institute for Space Research

Conference Program

Monday, 25 August:
Workshops/Tutorials

09:00 Intel Hackathon
09:00 Workshop Empatica
12:30 Lunch
13:30 Workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments
18:00 Cheese and wine

Tuesday, 26 August:
ISPA and EUC

08:30 Welcome message
09:00 Keynote - Peter Hofstee, IBM Research Austin: "Dealing with a World of Data: A Systems Perspective"
10:00 EUC: Hardware Solutions for Embedded and Ubiquitous Systems
10:00 ISPA: Resource Allocation
12:00 Lunch
13:15 Keynote - Paul Guermonprez, Intel: "Internet of Things : From hacking to industrialization"
14:15 EUC: Resource- and Context-Aware Methods for Efficient Execution of Embedded and Ubiquitous Software Systems
14:15 ISPA: Parallel Workloads
16:15 Coffee break
16:45 EUC: Mechanisms and Design Technologies for Future Embedded and Ubiquitous Software Systems
16:45 ISPA: Applications
20:00 Cenacolo

Wednesday, 27 August:
ISPA and EUC

09:00 Keynote - Fabrizio Petrini, IBM T. J. Watson: "Real-time Graph Exploration on Large-scale Distributed Memory Machines"
10:00 EUC: Applications of Ubiquitous Embedded Systems
10:00 ISPA: Cloud, Social, Netowrks and Service Oriented Architectures
12:00 Lunch
13:00 Keynote - Nikil Dutt, UCI: "Towards Sentient Chips: Self-Awareness through On-Chip Sensemaking"
14:00 ISPA: Poster Session
14:45 EUC: High Level Synthesis (SS)
16:15 Coffee break
16:45 EUC: Hardware and Design Methodologies for Heterogeneous Compute Clusters (SS)
16:45 ISPA: Runtime management and resource optimization in heterogeneous computing systems (SS)
20:00 Social Event

Thursday, 28 August:
ISPA and EUC

08:45 Keynote - Donatella Sciuto, Politecnico di Milano: "Designing smart energy-efficient buildings"
09:45 EUC: Future Airborne WSN (SS)
09:45 EUC: Smart Homes and Buildings Energy Management (SS)
12:15 Lunch
13:30 Xilinx Workshop: Embedded System Design Flow on Zynq using Vivado
13:30 EUC: Poster Session
14:15 EUC: Smart and distributed embedded systems
14:15 ISPA: Present and Future directions in the Reconfigurable Computing Domain (SS)
16:15 Coffee break
16:45 EUC: Mobile Devices (SS)
16:45 ISPA: Fault tolerance and simulation in the multicore era (SS)
18:15 Closing remarks

Friday, 29 August:
Workshops/Tutorials

08:30 Tutorial: Hands-On ILDJIT 2.0 for Static and Dynamic Program Analysis and Transformation
08:30 Xilinx Workshop (cont.): Embedded System Design Flow on Zynq using Vivado
10:30 Coffee break
12:30 Lunch
13:30 Tutorial: On how to efficiently exploit reconfiguration aspects from your design - The FASTER tool chain
16:00 Coffee break

Social Program

Three different social events will be held at the P2CWeek event.

- Cheese and Wine Dinner
- Visit to Leonardo's Last Supper
- Social Dinner at Palazzo Gireconsulti

More information can be found below:

Aug. 25, 2010 - Cheese and Wine Dinner
h. 18:00 - 19:30
A typical italian food dinner, to exchanges opinions and ideas in an international environment.

Aug. 26, 2010 - Visit to Leonardo's Last Supper
h. 19:30 - 23:00
The Last Supper (Italian: Il Cenacolo or L'Ultima Cena) is a late 15th-century mural painting by Leonardo da Vinci in the refectory of the Convent of Santa Maria delle Grazie, Milan. It is one of the world's most famous paintings, and one of the most studied, scrutinized, and satirized. (http://en.wikipedia.org/wiki/The_Last_Supper_%28Leonardo_da_Vinci%29).

The visit is organized for groups and the visit lasts 20 minutes, approximately. The group composition will be provided at the conference information desk in Milan.

English-speaking guides will be available.
http://www.milanoarte.net/beauties-you-cannot-miss/last-supper-and-santa-maria-delle-grazie

Aug. 27, 2010 - Social dinner at Palazzo Gireconsulti
h. 20:00 - 23:00
A social dinner at Palazzo Gireconsulti (http://www.palazzogiureconsulti.it/), one of the fundamental features of Piazza dei Mercanti, topographical centre of Medieval Milan and heart of the economic and social life of those times.

Contents

P2Cweek: ISPA & EUC

About P2C

Parallel and Pervasive Week (P2CWeek) is a premier event covering very important aspects of computing systems. By bringing together two international conferences (EUC and ISPA), and several workshops, P2CWeek allows attendees to benefit from a wide range of topics covering the state of the art in computing systems and architectures research and development.
The P2C week will be held in Milan from Monday 25 August to Friday 29 August 2014.

One registration, two conferences and workshops

Registered attendees will be allowed to attend sessions in the other conference and tutorials for free: EUC 2014, ISPA 2014. Please note that symposia and workshops may require separate registration.

Welcome to EUC

Embedded and ubiquitous computing is an exciting paradigm that promises to provide computing and communication services to the end users all the time and everywhere. Its systems are now invading in every aspect of our daily life and promise to revolutionize our life much more profoundly than elevators, electric motors or even personal computer evolution ever did. The emergence of this technology is a natural outcome of research and technological advances in a variety of areas including embedded systems, pervasive computing and communications, wireless networks, mobile computing, distributed computing and agent technologies.
EUC 2014 is the next event, in a series of highly successful International Conferences on embedded and Ubiquitous Computing (EUC), previously held as ICDCS-ECS04 (Tokyo, Japan, March 2004), EUC-04 (Aizu, Japan, August 2004), EUC-05 (Nagasaki, Japan, December 2005), EUC-06 (Seoul, Korea, August 2006), EUC-07 (Taipei, Taiwan, December 2007), EUC-08 (Shanghai, China, December 2008), EUC-09 (Vancouver, Canada, August 2009), EUC-10 (Hong Kong,China, December 2010), EUC-11 (Melbourne, Australia, October 2011), EUC-12 (Paphos, Cyprus, December 2012) and EUC-13 (Zhangjiajie, China, November 2013).

EUC 2014 will take place in Milan, Italy and it is part of the **P2CWeek 2014** (Parallel and Pervasive Computing Week) event. The conference will be held from 26 August 2014 to 28 August 2014.

Welcome to ISPA

ISPA-14 (12th IEEE International Symposium on Parallel and Distributed Processing with Applications) is a forum for leading work on parallel and distributed computing and networking, including architecture, compilers, runtime systems, applications, reliability, security, parallel programming models and much more. During the symposium, scientists and engineers in both academia and industry are invited to present their work on concurrent and parallel systems (multicore, multithreaded, heterogeneous, clustered systems, distributed systems, grids, clouds, and large scale machines).
The 12th ISPA follows the tradition of previous successful ISPA conferences, ISPA-03 (Aizu, Japan), ISPA-04 (Hong Kong), ISPA-05 (Nanjing, China), ISPA-06 (Sorrento, Italy), ISPA-07 (Niagara Falls, Canada), ISPA-08 (Sydney, Australia), ISPA-09 (Chengdu, China), ISPA-10 (Taipei, Taiwan), ISPA-11 (Busan, Korea), ISPA-12 (Madrid, Spain) and ISPA-13 (Melbourne, Australia). It will feature session presentations, workshops, tutorials and keynote speeches. ISPA-14 is sponsored by IEEE Technical Committee on Scalable Computing (TCSC) and IEEE Computer Society.
The objective of ISPA-14 is to provide a forum for scientists and engineers in academia and industry to exchange and discuss their experiences, new ideas, research results, and applications about all aspects of parallel and distributed computing and networking. It will feature session presentations, workshops, tutorials **and keynote speeches.**

Venue

Milan

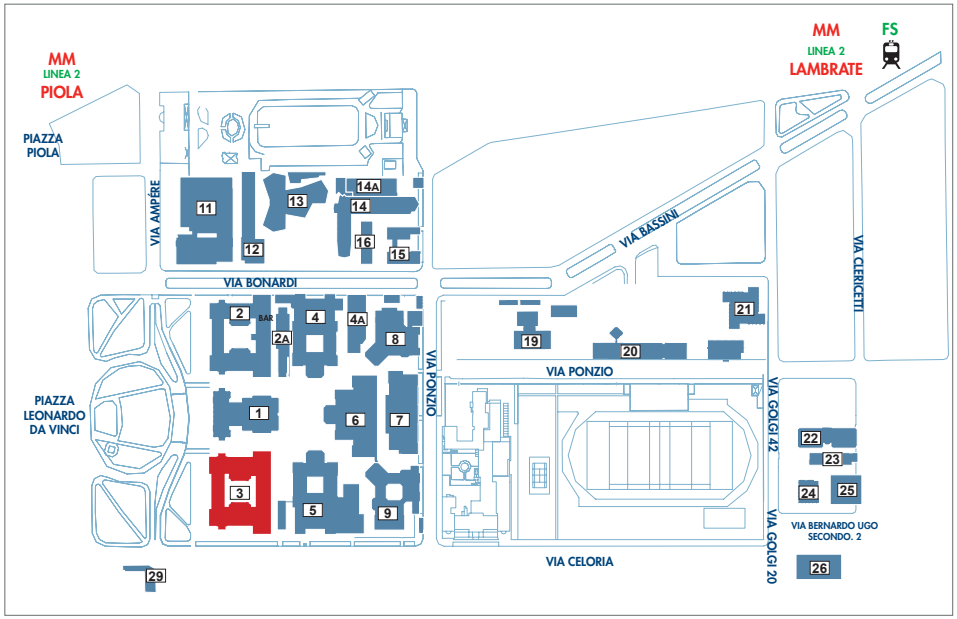
With a population of about 1.3 million, Milan, the capital of Lombardy, is located in the Po Valley, not far from the Alps with the great lakes (Lake Como, Lake Maggiore, Lake Lugano) to the North.
Milan is considered the Italian economic and finance center, with the headquarters of the Stock Exchange and of many of the most important industrial and financial businesses of the Country.
It is also the Italian symbol of fashion and design: it hosts many of the main Italian fashion maisons and international design fairs, such as "Settimana della Moda" (Milan Fashion Week) and the "Salone Internazionale del Mobile"(Milan Furniture Fair); also, a Design School operates at Politecnico di Milano.
Milan hosts the "Teatro alla Scala", considered the temple of lyrics all over the world, and several prose theatres such as the "Piccolo Teatro" founded by **Giorgio Strehler.**
In Milan are located the headquarters of the main daily newspapers (Il Corriere della Sera, Il Sole 24 Ore) and many of the main Italian publishers (Mondadori, Feltrinelli, Garzanti, Rizzoli).
The city offers to visitors the possibility to admire a wide range of monuments, museums and buildings reflecting the vestiges of history and culture left by many people who lived here. The ancient Roman remains are preserved at the Colonne di San Lorenzo, whereas the Romanesque can be admired at Sant'Ambrogio, Sant'Eustorgio or San Simpliciano Basilicas. The Duomo is one of the largest cathedrals in the world and the most important example of Gothic architecture in Italy.
The Castello Sforzesco, built on the wishes of the Duke Francesco Sforza, nowadays hosts the **Michelangelo's** "Pietà Rondanini" and several museums. The church of Santa Maria delle Grazie hosts the famous masterpiece "The Last Supper" by **Leonardo da Vinci** - declared part of the World Heritage by UNESCO.
The city has always participated actively to the National History since its origins, contributing to the purposes and the aims that led to reunification of Italy in the 18th century. Some distinguished people, who gave a significant contribution to Italian culture, lived in Milan, such as **Leonardo da Vinci** (who lived in Milan from 1482 to 1500), the poet and novelist Alessandro Manzoni, the musician **Arturo Toscanini**, the writer **Carlo Emilio Gadda**, the film director **Luchino Visconti**. Two Nobel prizes operated in Milan: **Giulio Natta** (1963, in chemistry) and **Dario Fo** (1997, in literature).
Expo 2015 is the next scheduled Universal Exposition and between May 1st and October 31st 2015 will be hosted in Milan. The Expo goal is not only to show the latest advances in technology, but also to welcome and to interpret the new challenges that human mankind faces nowadays. A theme of Expo 2015 will be "Feeding the planet, energy for life".

Politecnico di Milano

Politecnico di Milano is one of the most outstanding universities in Europe, ranked 28th in the world and 9th in Europe among technical universities, according to the QS World University Ranking – Engineering & Technology 2013. Founded in 1863, Politecnico di Milano is the largest school of architecture, design and engineering in Italy, with three main campuses located in Milan and five more branches around the Lombardy region.
Many important scientists and architects studied and taught here, among them **Achille Castiglioni**, **Gio Ponti**, **Gae Aulenti**, **Renzo Piano** and **Aldo Rossi**, both Pritzker Prize in 1990 and 1998 respectively, and Giulio Natta, Nobel Prize in Chemistry in 1963.
Research linked to didactics is a priority commitment that allows Politecnico di Milano to achieve high quality results also at an international level, developing a fruitful relationship with business and productive world by means of experimental research and technological transfer.
Politecnico takes part in several research and training projects collaborating with the most qualified European universities, together with national and international companies and institutions.

Conference venue

Politecnico di Milano
P.za Leonardo da Vinci 32,
Building 3
20133 Milano



Public transports in Milano

The public transportation system within the city of Milano is run by ATM (Azienda Trasporti Milanesi). It consists of buses, cable cars (TRAM) and subway (METRO).

By visiting the **ATM website** you can create personalized itineraries.
www.atm.it/en

A urban network ticket costs € 1, 50 and it is valid for 75 minutes on all lines but it can not be used twice on the subway

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  Paul Townend, Univ. of Leeds, United Kingdom

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  Zhiwen Yu, NWPU, China
  Florian Mueller, RMIT, Australia
  Hong Lu, Intel, USA
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Politecnico di Torino

Rafael Santos,
National Institute for Space Research

Conference Program

Monday, 25 August:
Workshops/Tutorials

09:00 Intel Hackathon
09:00 Workshop Empatica
12:30 Lunch
13:30 Workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments
18:00 Cheese and wine

Tuesday, 26 August:
ISPA and EUC

08:30 Welcome message
09:00 Keynote - Peter Hofstee, IBM Research Austin: "Dealing with a World of Data: A Systems Perspective"
10:00 EUC: Hardware Solutions for Embedded and Ubiquitous Systems
10:00 ISPA: Resource Allocation
12:00 Lunch
13:15 Keynote - Paul Guermonprez, Intel: "Internet of Things : From hacking to industrialization"
14:15 EUC: Resource- and Context-Aware Methods for Efficient Execution of Embedded and Ubiquitous Software Systems
14:15 ISPA: Parallel Workloads
16:15 Coffee break
16:45 EUC: Mechanisms and Design Technologies for Future Embedded and Ubiquitous Software Systems
16:45 ISPA: Applications
20:00 Cenacolo

Wednesday, 27 August:
ISPA and EUC

09:00 Keynote - Fabrizio Petrini, IBM T. J. Watson: "Real-time Graph Exploration on Large-scale Distributed Memory Machines"
10:00 EUC: Applications of Ubiquitous Embedded Systems
10:00 ISPA: Cloud, Social, Netowrks and Service Oriented Architectures
12:00 Lunch
13:00 Keynote - Nikil Dutt, UCI: "Towards Sentient Chips: Self-Awareness through On-Chip Sensemaking"
14:00 ISPA: Poster Session
14:45 EUC: High Level Synthesis (SS)
16:15 Coffee break
16:45 EUC: Hardware and Design Methodologies for Heterogeneous Compute Clusters (SS)
16:45 ISPA: Runtime management and resource optimization in heterogeneous computing systems (SS)
20:00 Social Event

Thursday, 28 August:
ISPA and EUC

08:45 Keynote - Donatella Sciuto, Politecnico di Milano: "Designing smart energy-efficient buildings"
09:45 EUC: Future Airborne WSN (SS)
09:45 EUC: Smart Homes and Buildings Energy Management (SS)
12:15 Lunch
13:30 Xilinx Workshop: Embedded System Design Flow on Zynq using Vivado
13:30 EUC: Poster Session
14:15 EUC: Smart and distributed embedded systems
14:15 ISPA: Present and Future directions in the Reconfigurable Computing Domain (SS)
16:15 Coffee break
16:45 EUC: Mobile Devices (SS)
16:45 ISPA: Fault tolerance and simulation in the multicore era (SS)
18:15 Closing remarks

Friday, 29 August:
Workshops/Tutorials

08:30 Tutorial: Hands-On ILDJIT 2.0 for Static and Dynamic Program Analysis and Transformation
08:30 Xilinx Workshop (cont.): Embedded System Design Flow on Zynq using Vivado
10:30 Coffee break
12:30 Lunch
13:30 Tutorial: On how to efficiently exploit reconfiguration aspects from your design - The FASTER tool chain
16:00 Coffee break

Social Program

Three different social events will be held at the P2CWeek event.

- Cheese and Wine Dinner
- Visit to Leonardo's Last Supper
- Social Dinner at Palazzo Gireconsulti

More information can be found below:

Aug. 25, 2010 - Cheese and Wine Dinner
h. 18:00 - 19:30
A typical italian food dinner, to exchanges opinions and ideas in an international environment.

Aug. 26, 2010 - Visit to Leonardo's Last Supper
h. 19:30 - 23:00
The Last Supper (Italian: Il Cenacolo or L'Ultima Cena) is a late 15th-century mural painting by Leonardo da Vinci in the refectory of the Convent of Santa Maria delle Grazie, Milan. It is one of the world's most famous paintings, and one of the most studied, scrutinized, and satirized. (http://en.wikipedia.org/wiki/The_Last_Supper_%28Leonardo_da_Vinci%29).

The visit is organized for groups and the visit lasts 20 minutes, approximately. The group composition will be provided at the conference information desk in Milan.

English-speaking guides will be available.
http://www.milanoarte.net/beauties-you-cannot-miss/last-supper-and-santa-maria-delle-grazie

Aug. 27, 2010 - Social dinner at Palazzo Gireconsulti
h. 20:00 - 23:00
A social dinner at Palazzo Gireconsulti (http://www.palazzogiureconsulti.it/), one of the fundamental features of Piazza dei Mercanti, topographical centre of Medieval Milan and heart of the economic and social life of those times.

EUC Sessions

Hardware Solutions for Embedded and Ubiquitous Systems
18. Ioannis Christoforakis and George Kornaros. Runtime Adaptation of Embedded Tasks with a-priori Known Timing Behavior Utilizing On-line Partner-Core Monitoring and Recovery

33. Boris HŸbener, Gregor Sievers, Thorsten Jungeblut, Mario Porrmann and Ulrich RŸckert. CoreVA: A Configurable Resource-efficient VLIW Processor Architecture

49. Mohamad Hammam Alsafrjalani and Ann Gordon-Ross. Dynamic Scheduling for Reduced Energy in Configuration-Subsetted Heterogeneous Multicore Systems

19. Mehrdad Bagheri and Gert Jervan. Fault-tolerant scheduling of mixed-critical applications on multi-processor platforms

Resource- and Context-Aware Methods for Efficient Execution of Embedded and Ubiquitous Software Systems
39. Matteo Ferroni, Andrea Damiani, Alessandro A. Nacci, Donatella Sciuto and Marco Domenico Santambrogio. cODA: An Open-Source Framework to Easily Design Context-Aware Android Apps

12. Laurent Lemarchand, Isaac Armah-Mensah and Jean-Philippe Babau. Dynamic Server Configuration for Multiple Streaming in a Home Network

55. Sangsoo Park. Task-I/O Co-Scheduling for Pfair Real-Time Scheduler in Embedded Multi-Core Systems

52. Yiqiang Ding and Wei Zhang. Hop-based Priority Scheduling to Improve Worst-Case Inter-Core Communication Latency

Mechanisms and Design Technologies for Future Embedded and Ubiquitous Software Systems
21. Yi Zhang, Nan Guan and Wang Yi. Understanding the Dynamic Caches on Intel Processors: Methods and Applications

24. Mohamad Hammam Alsafrjalani, Pablo Viana and Ann Gordon-Ross. Minimum Effort Design Space Subsetting for Configurable Caches

41. Kiril Georgiev and Vania Marangozova-Martin. MPSoC Zoom Debugging: A Deterministic Record-Partial Replay Approach

27. Ferry Pramudianto, Beatriz Avila, Prof. Dr.Mathias Jarke and Marco Jahn. Extending Semantic Device Discovery with Synonym of Terms

Applications of Ubiquitous Embedded Systems
7. Yuyan Sun, Xinyun Zhou, Limin Sun and Shuixian Chen. Vehicle activity analysis based on ANPR system

29. Vlado Altmann, Jan Skodzik, Peter Danielis, Johannes Mueller, Frank Golatowski and Dirk Timmermann. A DHT-based Scalable Approach for Device and Service Discovery

43. Hai Nam Tran, Frank Singhoff, StŽphane Rubini and Jalil Boukhobza. Instruction cache in hard real-time systems: modeling and integration in scheduling analysis tools with AADL

37. Arash Vahidi. The monotonic separation kernel

High Level Synthesis
Blair Fort, Andrew Canis, Jongsok Choi, Nazanin Calagar, Ruolong Lian, Stefan Hadjis, Yu Ting Chen, Mathew Hall, Bain Syrowik, Tomasz Czajkowski, Stephen Brown, Jason Anderson. Automating the Design of Processor/Accelerator Embedded Systems with LegUp High-Level Synthesis

Paolo Burgio, Andrea Marongiu, Philippe Coussy and Luca Benini. A HLS-based toolflow to design next-generation heterogeneous many-core platforms with shared memory

Razvan Nane, Vlad-Mihai Sima, Cuong Pham-Cuoq, Fernando Goncalves, Koen Bertels. High-Level Synthesis in the Delft Workbench Hardware/Software Co-design Tool-Chain

Hardware and Design Methodologies for Heterogeneous Compute Clusters
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Francesco Bandiera, Angelo Coluccia, Giuseppe Ricci, Fabio Ricciato, Danilo Spano. TDOA localization in asynchronous WSN

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15. Florian Adamsky, Syed Ali Khayam, Rudolf JŠger and Muttukrishnan Rajarajan. Who is going to be the next BitTorrent Peer Idol?

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Benedikt Janssen, Jones Yudi Mori Alves Da Silva, Osvaldo Navarro, Diana Goehringer, Michael Huebner. Future Trends on Adaptive Processing Systems

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Lars Schor, Iuliana Bacivarov, Luis Gabriel Murillo, Pier Stanislao Paolucci, Frederic Rousseau, Ashraf El Antably, Robert Buecs, Nicolas Fournel, Rainer Leupers, Devendra Rai, Lothar Thiele, Laura Tosoratto, Piero Vicini, and Jan Weinstock. EURETILE Design Flow: Dynamic and Fault Tolerant Mapping of Multiple Applications onto Many-Tile Systems

Thomas Bruckschloegl, Oliver Oey, Michael Rueckauer, Timo Stripf and Juergen Becker. A Hierarchical Architecture Description for Flexible Multicore System Simulation

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41. Fernando Adolfo Escobar Juzga, Jimmy Fernando Tarrillo, Xin Chang and Carlos Valderrama. Hardware Managers with File System Support for Faster Dynamic Partial Reconfiguration

28. Elena Baralis, Luca Cagliero, Tania Cerquitelli, Silvia Chiusano, Paolo Garza, Luigi Grimaudo and Fabio Pulvirenti. Misleading generalized itemset mining in the cloud

29. Ying Liu, Vamis Xhagjika, Vladimir Vlassov and Ahmad Al-Shishtawy. BwMan: Bandwidth Manager for Elastic Services in the Cloud

36. Jean-Claude Charr, Rapha'l Couturier, Ahmed Fanfakh and Arnaud Giersch. Dynamic Frequency Scaling for Energy Consumption Reduction in Distributed MPI Programs

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Keynotes

Real-time Graph Exploration on Large-scale Distributed Memory Machines

Fabrizio Petrini
IBM TJ Watson Research Center

Abstract - The trend of "big data growth" presents enormous challenges, but it also presents incredible scientific and business opportunities. Together with the data explosion, we are also witnessing a dramatic increase in data processing capabilities, thanks to new powerful parallel computer architectures and more sophisticated algorithms. In this talk we describe the algorithmic design and the optimization techniques that led to the unprecedented processing rate of 15.3 trillion edges per second on 64 thousand BlueGene/Q nodes, that allowed the in-memory exploration of a petabyte-scale graph in just a few seconds. We believe that these techniques can be successfully applied to a broader class of graph algorithms.

Short bio - Fabrizio Petrini is the manager of the High Performance Analytics Department of the IBM TJ Watson Research Laboratory. His research interests include various aspects of multi-core processors and supercomputers, including high-performance interconnection networks, network interfaces, fault tolerance, and data-intensive computing algorithms for mining large data sets. He is the recipient of numerous awards for DOE, IEEE and ACM, including best paper awards from the international conference on supercomputing (SC 2003), the international supercomputing conference (ISC 2009), and the international parallel and distributed processing symposium (IPDPS 2003 and 2014).

Internet of Things : From hacking to industrialization

Paul Guermonprez
Intel Corporation

Abstract - Hobbyists have been playing with internet of things for years. They hack existing devices or 3D print their own and connect them via internet. As IoT demand is increasing, we need to find proper tools and methods to develop high quality IoT products, while maintaining the creativity of the hobbyist. The Intel Software Academic Program is working with universities to help and develop innovative student projects. We'll see what methods they use and results they achieve. Short bio - After 8 years in the biotech field, Paul Guermonprez joined Intel to optimize parallel software. He is now developing technical collaboration with universities all over Europe, Middle East, Africa and Russia

Towards Sentient Chips: Self-Awareness through On-Chip Sensemaking

Nikil Dutt
Center for Embedded Computer Systems (CECS)

Abstract - While the notion of self-awareness has a long history in biology, psychology, medicine, engineering and (more recently) computing, we are seeing the emerging need for self-awareness in the context of complex many-core chips that must address the (often conflicting) challenges of resiliency, energy, heat, cost, performance, security, etc. in the face of highly dynamic operational behaviors and environmental conditions. In this talk I will present the concept of CyberPhysical-Systems-on-Chip (CPSoC), a new class of sensor-actuator rich many-core computing platforms that intrinsically couples on-chip and cross-layer sensing and actuation to enable self-awareness. Unlike traditional MultiProcessor Systems-on-Chip (MPSoCs), CPSoC is distinguished by an intelligent co-design of the control, communication, and computing system that interacts with the physical environment in real-time in order to modify the system's behavior so as to adaptively achieve desired objectives and Quality-of-Service (QoS). The CPSoC design paradigm enables self-awareness (i.e., the ability of the system to observe its own internal and external behaviors such that it is capable of making judicious decision) and (opportunistic) adaptation using the concept of cross-layer physical and virtual sensing and actuations applied across different layers of the hardware/software system stack. The closed loop control used for adaptation to dynamic variation -- commonly known as the observe-decide-act (ODA) loop -- is implemented using an adaptive, reflexive middleware layer. The learning abilities of CPSoC provide a unified interface API for sensor and actuator fusion along with the ability to improve autonomy in system management. The CPSoC paradigm is the first step towards a holistic software/hardware effort to make complex chips "sentient".

Short bio - Nikil Dutt is a Chancellor's Professor of CS, Cognitive Sciences, and EECS at the University of California, Irvine. He received a PhD from the University of Illinois at Urbana-Champaign (1989). His research interests are in embedded systems design automation, computer architecture, optimizing compilers, system specification techniques, distributed embedded systems, and brain-inspired architectures and computing. He has received numerous best paper awards and is coauthor of 7 books. Professor Dutt served as EiC of ACM TODAES (2003-2008) and as AE for ACM TECS and IEEE TVLSI. He has served on the steering, organizing, and program committees of several premier CAD and Embedded System Design conferences and workshops, and serves or has served on the advisory boards of ACM SIGBED, ACM SIGDA, ACM TECS and IEEE ESL. Professor Dutt is a Fellow of the IEEE, an ACM Distinguished Scientist, and recipient of the IFIP Silver Core Award.

Dealing with a World of Data: A Systems Perspective

H. Peter Hofstee
IBM Austin Research Laboratory

Abstract - Increasingly Big Data computing is being applied to some of the world's most difficult, most urgent problems. This talk will describe the nature of Big Data computing and present technology that has been developed to allow Big Data computing systems to address these challenges. We discuss the design of systems for Big Data and their corresponding middleware and look at how both of these might evolve and challenge the current thinking about Big Data systems. Finally we motivate shared-memory heterogeneous architectures in this context and we discuss the coherent attach processor interface on Power 8 as a concrete example of how to achieve a system-level benefit.

Short bio - H. Peter Hofstee currently works at the IBM Austin Research Laboratory on workload-optimized and hybrid systems. Peter has degrees in theoretical physics (MS, Rijks Universiteit Groningen, Netherlands) and computer science (PhD, California Inst. of Technology). At IBM Peter has worked on microprocessors, including the first CMOS processor to demonstrate GHz operation (1997), and he was the chief architect of the synergistic processor elements in the Cell Broadband Engine, known from its use in the Sony Playstation 3 and the Roadrunner supercomputer that first broke the 1 Petaflop Linpack benchmark. His interests include VLSI, multicore and heterogeneous microprocessor architecture, security, system design and programming. Peter is an IBM master inventor with over 100 patents.

On how to design smart energy-efficient buildings

Donatella Sciuto
Politecnico di Milano

Abstract - Smart spaces are environments such as apartments, offices, museums, hospitals, schools, malls, university campuses, and outdoor areas that are enabled for the cooperation of objects (e.g., sensors, devices, appliances) and systems that have the capability to self-organize themselves, based on given policies. Since they can be used for an efficient management of the energy consumption of buildings, there is a growing interest for them, both in academia and industry. Unfortunately, nowadays, these systems are still designed manually with ad-hoc solutions. As a consequence, a huge effort has to be spent for each new smart building. Within this context, aim of this work is to propose a methodology to automate the design process of such smart spaces. The paper presents an overview of the design flow implemented to support the design of scalable architectures for energy aware smart spaces.

Short bio - Donatella Sciuto received her Laurea in Electronic Engineering from Politecnico di Milano and her PhD in Electrical and Computer Engineering from the University of Colorado, Boulder. She is currently Vice Rector of the Politecnico di Milano and Full Professor in Computer Science and Engineering. She is in the Board of Governors of the Bank of Italy. Her main research interests cover the methodologies for the design of embedded systems and multicore systems, from the specification level down to the implementation of both the hardware and software components, including reconfigurable and adaptive systems. She has published over 200 scientific papers. She is a Fellow of IEEE and has been President of the IEEE Council of Electronic Design Automation for the past two years. She has been in the executive and program committees of different conferences and journals in the area of Electronic Design Automation.

Workshops and Tutorials

Workshops

Xilinx Workshop

During this Xilinx University Program professor workshop, attendees will have an opportunity to learn about the latest Xilinx technology, devices, and trends, and will gain practical experience of working with Xilinx Vivado, IP Integrator, and Vivado HLS to create designs for Xilinx Zynq All Programmable SOC devices. There will also be an opportunity to network with Xilinx University Program staff and find out about the Xilinx University Program. Topics covered will include an introduction to Xilinx 7 series devices and technology, an overview of the new Vivado design flow, System Design using IP Integrator, Embedded design for the Xilinx Zynq SOC (based on the ARM Cortex A9 dual core processor), and higher level design using Vivado High Level Synthesis. Hands-on labs using the Xilinx ZyBo Zynq development board will cover hardware design, software design for the ARM Cortex A9, custom IP, hardware and software debugging, creation of hardware accelerators using Vivado high level synthesis.

More info: http://www.xilinx.com/university/workshops/workshop-schedule.htm

Intel Workshop

Experimenting with electronics using Arduino is fun, but what if you need more software and networking capabilities ? There's a board for that : the Intel Galileo. It's an Intel based linux PC with analogic and digital IO, plus USB and other typical PC ports. During this workshop, we'll see how to code for Internet of Things using Intel Galileo. Any linux compatible language can be used. We'll also brainstorm to find the best IoT project ideas. Should you want to see the technical details and get ready, Open Source Courseware can be found at : http://intel-software-academic-program.com/pages/courses#iot

Speaker bio: Trained as a biologist, Paul Guermonprez worked for 8 years in the biotech field as a software developer and bioinformatician. He then joined Intel Software as an application engineer to optimize parallel software in the biotech and medical field. After 5 years, Paul took in charge the Intel Software Academic Program for the EMEA-Russia geo. The Academic program is developing technical collaborations with professors and students to make software fun and innovative. Various aspects of the program include : Hardware seeding programs, workshops, contests, mentorship. Topics covered : Internet of Things, HPC, mobile programming, perceptual computing

CHANGE Workshop

International Workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (CHA'N'GE). Its objective is to bring together researchers and industry from all over the world for a wide ranging discussion of self-aware adaptive systems, including, but not limited to: system architectures, self-aware operating systems, autonomous self-aware computer architecture, dynamic reconfiguration, applications, embedded processors, adaptive algorithm and distributed self-training algorithms, biologically inspired systems, surveys and/or prospective papers in self-aware computing systems, etc.

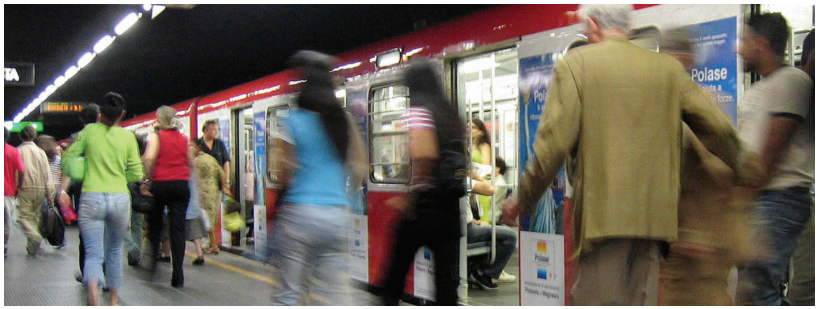
Tutorials

On how to efficiently exploit reconfiguration aspects from your design - The FASTER tool chain

Extending the functionality and the lifetime of products requires the addition of new functionality to track and satisfy the customer's needs and market and technology trends. While adaptability of software components is straightforward, products include hardware accelerators –for reasons of performance and power efficiency- that also need to adapt to the new requirements. Hardware solutions can achieve high performance, and software solutions can easily adapt to the new set of threats, but neither can achieve flexibility and high performance at the same time. Reconfigurable logic allows the definition of new functions to be defined in hardware units, combining hardware speed and efficiency, with ability to adapt and cope in a cost effective way with expanding functionality, changing environmental requirements, improvements in system features, changing protocols and data-coding standards, etc. However, designing, implementing and verifying reconfigurable hardware systems is harder compared to static ones. This workshop aims at bringing together experts to discuss current technologies and trends in the reconfigurable computing area. This tutorial tends to focus on different topics/objectives of the design of computing systems to include reconfigurability as an explicit design concept. Current tools seem to lack a framework for system design where run-time adaptability, provided by dynamic hardware reconfiguration, becomes pivotal to computing system design.
In this tutorial we will present cutting-edge research aiming at developing techniques and tools that analyze the structure and performance of the application, map it according to the capabilities of the underlying implementation platform, and provide a dynamically reconfigurable system implementation, e.g. through both micro-reconfiguration and module-based reconfiguration.

ILDJIT: Hands-On ILDJIT 2.0 for Static and Dynamic Program Analysis and Transformation

ILDJIT is a mature, open source, publicly available compilation framework that includes both static and dynamic compilers. Examples of well known benchmark suites supported by ILDJIT are SPEC CPU2000, SPEC CPU2006, MiBench and PARSEC. ILDJIT provides a plugin-based framework for static, as well as dynamic tasks like code translation, code analysis, code optimization, runtime instrumentation and memory management. Its plugin-based framework allows users to easily customize execution both at installation time and at run-time (by dynamically loading and unloading plugins without perturbing execution). Moreover, its multi-threaded design allows novel introspection of parallel compilation strategies to reduce overheads and dynamically optimize running code on today's x86 multi-core systems. The framework provides a rich intermediate language (IR), which users can exploit inside their own extensions. ILDJIT allows users to choose which extensions to execute at static time and which ones to execute at runtime. In order to simplify the implementation of high level code analysis, IR includes both simple RISC-like instructions (e.g. load, store, add) and high level operations. High level operations include both classic thread synchronization tasks, such as wait for another thread, create thread, memory barriers and memory management tasks, such as create a new array, free a piece of memory and create a new aligned piece of memory. ILDJIT supports the CIL language, which includes the full information of the source language by having a rich set of metadata. Nowadays, several source languages are successfully translated to CIL including C, C++, C#, Java, Python and LISP. Hence, by providing the full support of the complex CIL language, ILDJIT is able to manage, analyze and optimize all of the above languages. Users of ILDJIT do not need to handle unnecessary details of the source language used because they can rely on the IR of ILDJIT to perform their tasks. We believe ILDJIT is useful to anyone interested in compilers and computer architecture research. It provides a platform for dynamically introspecting and performing code transformations on CIL bytecode programs. These management environments are emerging as the dominant front for run-time execution because of their platform-independent interoperability. In this tutorial, we demonstrate how users can exploit the ILDJIT framework for research-specific purposes. We will compare and contrast the ease of using ILDJIT relative to more commonly known tools like Pin and Dynamo. We will also demonstrate the ease of using ILDJIT relative to its CIL counterparts like Mono, DotNet and DotGNU that, while robust, are not well suited for research purposes. Design and development of software includes the monitoring of its runtime behaviors (e.g. for performance or memory usage evaluation), which depend on both the underlying platform and the compilation process. On the other hand, the design of new hardware includes evaluation of both its performance and power consumption while running software that expose typical workloads. Hence, both software and hardware evaluation need runtime analysis, which should also include static or dynamic software transformations.



Other information

- Expected duration of the tutorial: full day
- Morning: lectures and demos
- Afternoon: hands-on exercises

Organizer short bio - Simone Campanoni is a research associate in Computer Science at Harvard University working with Prof. David Brooks and with Prof. Gu-yeon Wei. His work focuses on the boundary between hardware and software, relying on dynamic compilation, run-time optimizations and virtual execution environments for investigating opportunities on auto-parallelization. He is the author of the HELIX research project (http://helix.eecs.harvard.edu) and the ILDJIT compilation framework (http://ildjit.sourceforge.net).

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