Floorplanning for Partially-Reconfigurable FPGA Systems via Mixed-Integer Linear Programming

P²C WEEK, Milano
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POLITECNICO DI MILANO

FASTER

P²C week

Rationale and Innovation

- Problem statement
  - Given a partially-reconfigurable FPGA, find on-chip area constraints to meet the design requirements

- Innovative contribution:
  - Consider arbitrary distribution of heterogeneous resources
  - Possibility to customize the objective function
  - Control on the quality of the desired solution

Aims

- Considering the area assignment problem tailored for partially-reconfigurable FPGAs, provide:
  - A Mixed-Integer Linear Programming (MILP) model to improve the quality of heuristic solutions
  - An effective MILP model to find the optimal solution

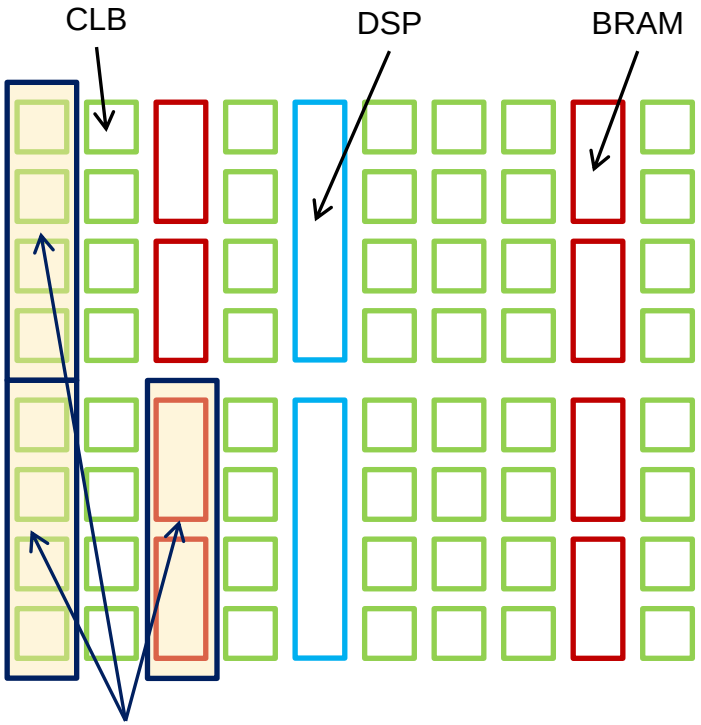
Outline

- Introduction
- Problem definition and state-of-the-art
- The Proposed Approach
- Overall system evaluation
- Conclusions and Future Work
- Demo

INTRODUCTION

FPGA (Field-Programmable Gate Array)

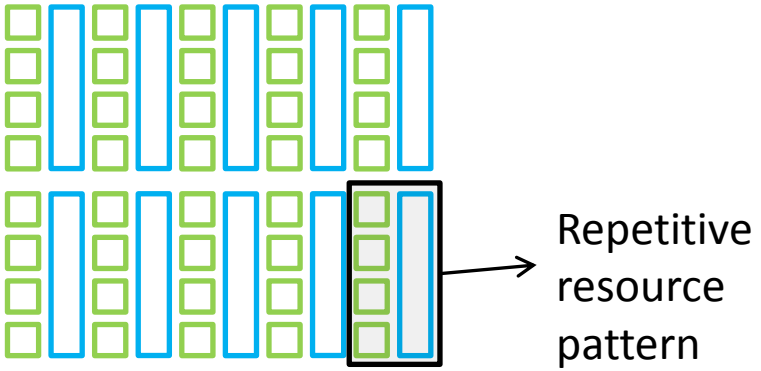
- FPGA characteristics
  - Heterogeneous resources
  - Reconfigurable device
  - Reconfiguration constraints
- Different resource distribution:
  - Uniform
  - Non-Uniform
- Different reconfiguration
  - Total
  - Partial (static)
  - Partial (dynamic)



Tiles: minimal reconfigurable units

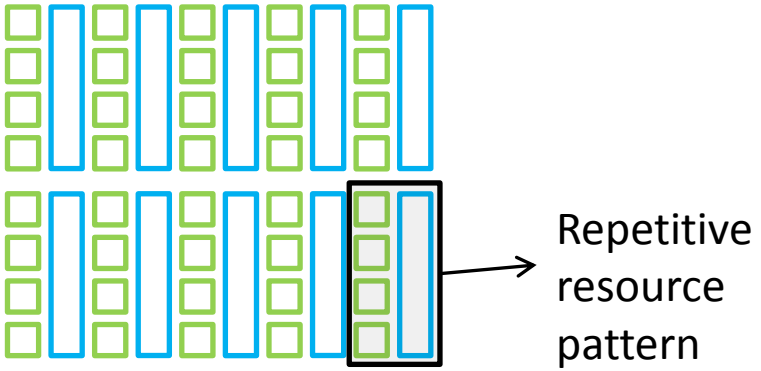
FPGA: resource distribution

- Uniform distribution
  - Xilinx Spartan3
  - Xilinx Virtex-II

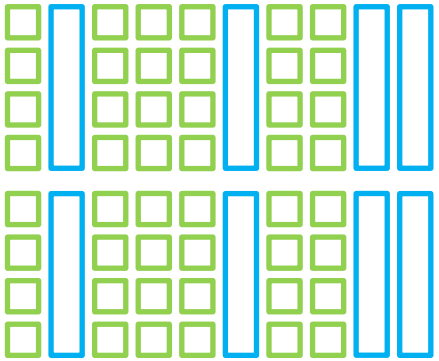


FPGA: resource distribution

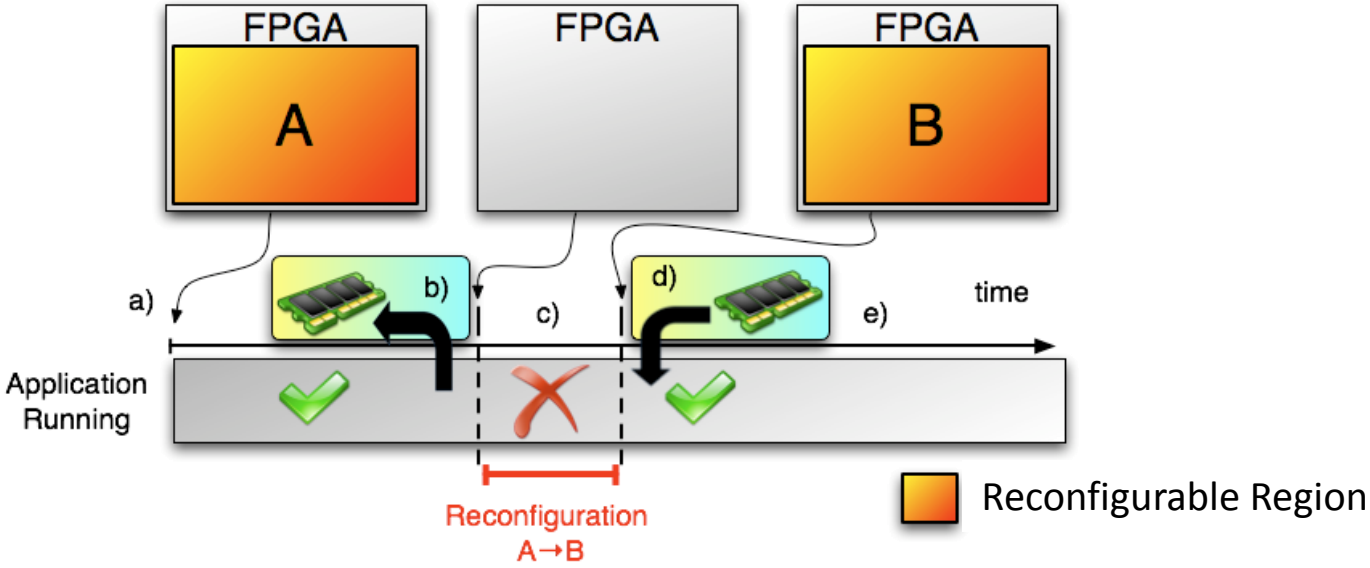
- Uniform distribution
  - Xilinx Spartan3
  - Xilinx Virtex-II



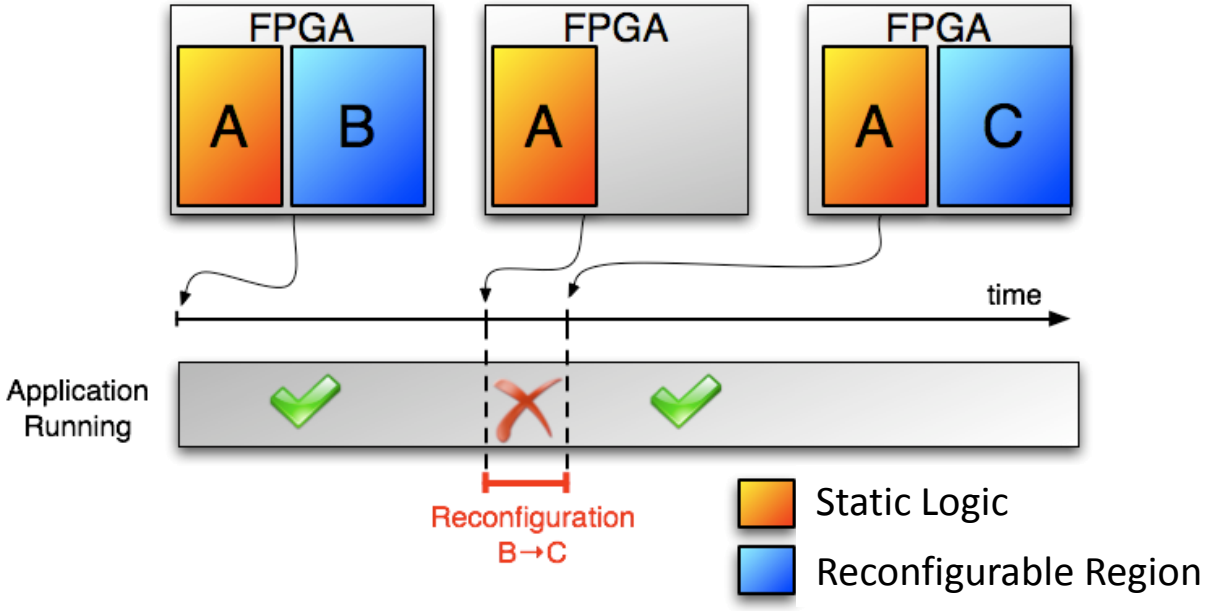
- Non-Uniform distribution
  - Xilinx Virtex-4
  - Xilinx Virtex-5



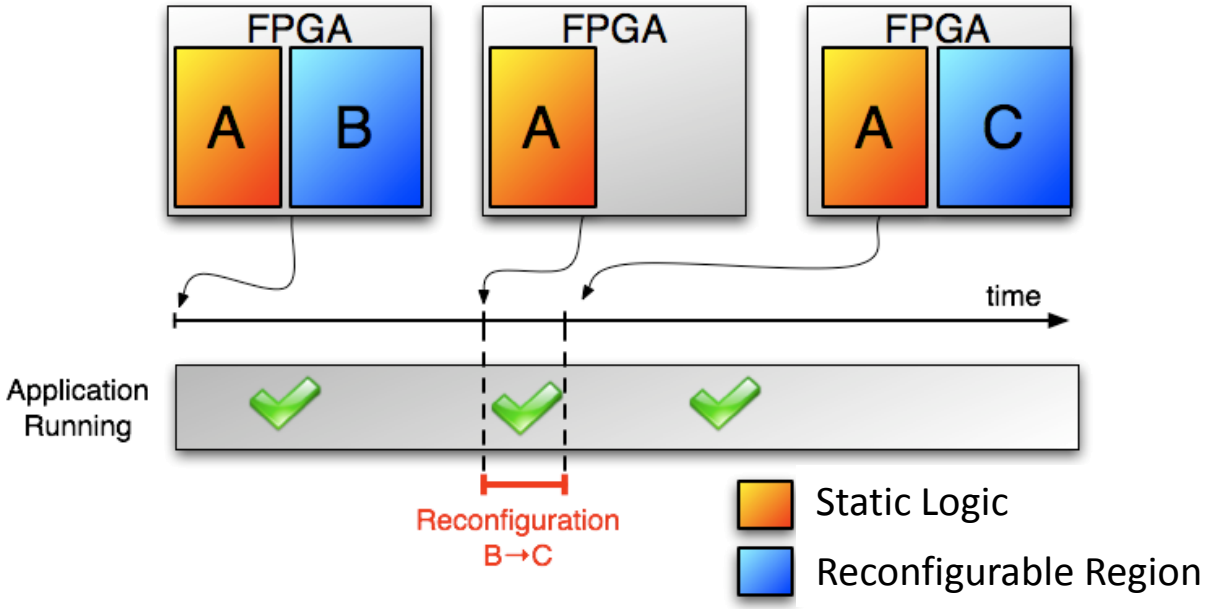
FPGA: total reconfiguration



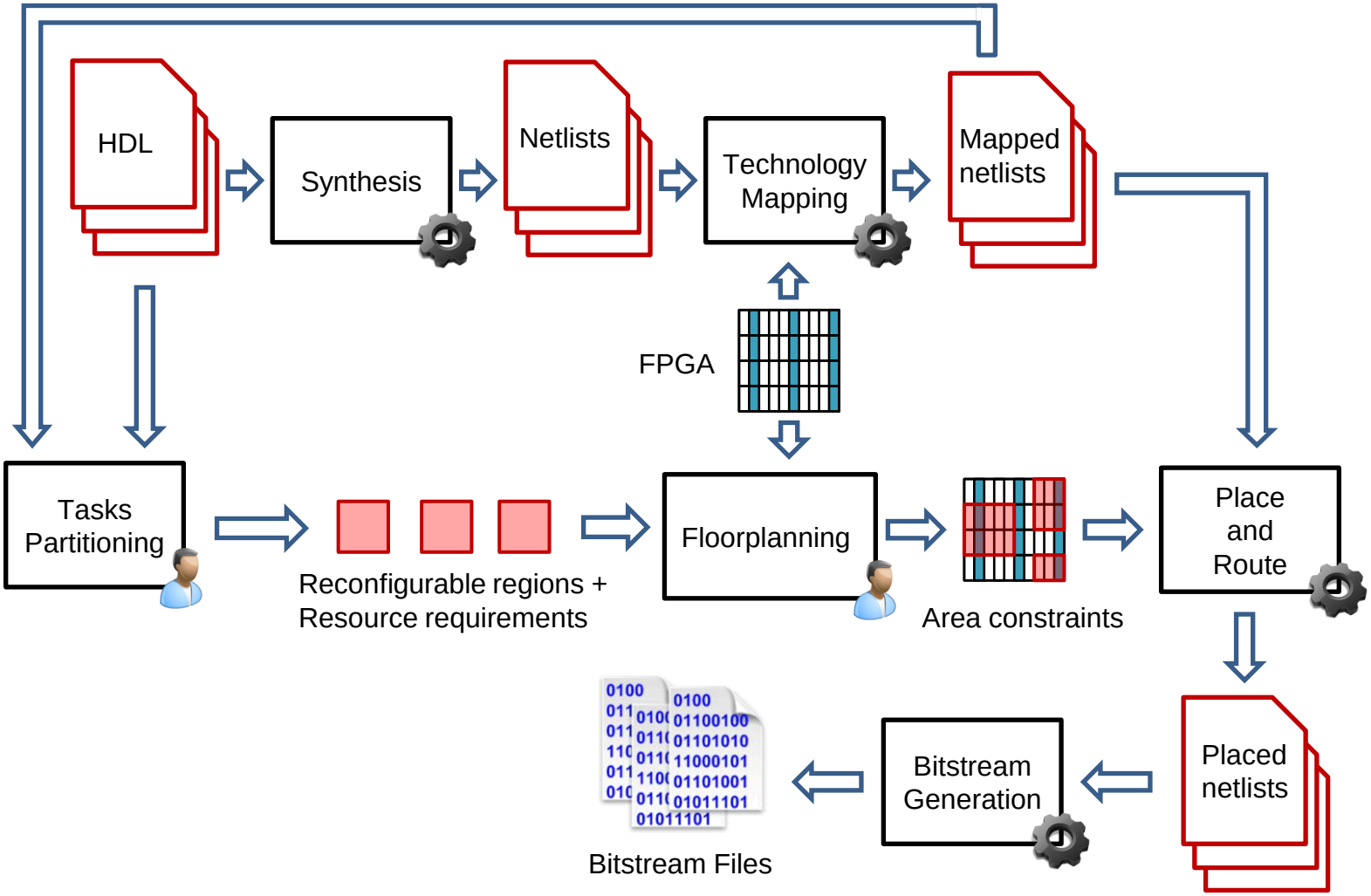
FPGA: partial (static) reconfiguration



FPGA: partial (dynamic) reconfiguration



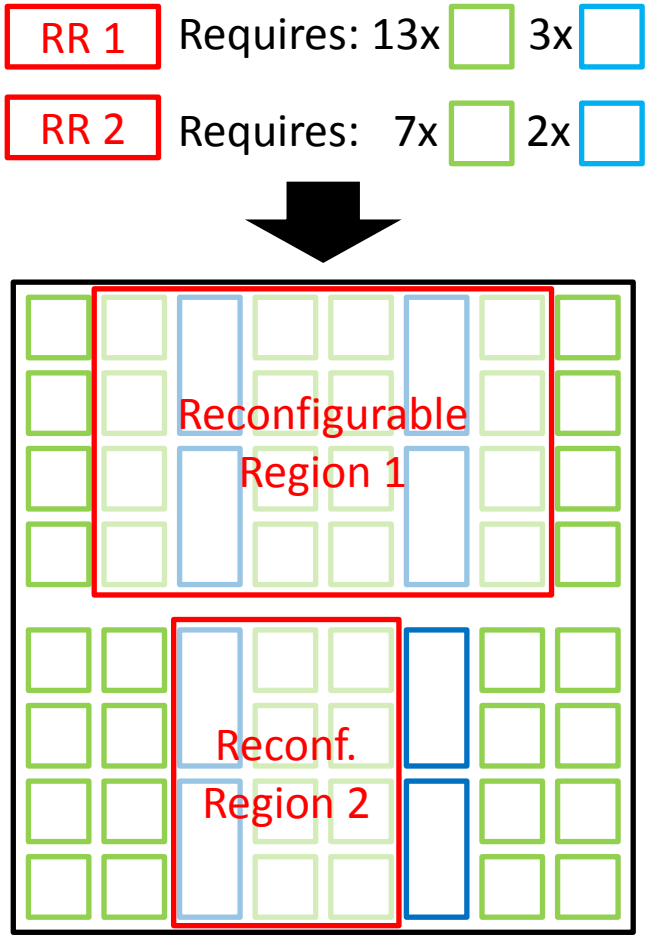
Partial dynamic design flow



PROBLEM DEFINITION AND STATE-OF-THE-ART

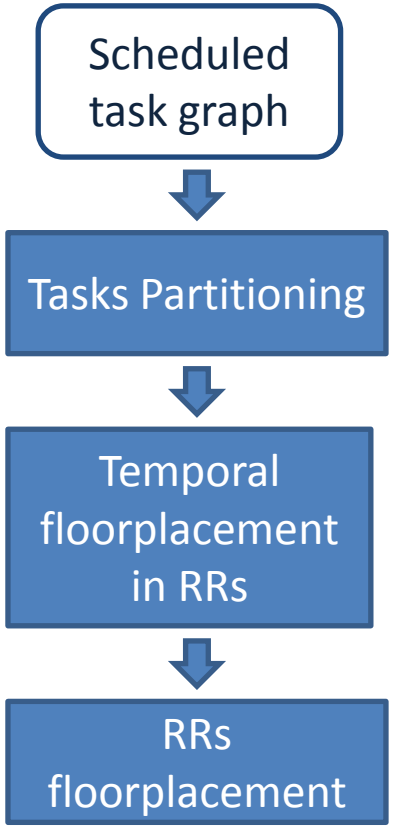
Floorplanning problem

- Given:
  - An FPGA
  - A set N of reconfigurable regions (RRs)
  - The resource requirements $\forall n \in N$
- Aim:
  - Find a rectangular area for each region, such that:
    - No two regions overlap
    - Complete tiles are covered
    - All the resource requirements are met
    - A given objective function is optimized



Related work - I

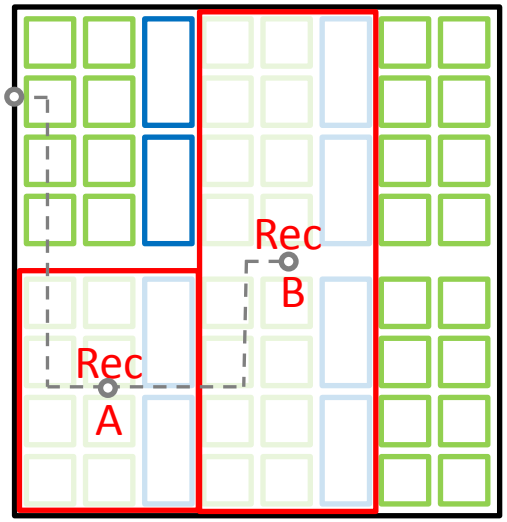
- [*] Is a 3 steps floorplacer based on simulated annealing
  - Considers both partitioning and floorplanning
  - Optimizes external wirelength and area
- Limits
  - Considers only uniform resource distribution
  - No guarantee on the solution quality
  - Objective function not customizable



[*] Montone, A., Santambrogio, M. D., and Sciuto, D.: Wirelength driven floorplacement for FPGA-based partial reconfigurable systems. In IPDPS Workshops, pages 1-8, 2010.

Related work - II

- [*] Is an adaption of Parquet [**] for Floorplanning on heterogeneous FPGAs
  - Considers arbitrary resource distribution
  - Optimizes internal and external wirelength
- Limits
  - Suboptimal search space
  - Objective function only based on wirelength



Sequence pair: $(\langle A, B\rangle, \langle A, B\rangle)$

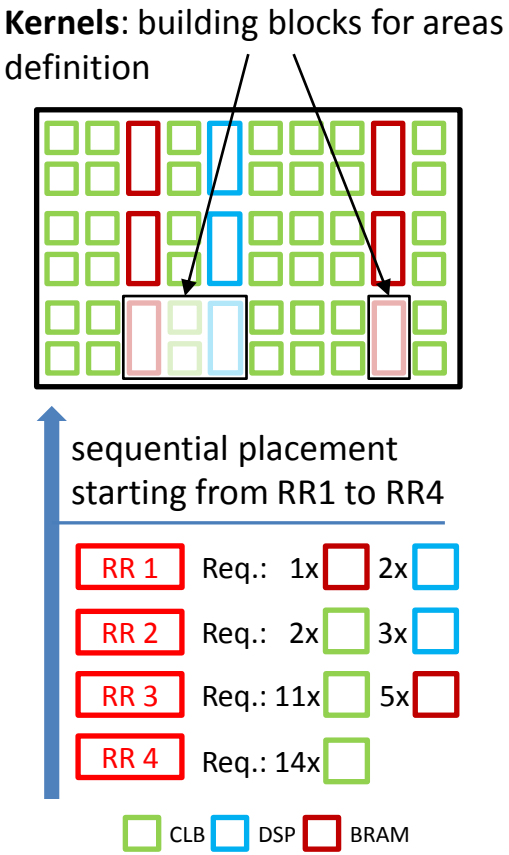
Height vector: $\{h_A = 1, h_B = 2\}$

[*] Bolchini, C., Miele, A., and Sandionigi, C.: Automated Resource-Aware Floorplanning of Reconfigurable Areas in Partially-Reconfigurable FPGA Systems. In FPL, pages 532-538, 2011.

[**] Adya, S. N. and Markov, I. L.: Fixed-outline floorplanning: enabling hierarchical design. IEEE Trans. VLSI Syst., 11(6):1120-1135, 2003.

Related work - III

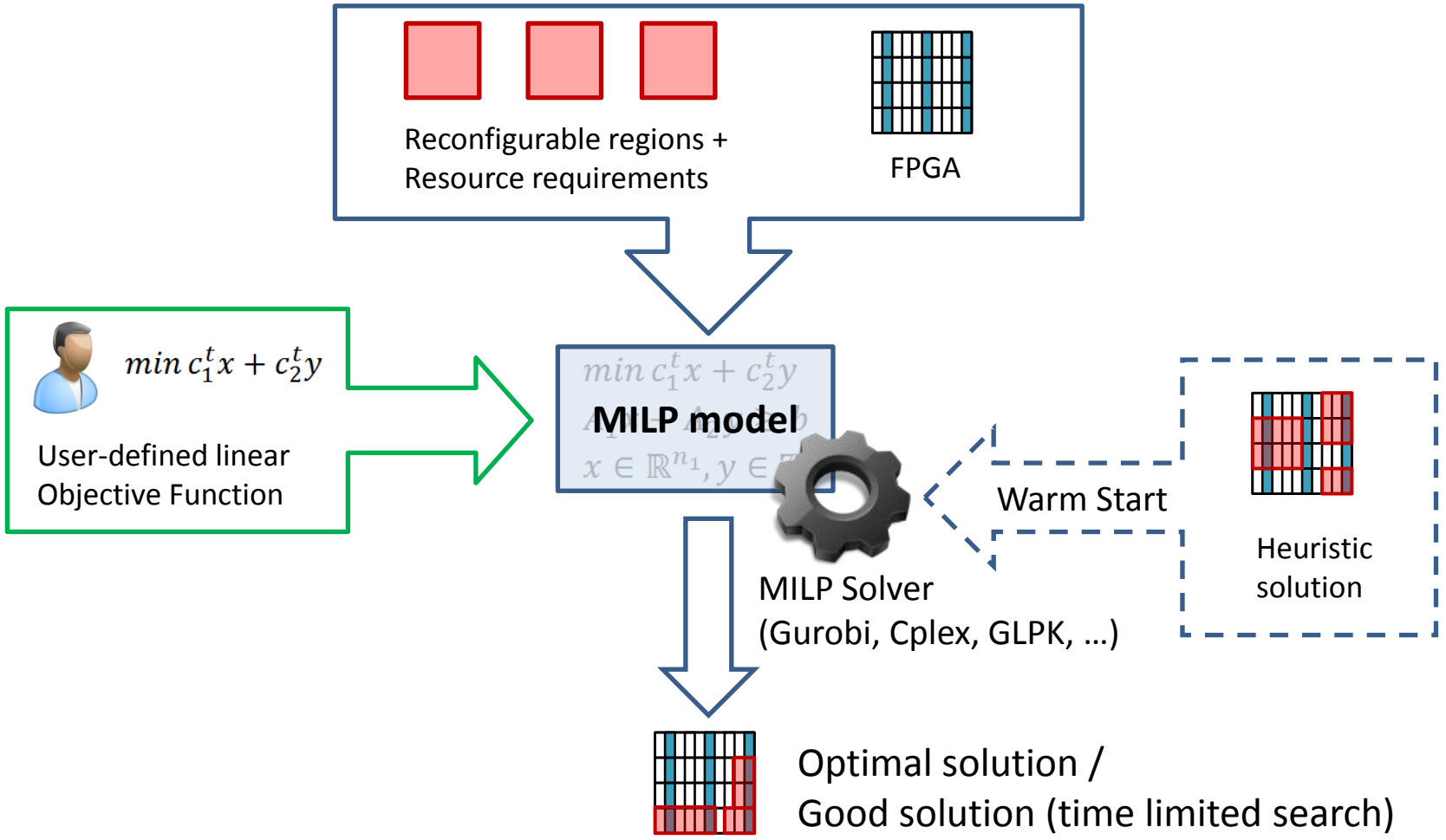
- [*] Introduces Columnar Kernel Tesselation
  - Takes into account complex device architecture
  - Optimizes area and internal wirelength
- Limits
  - Unexplored potentially promising solutions (fixed placement order of regions)
  - Objective function biased towards area optimization



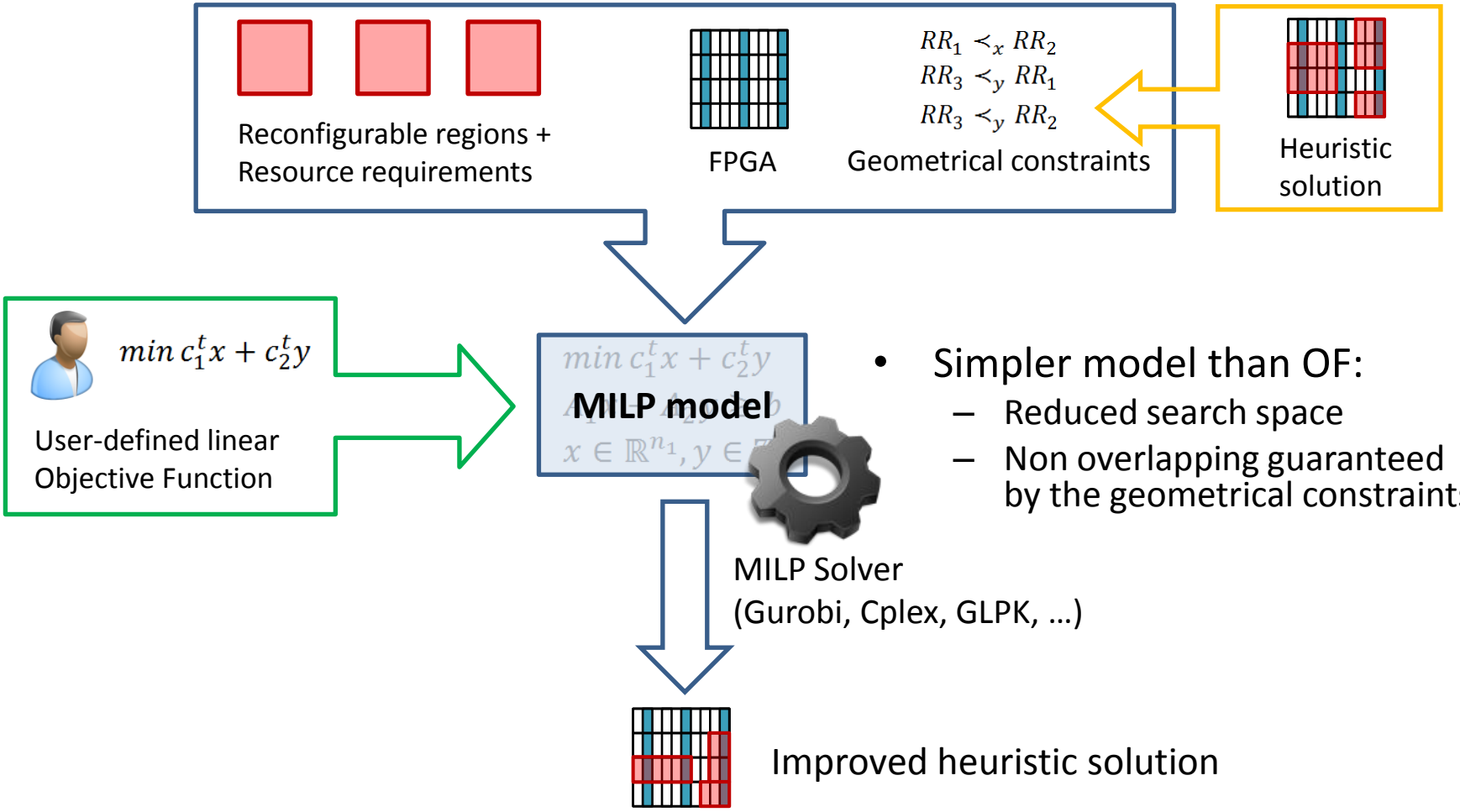
[*] Vipin, K. and Fahmy, S. A.: Architecture-aware reconfiguration-centric floorplanning for partial reconfiguration. In ARC, pages 13-25, 2012.

THE PROPOSED APPROACH

Optimal Floorplanner (OF)

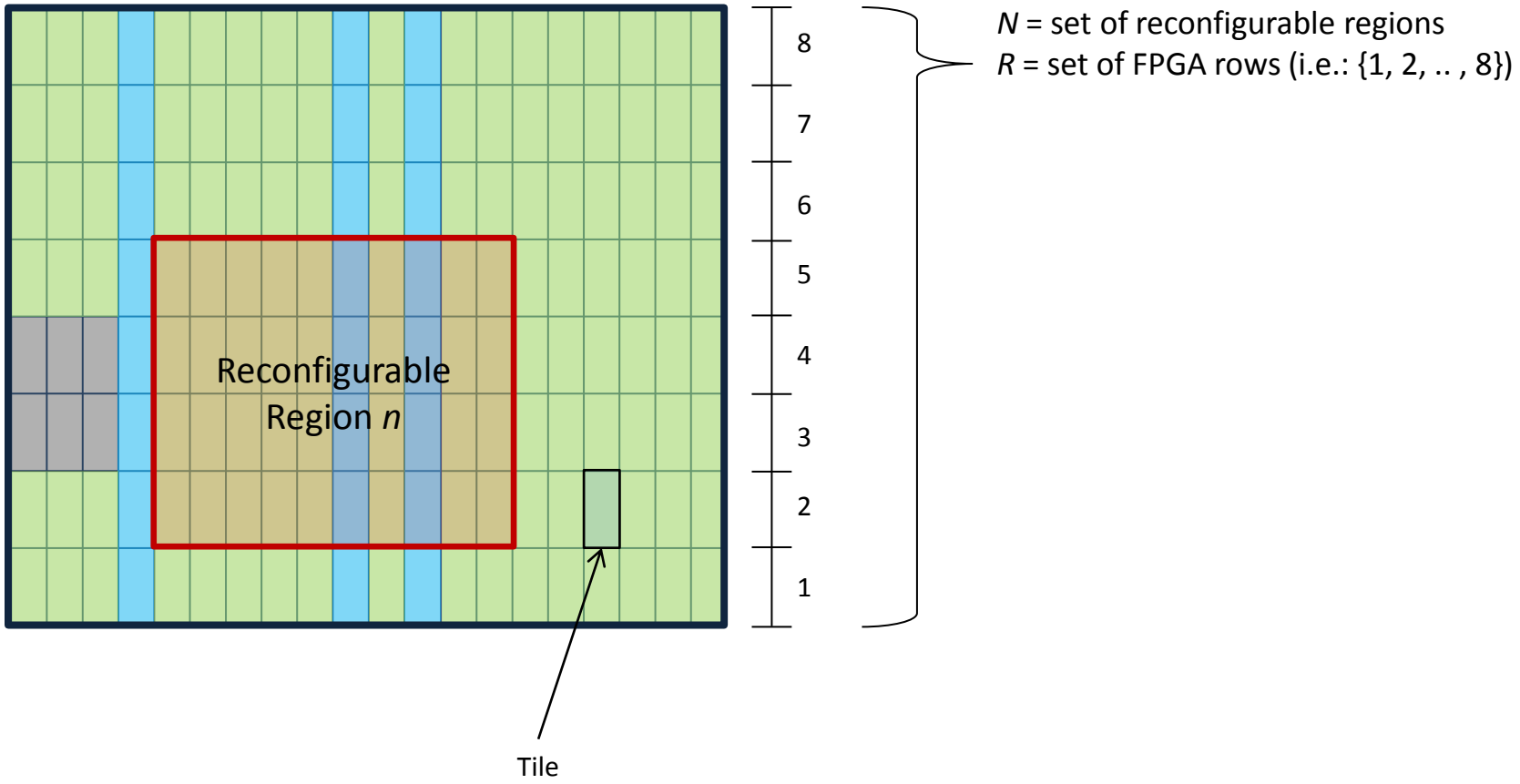


Heuristic-Optimal Floorplanner (HOF)

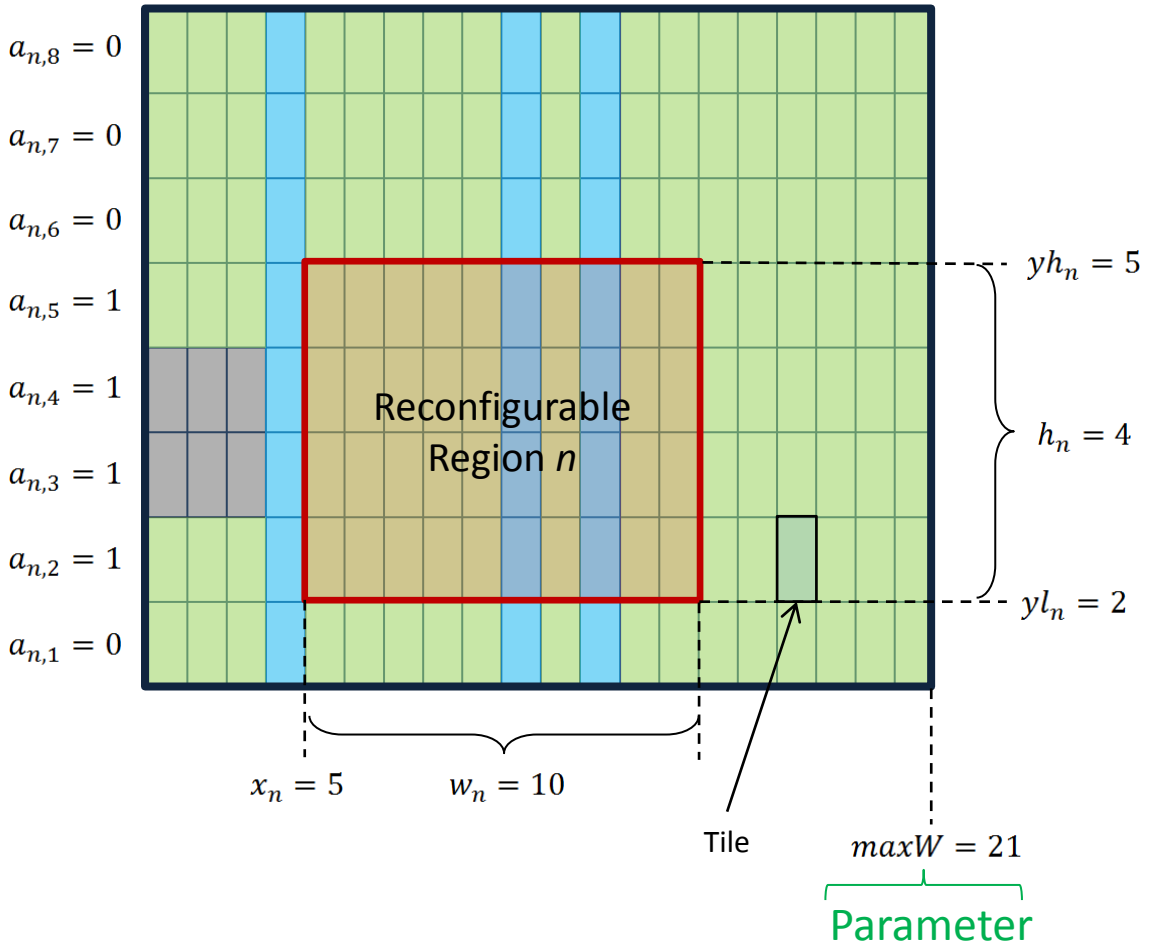


- Simpler model than OF:
  - Reduced search space
  - Non overlapping guaranteed by the geometrical constraints

MILP: Problem linearization - I



MILP: Problem linearization - II



N = set of reconfigurable regions
R = set of FPGA rows (i.e.: {1, 2, .. , 8})

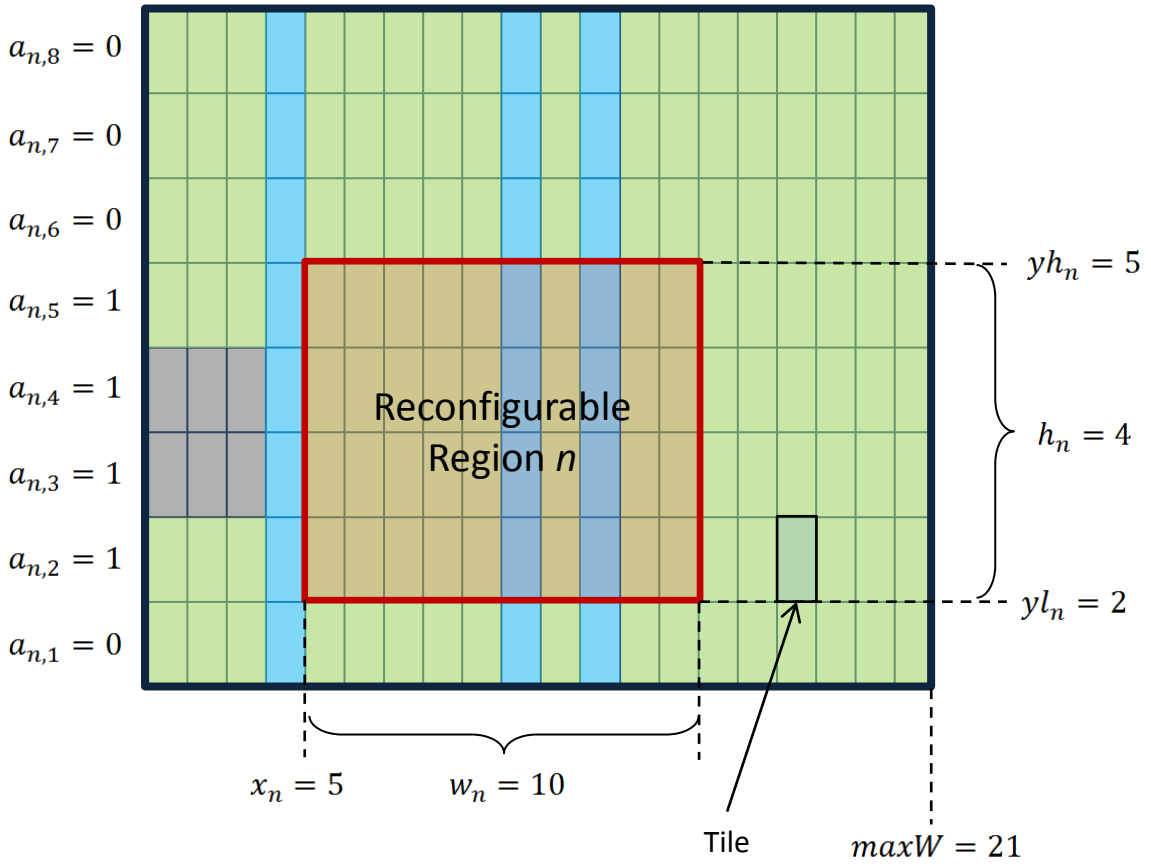
Variables:

$\forall r \in R, n \in N$:

Integer
- $a_{n,r} \in \{0,1\}$
- $x_n \in \mathbb{Z}^+$
- $w_n \in \mathbb{Z}^+$

Real
- $yh_n \in \mathbb{R}$
- $h_n \in \mathbb{R}$
- $yl_n \in \mathbb{R}$

MILP: Problem linearization - III



N = set of reconfigurable regions
R = set of FPGA rows (i.e.: {1, 2, .. , 8})

Semantic constraints:

$\forall n \in N$:

$$x_n + w_n \leq maxW$$

$$h_n = \sum_{r \in R} a_{n,r}$$

$$yh_n - yl_n + 1 = h_n$$

$\forall n \in N, r \in R$:

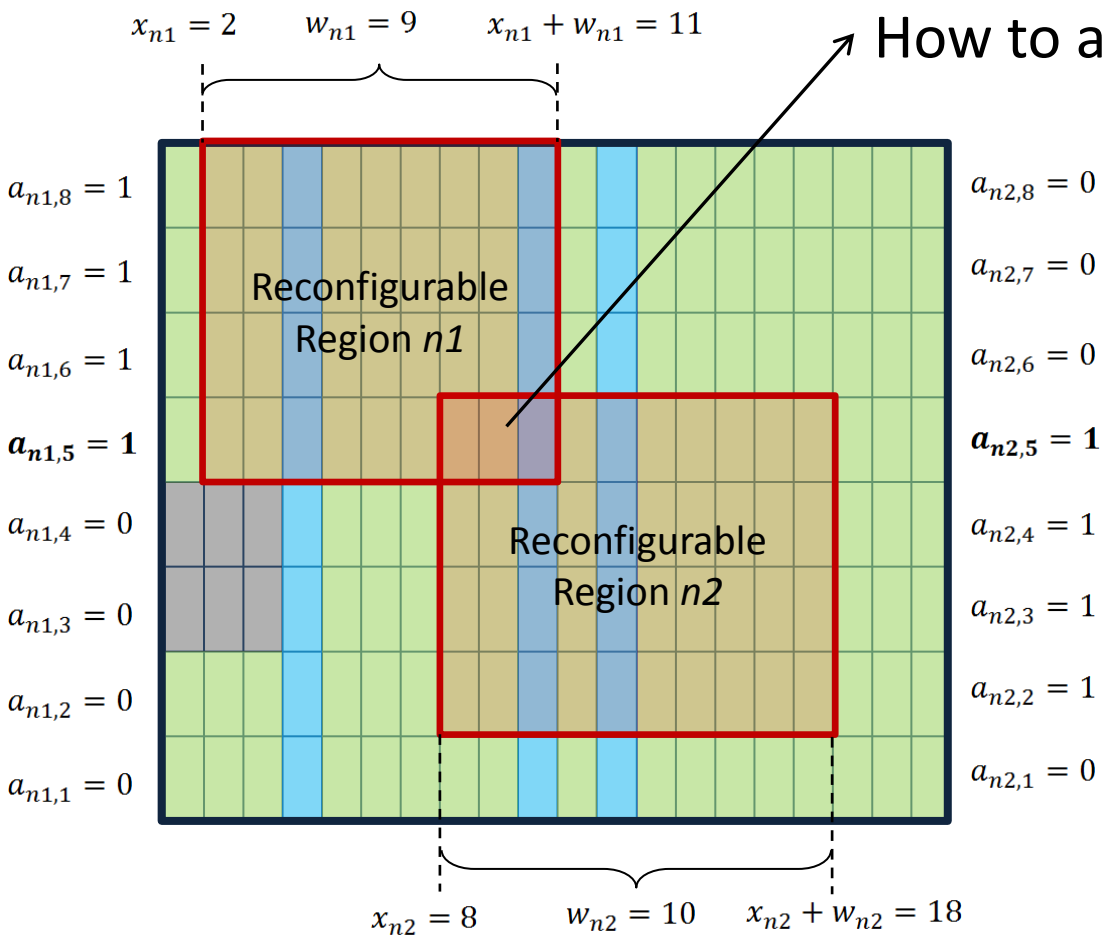
$$yl_n \leq |R| - a_{n,r} \cdot (|R| - r)$$

$$yh_n \geq a_{n,r} \cdot r$$

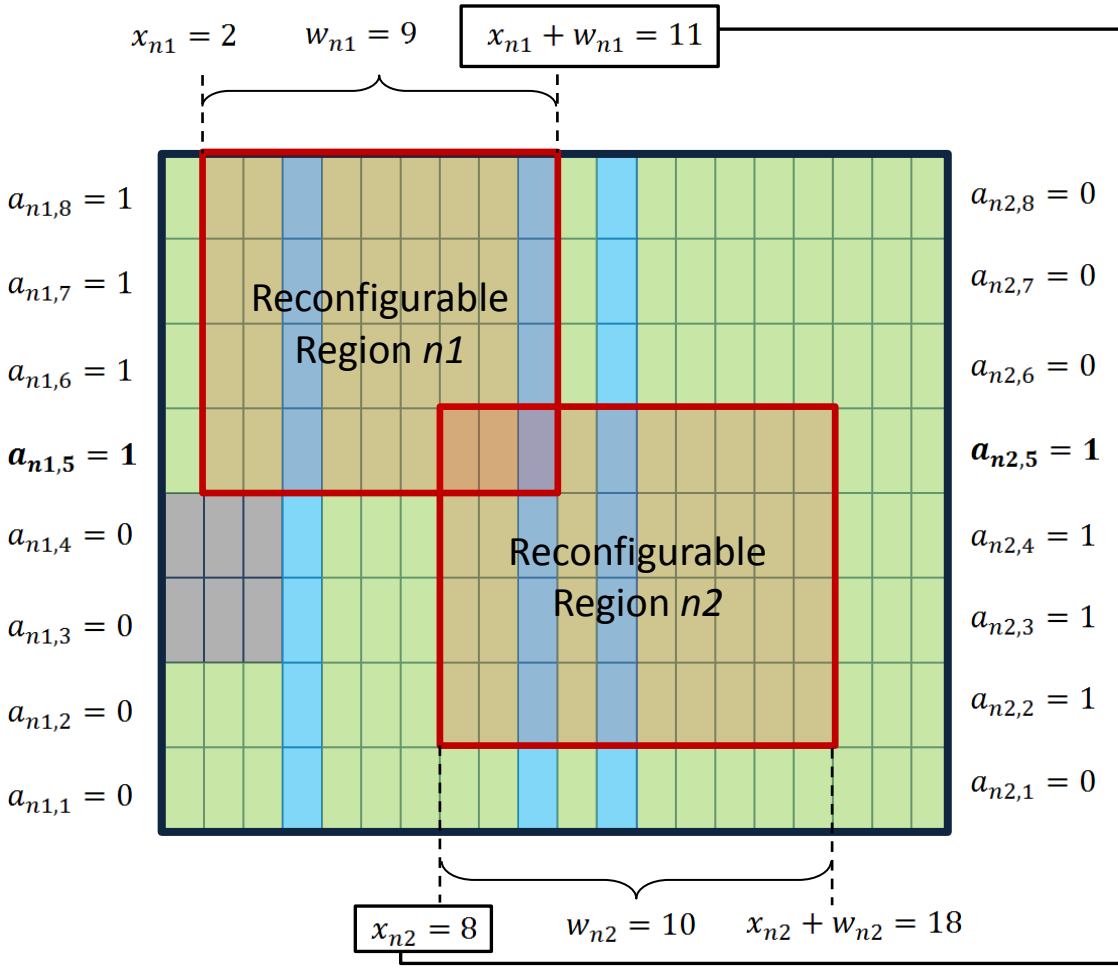
$\forall n \in N, r1, r2, r3 \in R | r3 > r2 > r1$:

$$a_{n,r2} \geq a_{n,r1} + a_{n,r3} - 1$$

Non overlapping (OF) - I



Non overlapping (OF) - II

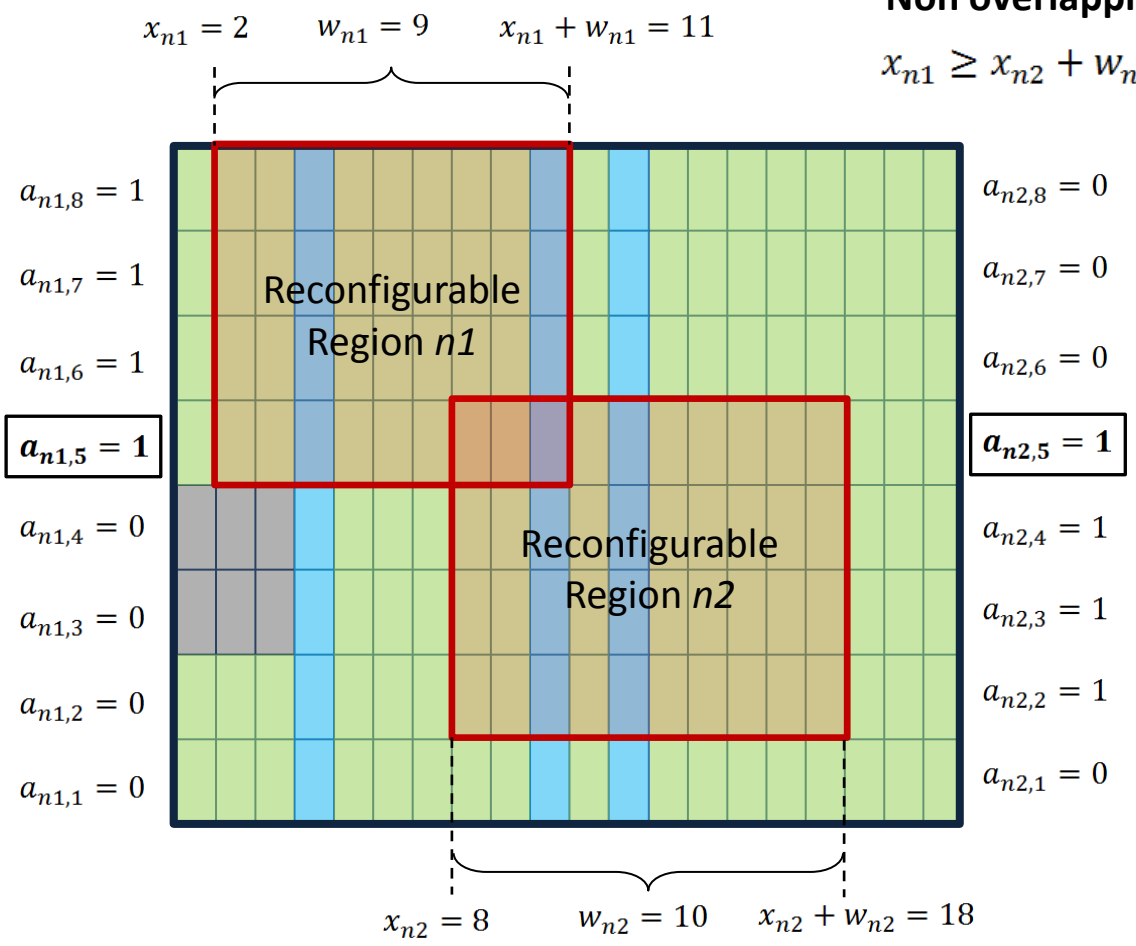


$$g_{n1,n2} = 1$$

binary variable forced to 1 if region ***n1*** is not to the left of region ***n2***:

$$x_{n1} + w_{n1} \leq x_{n2} + g_{n1,n2} \cdot maxW$$

Non overlapping (OF) - III



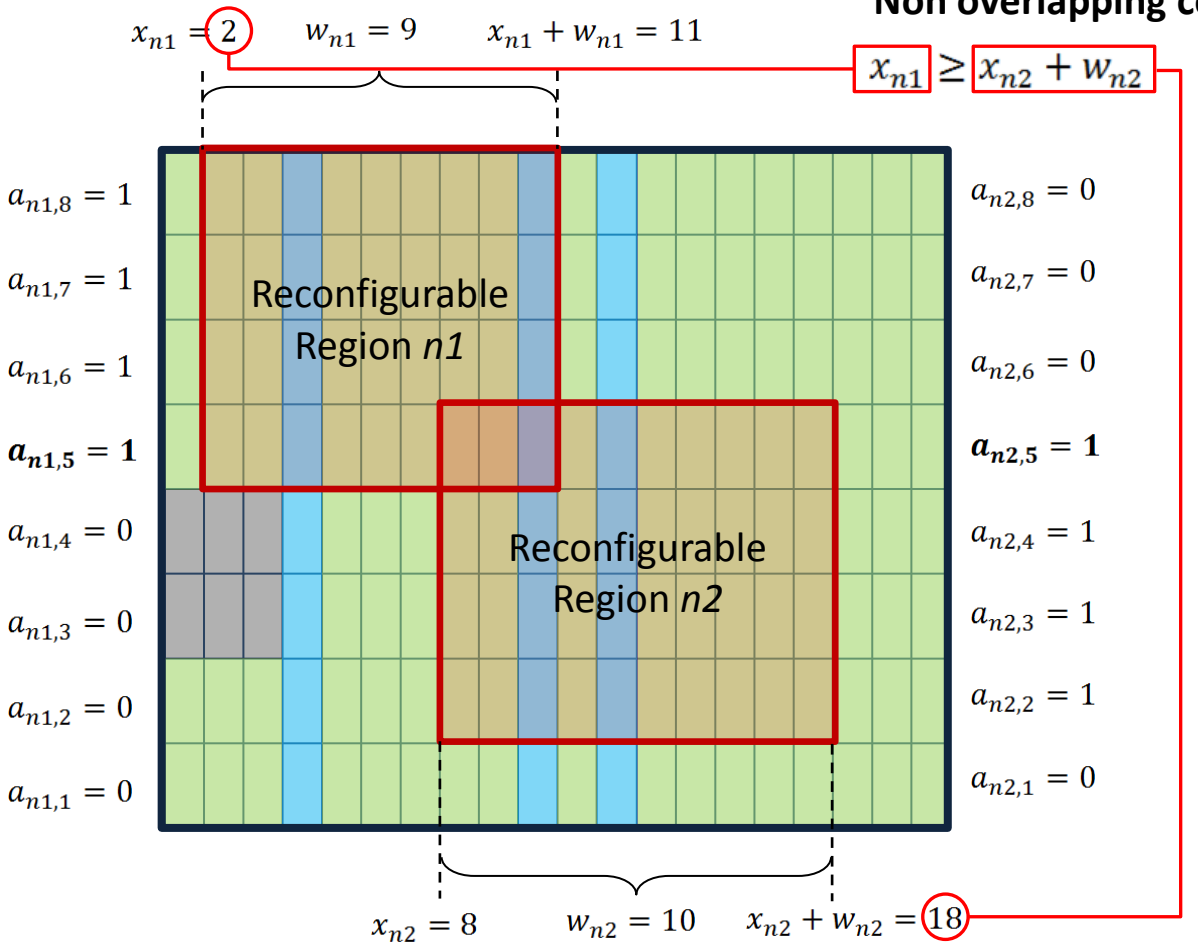
Non overlapping constraint:

$$x_{n1} \geq x_{n2} + w_{n2} - (3 - g_{n1,n2} - a_{n1,r} - a_{n2,r}) \cdot maxW$$

$$g_{n1,n2} = 1$$

binary variable forced to 1 if region ***n1*** is not to the left of region ***n2***:

Non overlapping (OF) - IV



Non overlapping constraint:

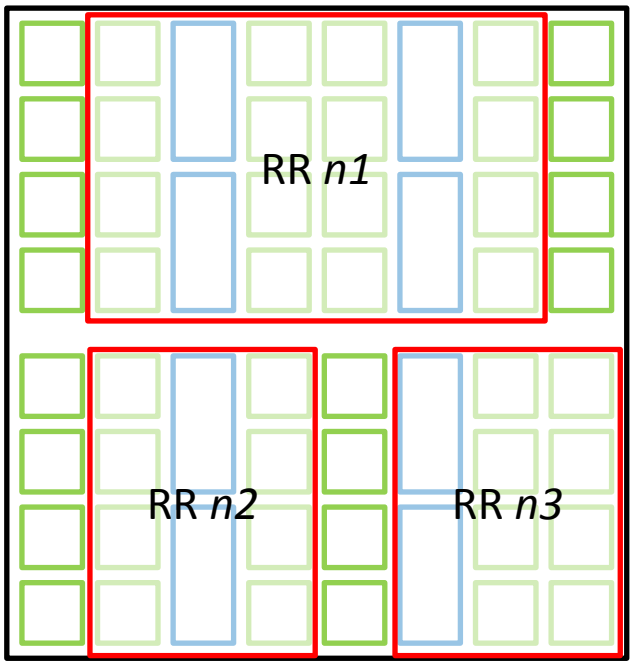
$x_{n1} \geq x_{n2} + w_{n2}$

Violation!

$$g_{n1,n2} = 1$$

binary variable forced to 1 if region ***n1*** is not to the left of region ***n2***:

Non overlapping (HOF)



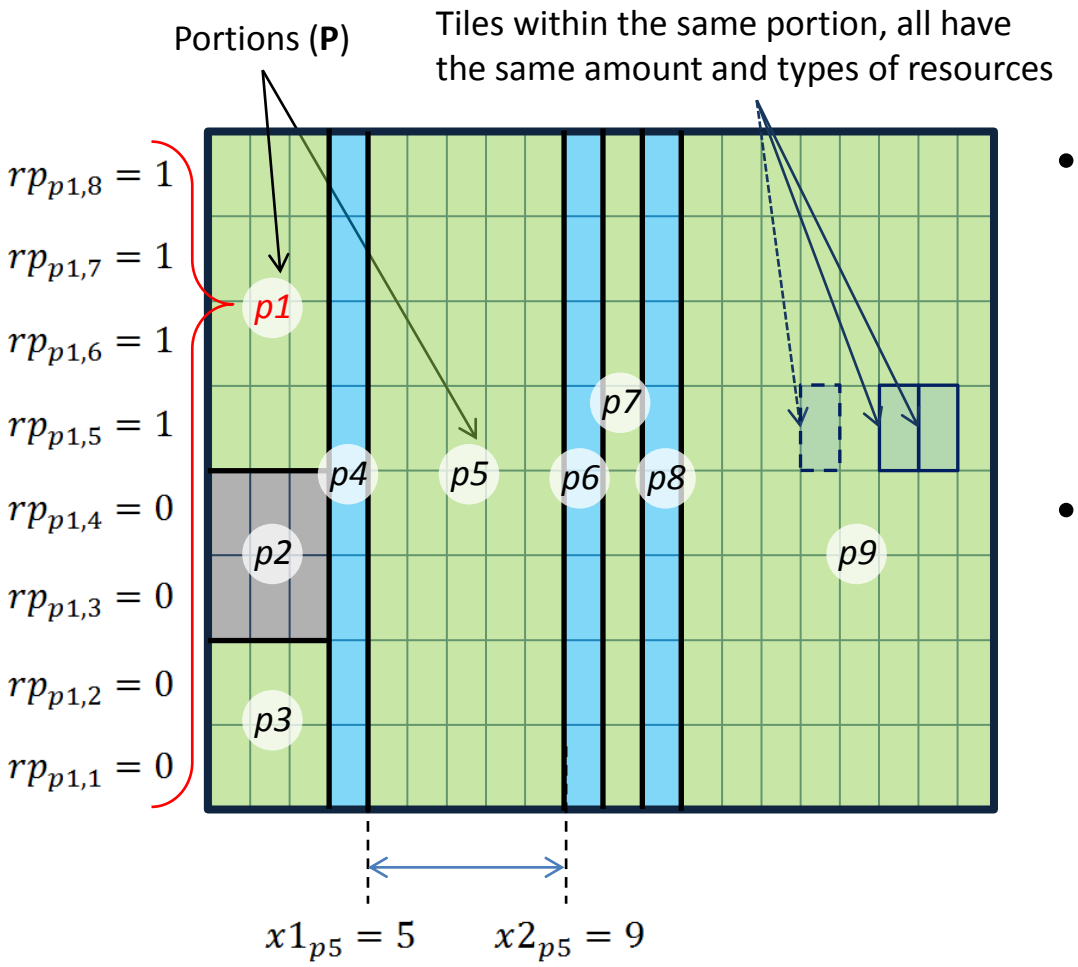
Heuristic solution

RR1 above RR2
RR1 above RR3
RR2 at the left of RR3

$$yl_{n1} \geq yl_{n2} + h_{n2}$$
$$yl_{n1} \geq yl_{n3} + h_{n3}$$
$$x_{n1} + w_{n1} \leq x_{n2}$$

Geometrical constraints
Added to the MILP model

Covered resources - I



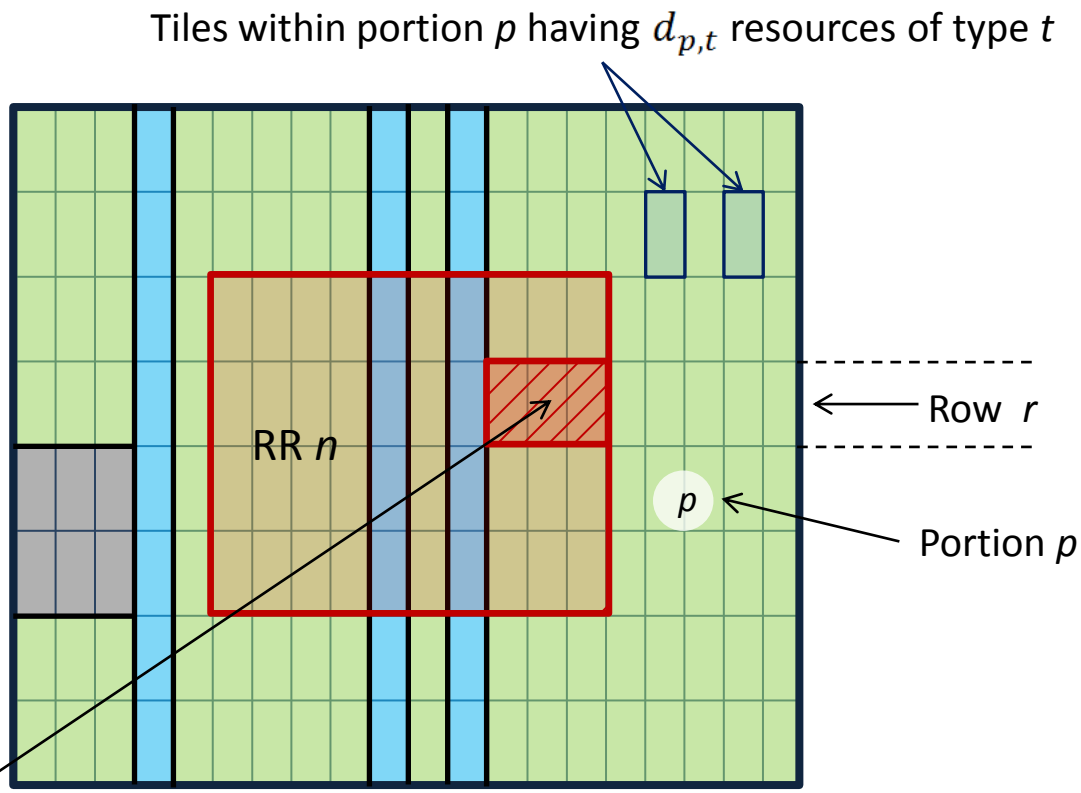
- FPGA partitioning
  - Reduce model complexity
  - **P**: set of portion describing the device
  - **T**: set of resource types
- Parameters

$x1_p$ leftmost pos. of portion **p**

$x2_p$ rightmost pos. of portion **p**

$rp_{p,r}$ { = 1 if portion **p** lies on row **r**; = 0 otherwise

Covered resources - II

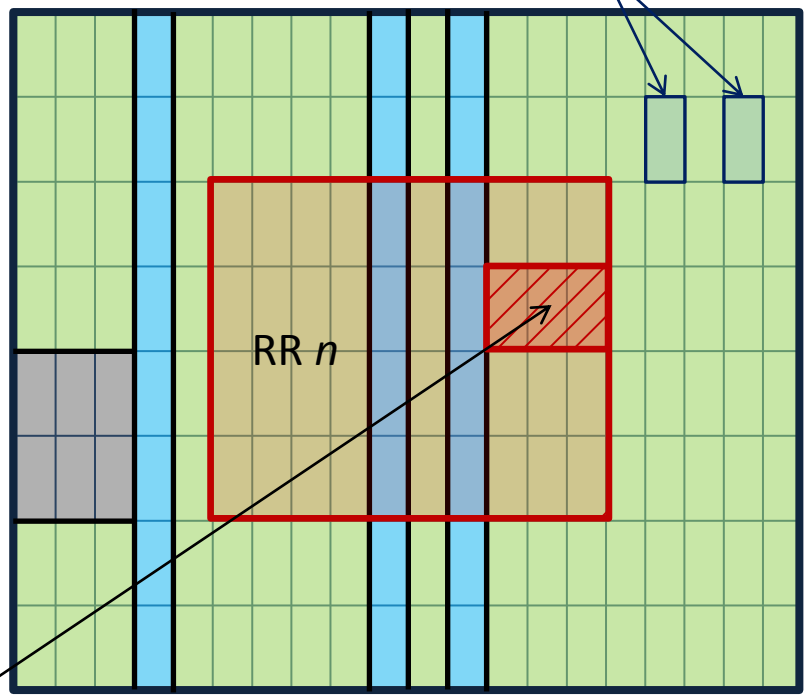


$l_{n,p,r} = 3$ (intersection between region *n* on portion *p* and row *r* measured in tiles)

$l_{n,p,r} \cdot d_{p,t}$ = resources of type *t* covered by region *n* on portion *p* and row *r*

Covered resources - III

Tiles within portion *p* having $d_{p,t}$ resources of type *t*



Resource requirement constraint:

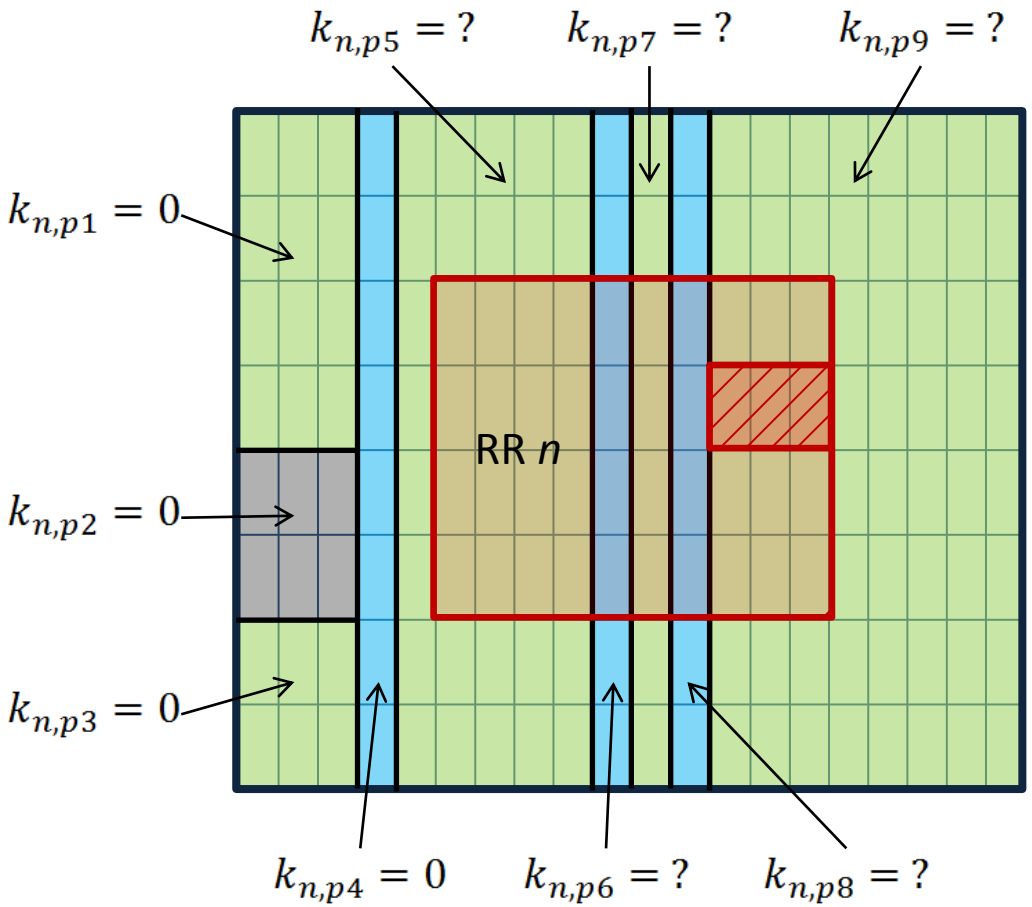
$$\forall t \in T: \sum_{p \in P, r \in R \mid rp_{p,r}=1} l_{n,p,r} \cdot d_{p,t} \geq c_{n,t}$$

$c_{n,t}$ resources of type ***t*** required by RR ***n***

$l_{n,p,r} = 3$ (intersection between region *n* on portion *p* and row *r* measured in tiles)

$l_{n,p,r} \cdot d_{p,t} =$ resources of type *t* covered by region *n* on portion *p* and row *r*

Covered resources - IV



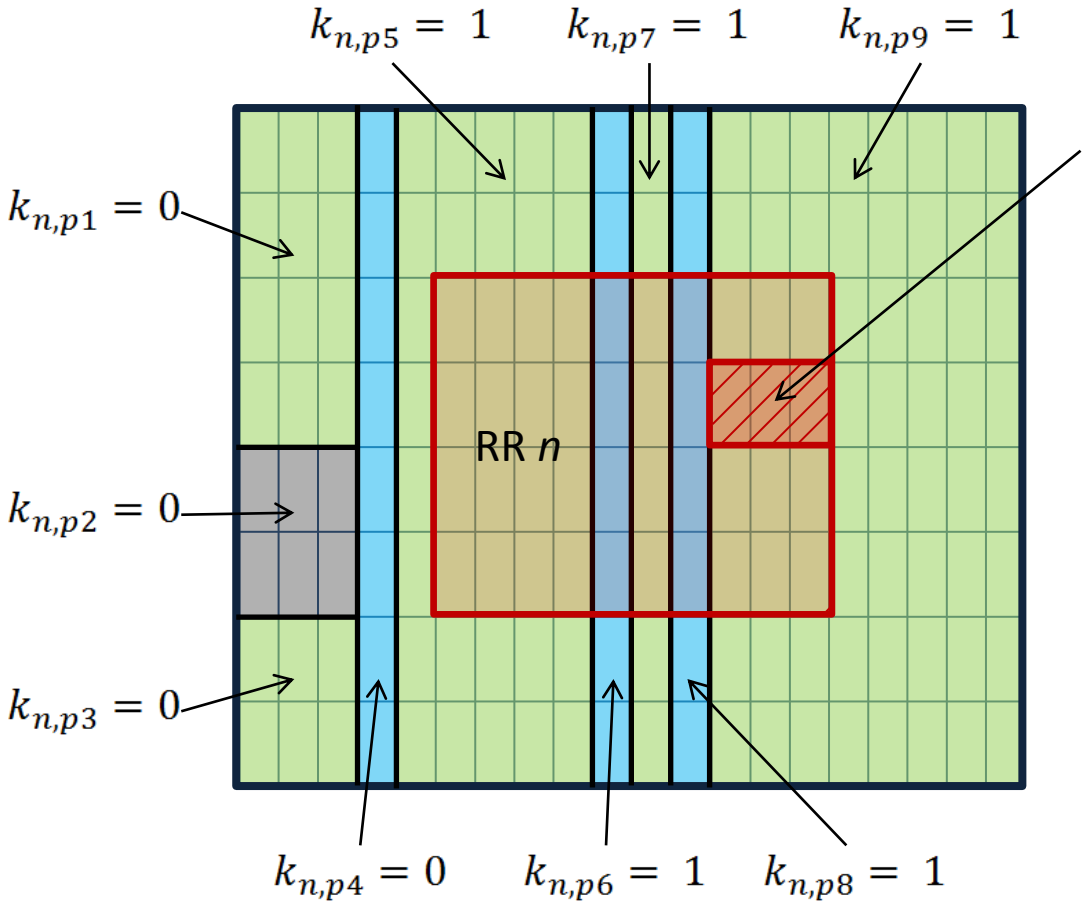
$$k_{n,p} \in \{0,1\}$$

Binary variable forced to 0 if region ***n*** is on the left or on the right of portion ***p***

$$x_n + w_n - 1 \geq x1_p \cdot k_{n,p}$$

$$x_n \leq x2_p + (1 - k_{n,p}) \cdot maxW$$

Covered resources - V



$$l_{n,p,r} \in \mathbb{R}^+$$

intersection between region ***n*** on portion ***p*** and row ***r*** measured in tiles

$$\forall n \in N, p \in P, r \in R | rp_{p,r} = 1:$$

$$l_{n,p,r} \leq a_{n,r} \cdot (x2_p - x1_p + 1)$$

$$l_{n,p,r} \leq k1_{n,p} \cdot (x2_p - x1_p + 1)$$

$$l_{n,p,r} \leq w_n$$

$$l_{n,p,r} \leq x_n + w_n - k_{n,p} \cdot x1_p$$

$$l_{n,p,r} \leq x2_p - x_n + 1 + (1 - k_{n,p}) \cdot maxW$$

$$\forall n \in N, r \in R:$$

$$\sum_{p \in P | rp_{p,r} = 1} l_{n,p,r} \geq w_n - (1 - a_{n,r}) \cdot maxW$$

Objective function

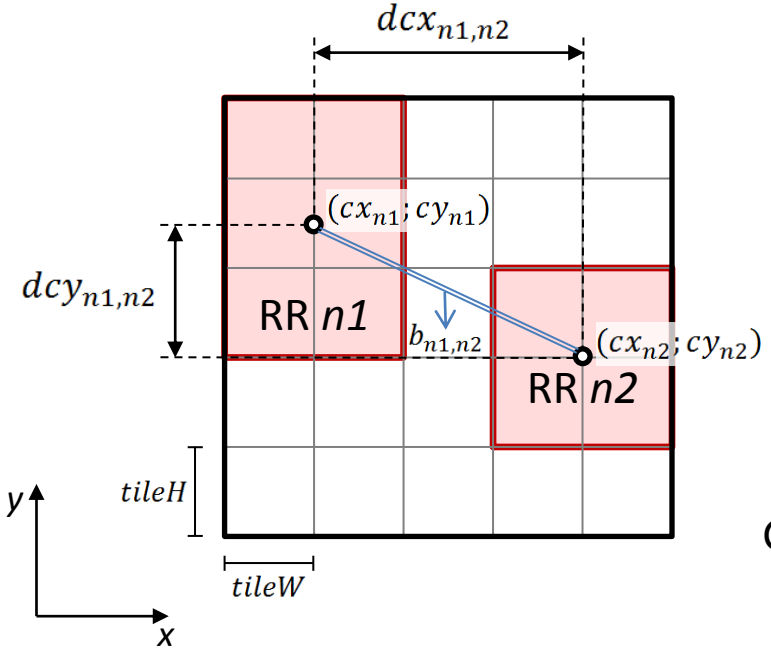
- Cost function can be defined starting from the variables and parameters of the MILP model

- Implemented metrics:
  - Global wirelength measured using HPWL (WL_{cost})
  - Regions perimeter (P_{cost})
  - Wasted resources (R_{cost})

- $$min\left\{q_1 \cdot \frac{WL_{cost}}{WL_{max}} + q_2 \cdot \frac{P_{cost}}{P_{max}} + q_3 \cdot \frac{R_{cost}}{R_{max}}\right\}$$

Objective function – Example I

- Internal Wirelength
  - Measured with HPWL (half-perimeter wirelength)
  - $b_{n1,n2}$: number of interconnections between regions *n1* and *n2*



$$cx_n = tileW \cdot (x_n + w_n/2)$$
$$cy_n = tileH \cdot (yl_n + h_n/2)$$

$$dcx_{n1,n2} \geq cx_{n1} - cx_{n2}$$
$$dcx_{n1,n2} \geq cx_{n2} - cx_{n1}$$

$$dcy_{n1,n2} \geq cy_{n1} - cy_{n2}$$
$$dcy_{n1,n2} \geq cy_{n2} - cy_{n1}$$

Geometrical constraints

$$WL_{cost} = b_{n1,n2} \cdot (dcx_{n1,n2} + dcy_{n1,n2}) + \cdots$$

Cost to be minimized

Objective function – Example II

- Wasted resources
  - Measures the number of resources occupied by not needed
  - rc_t : cost of wasting a resource of type *t*

$$R_{cost} = \sum_{n \in N, t \in T} waste_{n,t} \cdot rc_t$$

$$waste_{n,t} := \sum_{p \in P, r \in R | rp_{p,r}=1} (l_{n,p,r} \cdot d_{p,t}) - c_{n,t}$$

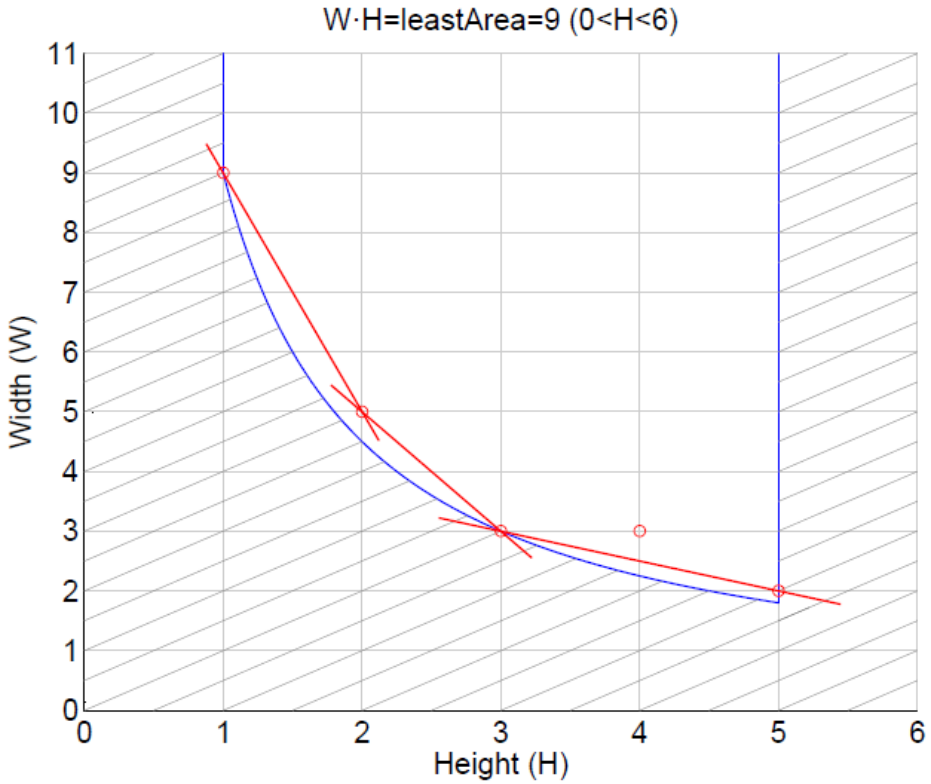
T = {CLB, BRAM, DSP}

Covered *t* resources

Required *t* resources

Formulation refinement

- Additional constraints to better describe the solution space of the LP (Linear Programming) relaxation



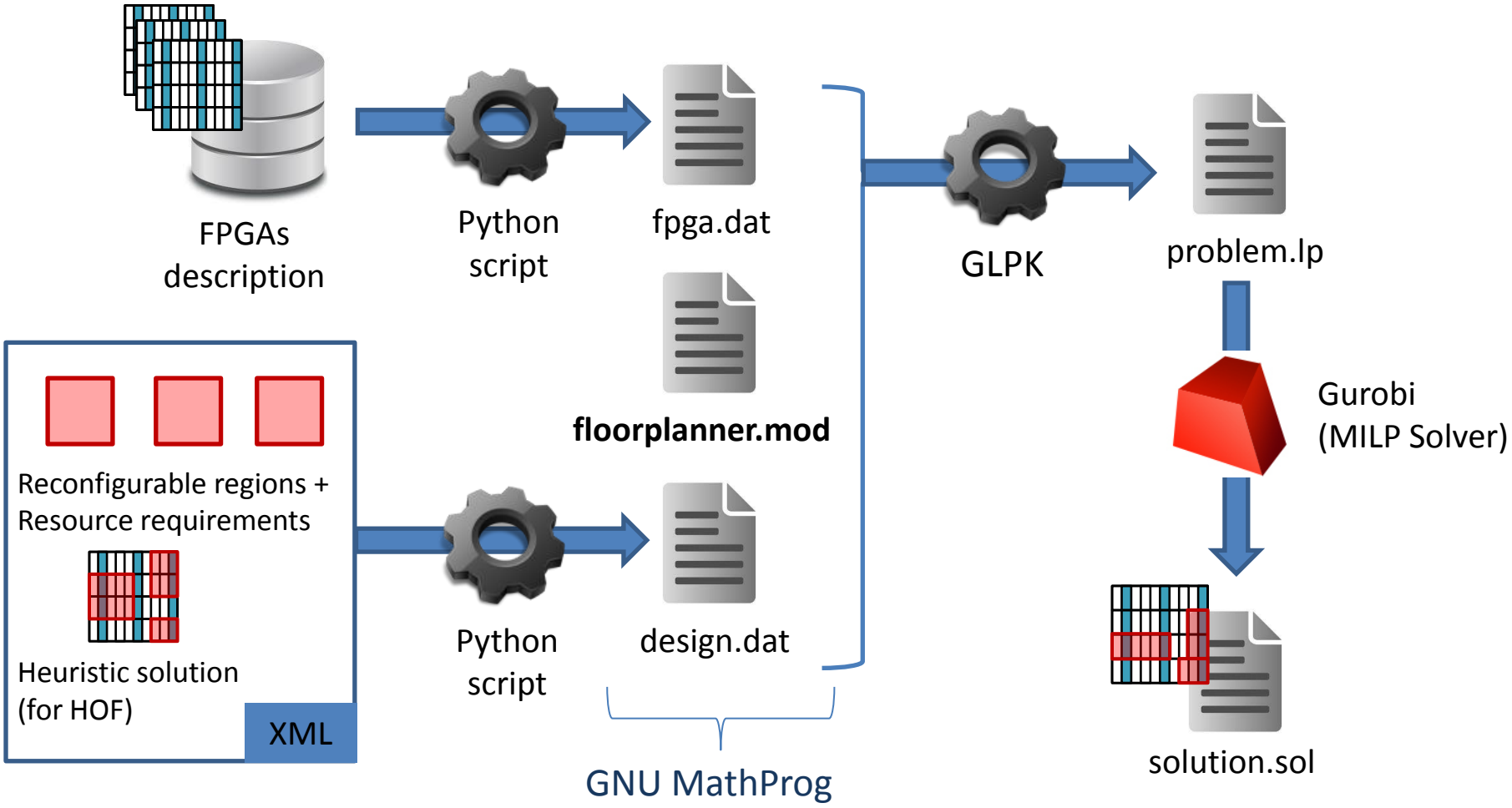
<u>For a given region n:</u>

$$leastArea := \max_{t \in T} \left\lceil \frac{c_{n,t}}{maxD_t} \right\rceil$$

$$w_n \cdot h_n \geq leastArea$$

$maxD_t =$ Maximum number of t resources within a tile

Implementation



OVERALL SYSTEM EVALUATION

Pseudo-random benchmark

- 20 designs with different number of regions and different device occupancy rate to test effectiveness
  - At least 1 or 2 regions requiring DSPs
  - From 3 to 7 regions requiring BRAMs
  - Random interconnections between regions and to the IO
  - Target device: Virtex-5 XC5VLX110T
- Global wirelength objective function to compare to Bolchini et al. [*]
  - 10 random executions of [*], best outcome considered
  - HOF re-optimization on [*] good solutions (within 10% of the best one)
  - OF warm started using HOF solution and execution time limited to 1800 sec.

[*] Bolchini, C., Miele, A., and Sandionigi, C.: Automated Resource-Aware Floorplanning of Reconfigurable Areas in Partially-Reconfigurable FPGA Systems. In FPL, pages 532-538, 2011.

benchmark results - I

# Regions	Average wirelength improvement w.r.t. [*]		Average execution time (sec)		
	HOF	OF	[*]	HOF	OF
5	6.99%	7.48%	10.9	12.9	56.0
10	7.59%	11.65%	23.8	45.3	1845.3
15	8.88%	20.06%	40.6	69.6	1869.7
20	5.47%	19.13%	64.9	83.3	1883.4
25	5.67%	21.97%	93.2	121.0	1921.0

[*] Bolchini, C., Miele, A., and Sandionigi, C.: Automated Resource-Aware Floorplanning of Reconfigurable Areas in Partially-Reconfigurable FPGA Systems. In FPL, pages 532-538, 2011.

benchmark results - II

Occupancy	Average wirelength improvement w.r.t. [*]		Average execution time (sec)		
	HOF	OF	[*]	HOF	OF
70%	8.51%	19.19%	47.0	89.2	1544.1
75%	5.49%	21.50%	46.8	62.7	1509.3
80%	6.20%	13.80%	46.7	59.2	1506.9
85%	7.48%	9.75%	46.3	54.6	1500.0

[*] Bolchini, C., Miele, A., and Sandionigi, C.: Automated Resource-Aware Floorplanning of Reconfigurable Areas in Partially-Reconfigurable FPGA Systems. In FPL, pages 532-538, 2011.

Floorplanners features comparison

Authors	Resource distribution aware	Compliant with PR	Customizable objective function	Reaches the optimum
Montone et al.	No	Yes	No	No
Bolchini al.	Yes	Yes	No	No
Vipin et al.	**Yes**	**Yes**	**Limited, biased towards area**	**No**
HOF	Yes	Yes	Yes	No
OF	Yes	Yes	Yes	Yes

The case study

- SDR (Software Defined Radio) taken from [*]
  - 5 reconfigurable regions
  - Heterogeneous resource requirements
  - Multiple modules assigned for each region
  - Sequential connections among regions with equal bandwidth
  - Target device: Virtex-5 FX70T
- Objective:
  1. Wasted frames
  2. Wirelength

[*] Vipin, K. and Fahmy, S. A.: Architecture-aware reconfiguration-centric floorplanning for partial reconfiguration. In ARC, pages 13-25, 2012.

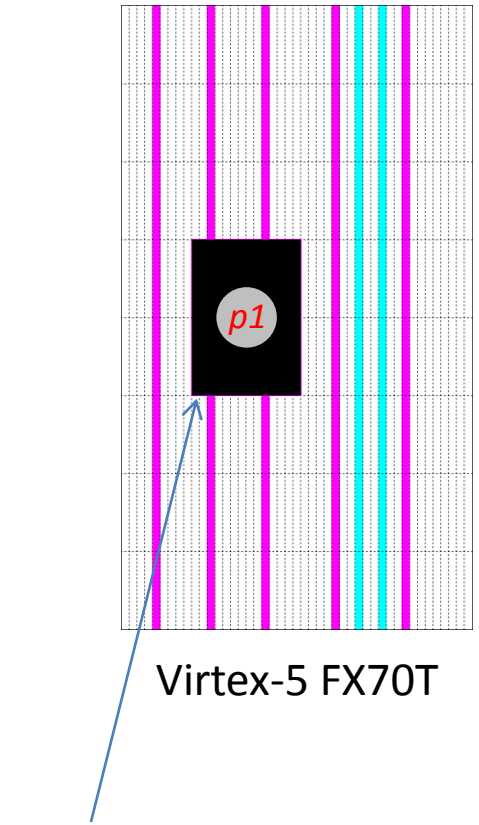
SDR resource requirements

Region	CLB tiles	BRAM tiles	DSP tiles	# Frames
Matched Filter	25	0	5	1040
Carrier Recovery	7	0	1	280
Demodulator	5	2	0	240
Decoder	12	1	0	462
Video Decoder	55	2	5	2180
Total	104	5	11	4202

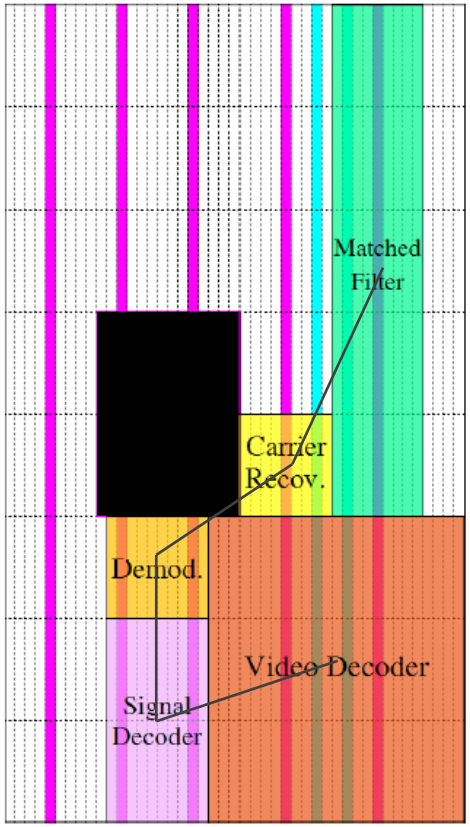
[*] Vipin, K. and Fahmy, S. A.: Architecture-aware reconfiguration-centric floorplanning for partial reconfiguration. In ARC, pages 13-25, 2012.

The proposed solution

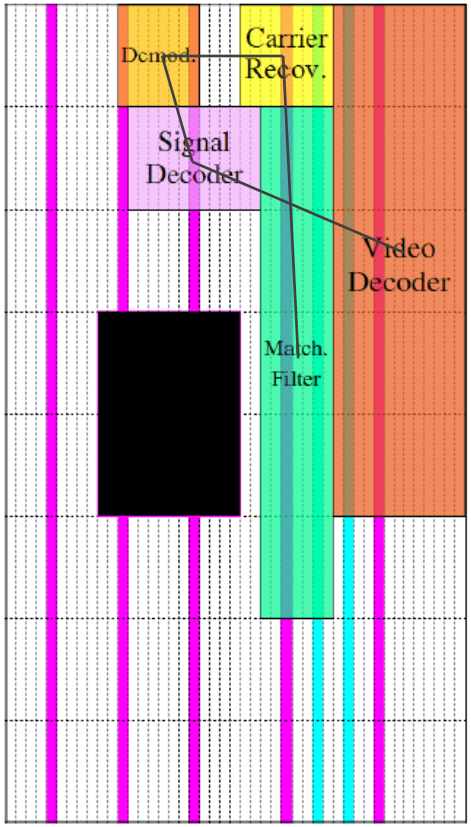
- Optimization via OF
  - Small number of regions (5)
  - We assume heuristic solution not available
- Objective parameters (same optimization)
  - $q_1 = 1;\ q_2 = 0;\ \ q_3 = R_{max}$
  - $min\left\{q_1 \cdot \frac{WL_{cost}}{WL_{max}} + q_2 \cdot \frac{P_{cost}}{P_{max}} + q_3 \cdot \frac{R_{cost}}{R_{max}}\right\}$
- Additional constraint to prevent intersection with the hard processor on the FPGA
  - $\forall n \in N, r \in R:\ l_{n,p1,r} = 0$



Solution comparison



Floorplan produced by [*].



Floorplan produced by OF.

- Optimal solution in 29 seconds
- 34% wasted frames reduction
  - No DSP and CLB wasted by the Video Decoder RR
  - No BRAM wasted by the Signal Decoder RR
- Approximately same wirelength

[*] Vipin, K. and Fahmy, S. A.: Architecture-aware reconfiguration-centric floorplanning for partial reconfiguration. In ARC, pages 13-25, 2012.

Conclusion

- Two approaches for the identification of area constraints on partially-reconfigurable FPGA have been introduced

- Novelties:
  - Consider arbitrary distribution of heterogeneous resources
  - Possibility to customize the objective function
  - Control on the quality of the desired solution

- Results published at FCCM 2014:
  - Rabozzi, M., Lillis, J., and Santambrogio, M. D.: Floorplanning for Partially-Reconfigurable FPGA Systems via Mixed-Integer Linear Programming. In FCCM, 2014.

Future work

- Enhance the description of the MILP model
- Consider alternative approaches between OF and HOF
  - Sequential K-placement (fix the position of k regions at a time)
  - Hierarchical floorplanning
- Consider other metrics
  - power consumption
  - provide support for bitstream relocation

DEMO

THANK YOU!

Available at: http://floorplacer.necst.it