

# Volatile Organic Compound Detection Using Insect Odorant-Receptor Functionalised Field-Effect Transistors

by

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# 1. Fabrication of Carbon Nanotube Network and Graphene Field-Effect Transistors

This chapter discusses the fabrication processes for both the carbon nanotube network and graphene transistors. Experimental optimisation of the transducer element is critical for biosensor work, and large numbers of transducers were required for testing various biosensor functionalisation processes. Therefore, these processes were developed to rapidly fabricate devices with reproducible device characteristics appropriate for biosensing work. Also outlined in this chapter are the characterisation techniques taken to test the quality and reproducibility of these fabrication processes.

The nitrogen ( $\geq 99.99\%$ ) and oxygen (99.7%) used in fabrication work was supplied by BOC Limited New Zealand. All acetone and isopropanol used for wafer/device processing had a minimum 99.9% purity (HPLC grade). Deionised (DI) water was taken from a Synergy<sup>®</sup> UV Water Purification System. The DI water had a measured conductivity of  $(1.4 \pm 0.1) \mu\text{S cm}^{-1}$ , compared to tap water with a measured conductivity of  $(7.8 \pm 0.2) \mu\text{S cm}^{-1}$ .

## 1.1. Deposition of Carbon Nanotubes

4-inch *p*-type (B-doped) silicon wafers with either a 100 nm or 300 nm SiO<sub>2</sub> layer (Wafer-Pro LLC) were used as the substrate for carbon nanotube network deposition. Devices intended for backgated measurements were fabricated with a 100 nm SiO<sub>2</sub> layer. Before deposition of carbon nanotubes, the wafers were spin-coated with AZ<sup>®</sup> 1518 photoresist, placed photoresist-side down onto a cleanroom wipe, fixed in place using vacuum suction, then cleaved into quarters using a diamond-tipped scribe tool.

For fabrication performed before June 2023, the protective photoresist layer was then removed by soaking the quarter-wafers in acetone for 15 minutes, then rinsed with isopropyl alcohol (IPA) and dried with N<sub>2</sub> gas. However, for complete removal of photoresist, we found it was necessary to flood expose the wafer with the Karl Suss Aligner for 1 min and then place it in AZ326 developer for 3 min, as discussed further in [?@sec-photoresist-contamination](#).

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Carbon nanotubes were deposited before alignment markers photolithography on all wafers fabricated between Aug 2021–Feb 2023, while devices fabricated before Aug 2021 and after Feb 2023 had alignment markers photolithography performed before the deposition of carbon nanotubes. The process order was first switched in Aug 2021 as this order led to faster processing times. However, the order was switched back in Feb 2023 to minimise the exposure of carbon nanotubes to photolithographic chemical processes.

### **1.1.1. Solvent-Based**

The solvent-based deposition process for the carbon nanotube network in the second fabrication protocol is as follows. 10 mg of 2-mercaptopurine (99%, Sigma-Aldrich) was dissolved in 1 ml ethanol by sonication until clear. Quarter wafers were sonicated in acetone for 3 min, then exposed to O<sub>2</sub> plasma at 100 W for at least 2 min in a small plasma cleaner (Plasma Etch, Inc., PE-50 Compact Benchtop Plasma Cleaning System) or reactive ion etcher (Oxford Instruments, Plasmalab® 80 Plus) under 300 mTorr pressure. The cleaned SiO<sub>2</sub>/Si surface was then coated with 2-mercaptopurine for 10 minutes, rinsed with ethanol to remove residual 2-mercaptopurine, and then nitrogen dried.

Meanwhile, 5 μ g of 99% semiconducting carbon nanotube bucky paper (NanoIntegris, IsoNanotubes S-99) was dispersed in 10 mL of anhydrous 1,2-dichlorobenzene (Sigma Aldrich) by ultrasonication until no particles were visible to the naked eye. During this time, the ultrasonic bath temperature was kept between 20 – 30°C or the buckypaper would not disperse successfully. The substrates were then placed into a dish with CNT-DCB suspension and left covered for 1 hour, dipped into ethanol for 10 min to remove residual solvent and any unattached carbon nanotube bundles, and then dried with nitrogen.

### **1.1.2. Surfactant-Based**

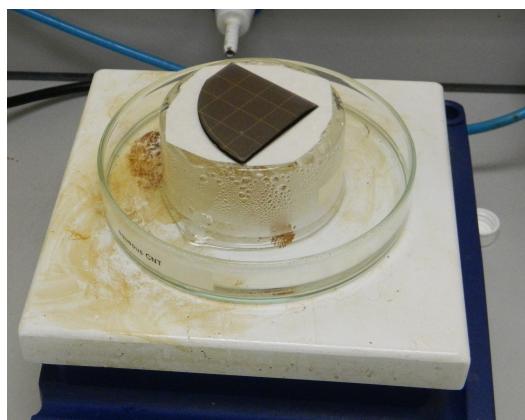
Two different approaches were used to attach the surfactant-dispersed CNTs. The composition of the surfactant used in the dispersion is proprietary to NanoIntegris. In both approaches, the quarter wafers were rinsed with ultrapure deionised water (DI water), acetone and IPA before being placed into a reactive ion etcher (Oxford Instruments, Plasmalab 80 Plus) and exposed to O<sub>2</sub> plasma at 100 W for at least 2 min in a small plasma cleaner (Plasma Etch, Inc, PE-50 Compact Benchtop Plasma Cleaning System) or reactive ion etcher (Oxford Instruments, Plasmalab 80 Plus) under 300 mTorr pressure to make the surface hydrophilic. 1 mL of poly-L-lysine (PLL) was immediately deposited onto each quarter wafer and left for 5 minutes. The quarter wafers were then rinsed for 30 s with DI water and dried with N<sub>2</sub> gas. This process allows for the surface adhesion of semiconducting single carbon nanotubes suspended in surfactant.

## 1.1. Deposition of Carbon Nanotubes

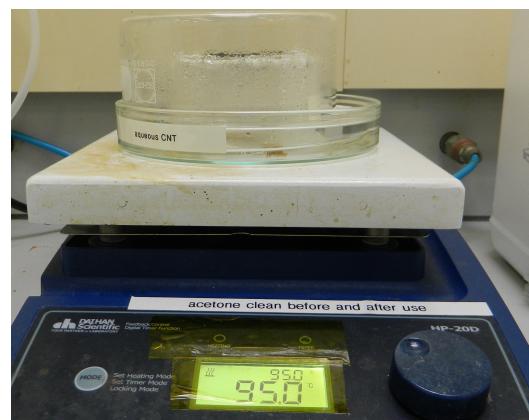
### Simple Dropcasting

2 mL of IsoNanotubes-S 90% or 99% solution (NanoIntegris) was decanted into a small bottle and sonicated for 5 s to break up bundles of CNTs. An even spread of 400  $\mu$ L CNT solution was placed in the centre of the PLL-functionalised quarter wafer, covered and left for 10 minutes. The CNT solution was then rinsed off with DI water and IPA, and then the quarter wafer was dried with N<sub>2</sub> gas. Next, the quarter wafer was annealed in a vacuum oven at 150° C for 1 hour to remove residual surfactant. This method would often lead to an inhomogeneous spread of CNTs across the quarter wafer surface, detailed further in section ?@sec-cnt-deposition-effects.

### Steam-Assisted Method



(a) Steam method setup without steam cover



(b) Steam method setup with steam cover

Figure 1.1.: Photographs of steam-assisted method setup (top and side view).

2 mL of IsoNanotubes-S 90% or 99% solution (NanoIntegris) was decanted into a small bottle and burst-sonicated once (on then off again) to break up bundles of CNTs. 75 mL of 95° C water was then placed into a glass dish on a hotplate held at 95° C. After this, the PLL-functionalised quarter wafer was placed in the centre of an insulating surface on the same hotplate. The CNT dispersion was carefully spread across the surface of the wafer without spilling any over the wafer edges. The wafer on the insulating surface and glass dish were then left under the same cover for 2 minutes to expose the wafer to steam from the glass dish. The use of an insulating surface meant that the wafer and CNT dispersion were not heated from below while exposed to steam. The steam-assisted deposition setup is shown in Figure 1.1.

The CNT dispersion was then rinsed off the wafer with DI water, ethanol, acetone and IPA, and then the quarter wafer was dried with N<sub>2</sub> gas. As in the original method, the quarter wafer was then annealed in a vacuum oven at 150° C for 1 hour to remove residual surfactant. This method gave an even spread of CNTs across the quarter wafer

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surface, leading to a greater consistency in performance between devices. Further details can be found in ?@sec-cnt-deposition-effects.

### 1.2. Photolithography for Carbon Nanotube and Graphene Field-Effect Transistors

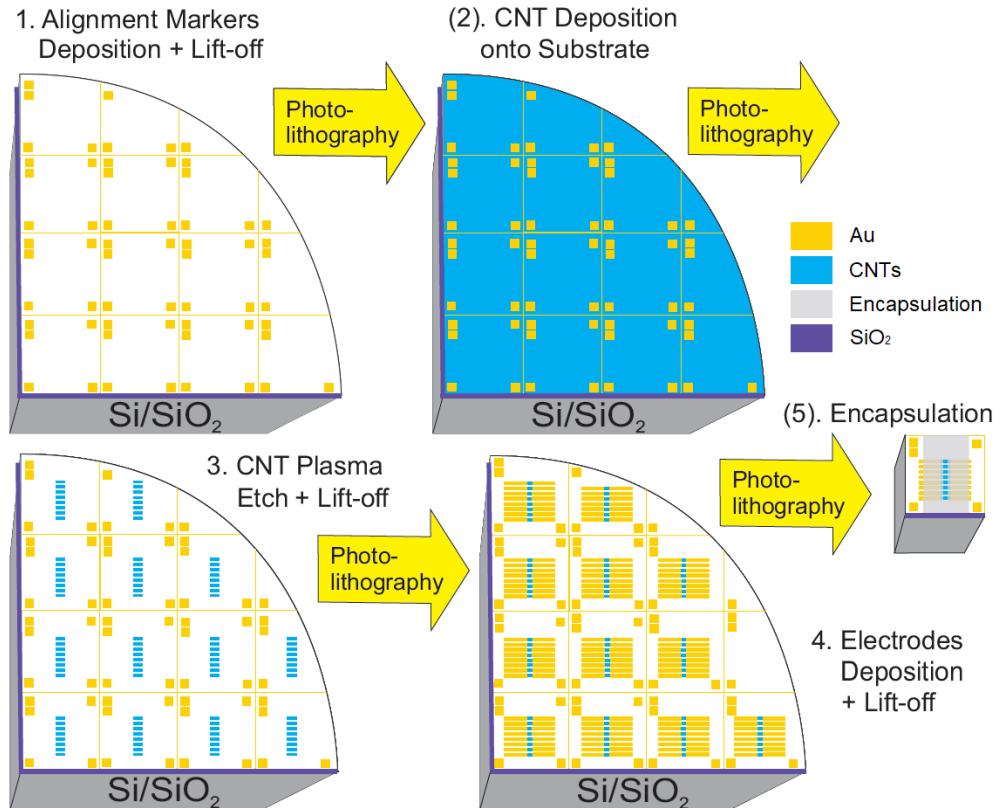


Figure 1.2.: The photolithographic processes used for fabrication of both carbon nanotube and graphene devices (graphene devices were fabricated individually for every step, step #2 skipped for graphene devices)

Photolithography was used to define eight channel regions on each device and subsequently to define metal contacts for each of these channels. A schematic demonstrating these photolithography processes on a quarter wafer is shown in Figure 1.2. Masks for photolithography were designed in-house using LayoutEditor CAD software and patterned externally with a UV laser writer.

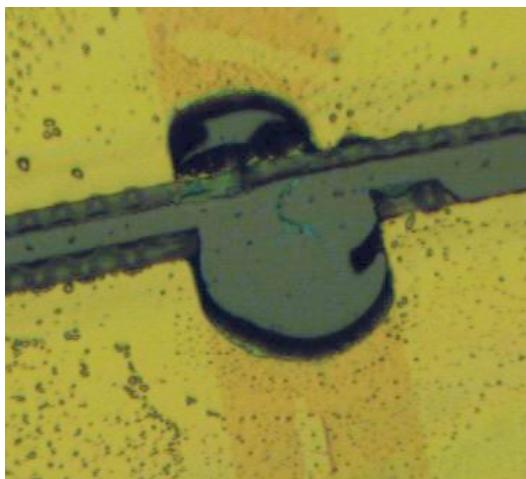
Thermal evaporation was used when depositing chromium (Cr-plated tungsten rods, Kurt J. Lesker) and gold (Au wire, 99.99%, Regal Castings Ltd.), while electron beam evaporation was used when depositing titanium (Ti pieces, 99.99%, Kurt J. Lesker) and

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metal oxides (*e.g.* Al<sub>2</sub>O<sub>3</sub> pieces, 99.99%, Kurt J. Lesker). Metal and metal oxide deposition was performed using an Angstrom Engineering Nexdep 200 Vacuum Deposition System. Deposition thickness was controlled using an Inficon Deposition Controller and electron beam power was provided by a Telemark TT-6 power supply. For metals, the chamber was initially evacuated to a pressure  $5 \times 10^{-6}$  mTorr, while for metal oxides the chamber was initially evacuated to a pressure of  $1 \times 10^{-5}$  mTorr. After evaporation, the chamber was cooled and vented with nitrogen.

Carbon nanotube network field-effect transistors were fabricated using the quarter wafer substrates discussed in Section 1.1.

Graphene field-effect transistors were fabricated using 300 nm SiO<sub>2</sub>/p-type Si substrates covered with a monolayer of mechanically transferred CVD graphene (Advanced Chemical Supplier). This substrate was cleaved into equal-sized square chips before photolithography, with side length between 11.6 – 11.7 mm, subject to variability in wafer size. The same cleaving process outlined in Section 1.1 was used for cleaving the chips, but the photoresist was not rinsed off after cleaving. Devices were exposed to a brief burst of N<sub>2</sub> gas to remove any dust from the cleaving process from the surface of devices. When not being used in photolithography, graphene-based devices were stored in a vacuum desiccator to prevent the quality of the graphene deteriorating with exposure to air over time. The limited adhesion of graphene to the wafer meant that photolithographic processing had to be performed particularly carefully when fabricating graphene devices.



(a) Damage to gold electrode in channel region after DMSO lift-off



(b) Damage to graphene (blue region) after DMSO lift-off

Figure 1.3.: Lift-off with dimethyl sulfoxide sometimes led to damage to regions where nanomaterials were present.

Dimethyl sulfoxide (DMSO) was sometimes used in lift-off processes instead of acetone between Jul 2021 and Feb 2023 because of its effectiveness as a photoresist stripping agent. However, it was abandoned due to some indications it was too aggressive for

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the devices being fabricated, as shown in Figure 1.3 and also as detailed in ?@sec-cnt-deposition-effects. It is possible that heat from the electrodes deposition sometimes crosslinked residual photoresist on the nanomaterial, and then during lift-off was removed aggressively together with any attached nanomaterial by the DMSO. However, it is also possible that prolonged exposure to DMSO alone was sufficient to detach nanomaterial from the substrate. Therefore, acetone was the preferred agent for lift-off despite being a less efficient stripping agent than DMSO.

From Jul 2023 onwards, after each photolithography step using negative resist, quarter wafers/chips placed in AZ® 326 or SU8 developer for 3 min to ensure complete removal of photoresist residue. For each step with positive resist, the same procedure was performed but with a flood exposure with UV light for 1 min before being placed in developer. The exception to this rule was for devices with an aluminium oxide layer present. Tetramethylammonium hydroxide (TMAH), the active ingredient of AZ® 326, etches through aluminium oxide and causes electrical shorts through the dielectric layer [1], [2]. A further discussion showing the results of this process is given in ?@sec-photoresist-contamination.

### **1.2.1. Alignment Markers**

Metal alignment markers were deposited in order to accurately align the device channels with device electrodes in subsequent photolithography steps. These alignment markers were asymmetric to indicate the orientation of the device for subsequent photolithography steps and electrical characterisation. In later discussion, channel 1 is defined as the channel placed closest to the large, double square alignment marker.

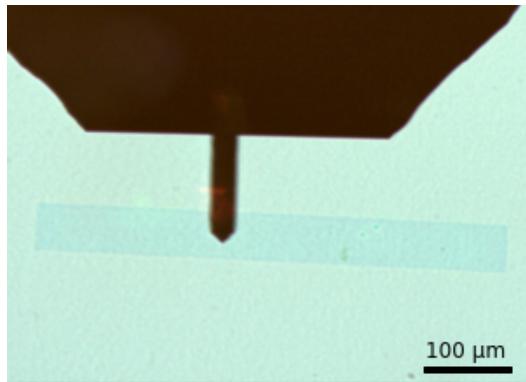
For carbon nanotube quarter wafers, alignment markers were deposited either directly before or after carbon nanotube deposition (see Section 1.1 for discussion). For graphene devices, alignment markers were deposited directly after cleaving using the protective photoresist layer spincoated prior to cleaving. AZ® 1518 was used for alignment marker photolithography.

For carbon nanotube devices made before Jun 2022, chromium was used as an adhesive layer for gold, while for all graphene devices and carbon nanotube devices made after Jun 2022, titanium was used as the adhesive layer. For chromium/gold depositions, a nominal 10 nm of chromium was deposited followed by a nominal 100 nm Au layer. For titanium/gold depositions, a nominal 10 – 20 nm of titanium was deposited followed by a nominal 50 nm Au layer (for independent measurements of metal layer thickness, see Section 1.2.3). Devices were then soaked in acetone for at least 2 hours for photoresist lift-off, washed in IPA and dried with nitrogen. The use of titanium gave rise to a cleaner lift-off and improved gold adhesion. Using a relatively thin gold layer (50 nm nominal instead of 100 nm) proved to still be clearly visible but to a cleaner lift-off.

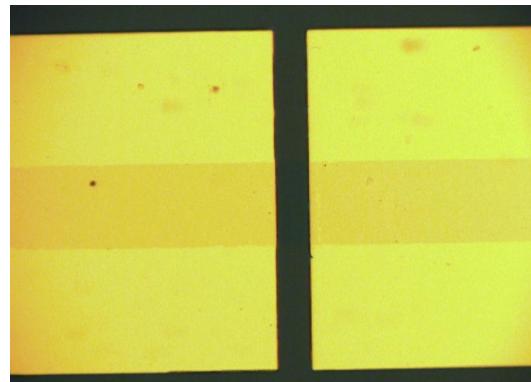
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### 1.2.2. Channel Etching

Eight channel features, each 1000  $\mu\text{m}$  in length and 100  $\mu\text{m}$  in width with a pitch of 1200  $\mu\text{m}$ , were patterned using AZ® 1518 photolithography on each carbon nanotube or graphene-covered substrate. Unwanted nanomaterial not covered with photoresist was then etched away with 200 W oxygen plasma at 600 mTorr using a reactive ion etcher or RIE (Plasmalab® 80 Plus, Oxford Instruments). The etch time was 3 minutes for carbon nanotube quarter wafers, and 1 minute for graphene chips. The protective photoresist was then removed by soaking in acetone for at least 5 minutes.



(a) Graphene channel after photolithographically defined plasma etch



(b) Graphene channel after photolithographically defined electrodes deposition and liftoff

Figure 1.4.: Microscope images of a graphene channel after plasma etch and electrodes photolithography steps.

### 1.2.3. Electrodes

The source and drain electrodes for each channel were patterned using photolithography with either AZ® 1518 photoresist (pre-Mar 2023) or AZ® nLOF 2020 photoresist (post-Mar 2023). Before metal deposition, the developed photoresist pattern was exposed to O<sub>2</sub> plasma at 50 W for up to 5 s or at 20 W for 20 – 25 s in a PE-50 plasma cleaner (Plasma Etch, Inc.) to remove residual photoresist on the developed regions and ensure a clean lift-off. After metal deposition, wafers/devices were soaked in acetone for at least 2 hours for photoresist lift-off, washed in IPA and dried with nitrogen.

As with the alignment markers deposition (see Section 1.2.1), before Jun 2022 chromium was used for the gold adhesion layer, and after Jun 2022 titanium was used. Adhesion layers are required to stick metals such as gold and platinum to silicon dioxide [3]. A 20 nm nominal titanium layer instead of 10 nm nominal was found to give better electrode adhesion, and devices after Feb 2023 were made using this thicker adhesion layer. Good

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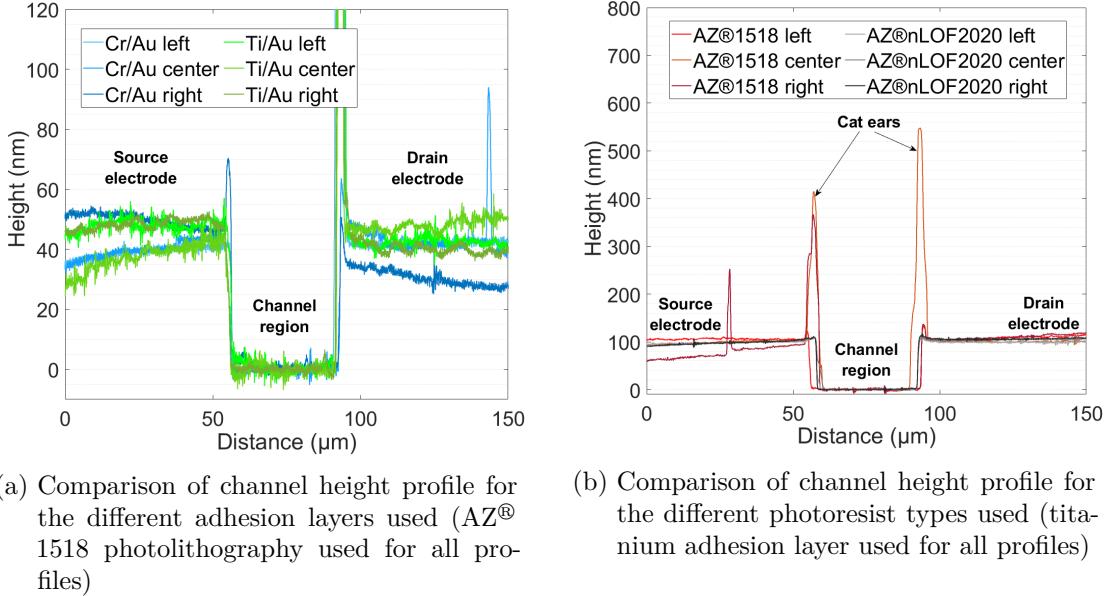


Figure 1.5.: Dektat height profiles taken between the source and drain electrodes across a channel from various quarter wafers with electrodes deposited using different approaches. For each quarter wafer, the profiles of three different channels are shown, selected from different locations across the quarter wafer surface.

electronic contact could be made with electrodes with a nominal gold layer thickness of 60 – 100 nm, and a Au layer nominally 100 nm thick was most commonly used.

Example height profiles of chromium layer channels and a titanium layer channels taken using a Veeco Dektat 150 profiler are shown in Figure 1.5a. AZ® 1518 photoresist was used here for photolithographic patterning. A 10 nm adhesion layer and 100 nm Au layer were used for both depositions to ensure a consistent comparison. From Figure 1.5a, we find an measured Cr/Au electrode height of  $42 \pm 1$  nm and an measured Ti/Au electrode height of  $48 \pm 2$  nm, slightly less than half the respective heights stated on the Inficon Deposition Controller.

Although using AZ® nLOF 2020 photolithography involves more processing steps, it gave rise to more cleanly-defined electrodes with a more consistent height profile. Often electrodes deposition using AZ® 1518 photoresist would lead to sharp vertical spikes along the edge of the electrode. These edge spikes or “cat ears” could partially or fully protrude through thin encapsulation materials such as SU8 and Al<sub>2</sub>O<sub>3</sub>, leading to significant leakage currents from the electrodes into the FET top gate. This effect is due to the profile of positive resists being suboptimal for lift-off processes, as discussed in Appendix A.

The height profiles corresponding to a wafer with electrodes fabricated using AZ® 1518 and to a wafer with electrodes fabricated using AZ® nLOF 2020 are shown in Figure 1.5b.

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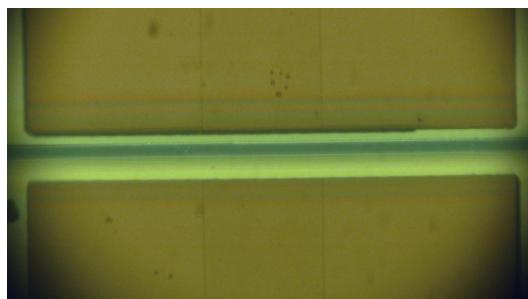
A 20 nm titanium adhesion layer and 100 nm Au layer were used for both depositions to ensure a consistent comparison, resulting in a measured electrode height of  $103 \pm 2$  nm for both wafers. The wafer which used AZ® nLOF 2020 photoresist clearly has a more consistent electrode height profile across the wafer surface than the wafer which used AZ® 1518 resist. The measured edge features for the AZ® 1518 resist electrodes vary in size from 20 nm to 450 nm above the bulk electrode surface, whereas the edge features for the AZ® nLOF 2020 resist do not exceed 14 nm in height.

### 1.2.4. Encapsulation

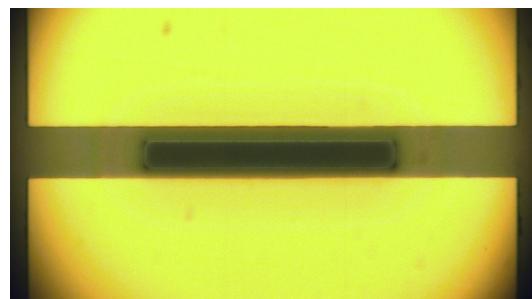
Several different approaches were used for the encapsulation, or contact protection, of devices. The encapsulation of graphene and carbon-nanotube transistors for biosensing is essential to improve transistor characteristics, passivate the electrodes and ensure only the nanomaterial region is active during biosensing, as discussed in [?@sec-biosensor-methods](#).

Before encapsulation photolithography the carbon-nanotube network quarter wafers were cleaved into individual 11 mm  $\times$  11 mm chips, using the cleaving process outlined in Section 1.1. Cleaving the devices at this step simplified mask alignment and ensured consistent thickness across photoresist encapsulated devices.

Two different photolithography masks were used for encapsulation photolithography in this work, with different exposed areas of active nanomaterial. The first mask was used for devices made before Jan 2023, and was designed to leave a region of 500  $\mu\text{m} \times 10 \mu\text{m}$  unencapsulated for each channel. The second mask was used exclusively after Jan 2023, and was designed to leave a region of 200  $\mu\text{m} \times 20 \mu\text{m}$  unencapsulated for each channel. This change was made to double the area of carbon nanotubes exposed to electrolyte while halving the area of SiO<sub>2</sub> dielectric exposed to electrolyte during aqueous sensing.



(a) Encapsulation with AZ® 1518 using pre-2023 mask



(b) Encapsulation with AZ® 1518 using 2023 mask

Figure 1.6.: Microscope images of carbon nanotube devices after encapsulation photolithography with hardbaked AZ® 1518.

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A side-by-side microscope comparison of hardbaked AZ® 1518 processed with each mask is given in Figure 1.6, while a Dektat profile comparison corresponding to Figure 1.6 is shown in Figure 1.7a. The profiles corresponding to the mask used after Jan 2023 clearly exhibit greater device-to-device consistency, partly due to the mask requiring a greater level of accuracy when aligning the encapsulation pattern with the electrode channel. The larger feature size also means development time has less of an impact on the quality of the encapsulation opening.

### Photoresist encapsulation

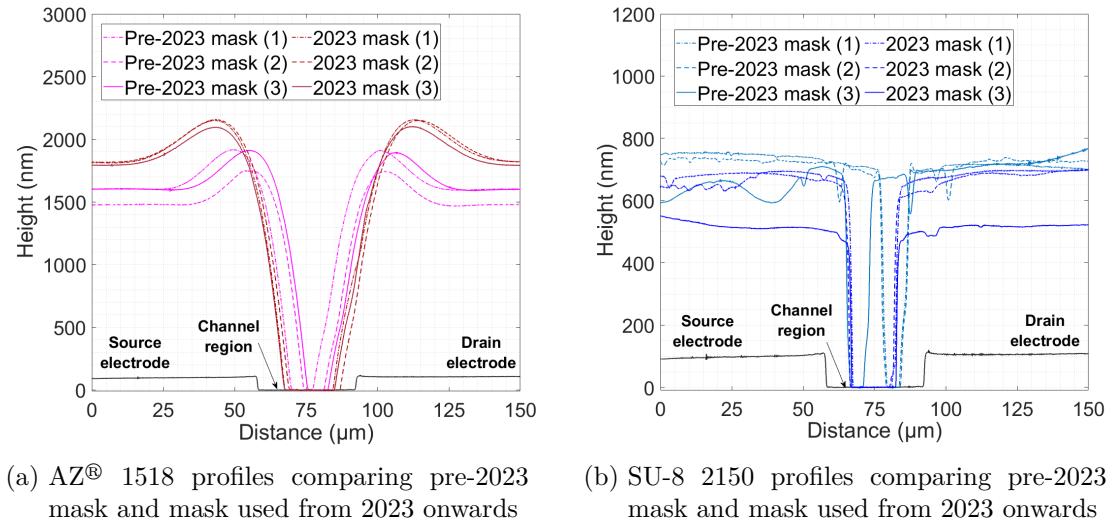


Figure 1.7.: Dektat of carbon nanotube devices after encapsulation photolithography using hardbaked AZ® 1518 and SU-8 2150, taken from various devices.

Two types of photoresist were initially trialled for encapsulation of carbon nanotube network devices, AZ® 1518 and SU8-2150. Both AZ® 1518 [4]–[6] and SU-8 have been previously used for device encapsulation, with SU-8 noted for being particularly stable and biocompatible [7]–[9].

Once developed, the photoresist pattern was exposed to O<sub>2</sub> plasma at 50 W for up to 5 s or at 20 W for 20 – 25 s to remove excess photoresist from the encapsulation opening. Devices were then hardbaked at 200°C for 1 hour to fully crosslink the encapsulation layer. This crosslinking ensured subsequent device exposure to solvent did not remove the photoresist encapsulation.

The exposed region clear of AZ® 1518 resist was  $6.8 \pm 0.3 \mu\text{m}$  in width when using the old, pre-2023 mask, while the exposed region was  $16.6 \pm 0.4 \mu\text{m}$  when using AZ® 1518 with the new mask from 2023, as seen in Figure 1.7a. However, the exposed region was reduced for the SU-8 encapsulation relative to the AZ® 1518, with an width of only  $3.6 \pm 0.5 \mu\text{m}$  for the pre-2023 mask, as seen in Figure 1.7b. Photoresist development using

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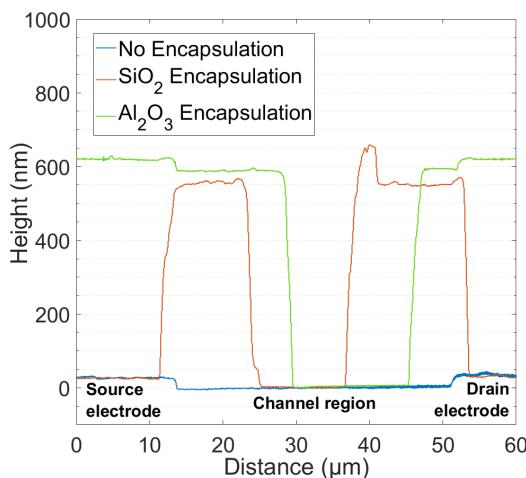
SU-8 was significantly more time-sensitive than for the AZ® 1518. This meant when the development time was increased to create a wider encapsulation opening, it was difficult to avoid removing large areas of photoresist across the surface of the encapsulation. This meant using the new mask from 2023 was especially important for maximising the exposed channel region of SU-8 devices. Using the new mask from 2023 with the SU-8 resist gave a significantly improved width of  $13.8 \pm 1.0 \mu\text{m}$  for the exposed region.

A relatively thin SU-8 encapsulation layer could be deposited when compared to the AZ® 1518 encapsulation profile. The AZ® 1518 encapsulation layer had a average height of  $1.7 \pm 0.2 \mu\text{m}$ , while the SU-8 encapsulation layer had a average height of  $680 \pm 20 \text{ nm}$ . The SU-8 also had much less significant edge features than the AZ® 1518, regardless of the profiles of the source and drain electrodes.

As noted previously, for both resists the overall profile was more consistent for the new, 2023 mask from device to device than for the old pre-2023 mask.

AZ® 1518 encapsulation was used for all graphene devices fabricated.

### Dielectric encapsulation



(a) Profile comparison of dielectric materials used for encapsulation



(b) Microscope image of channel with aluminium oxide encapsulation

Figure 1.8.: Dektat and microscope image of a device encapsulated with aluminium oxide.

Another approach taken was encapsulation of electrode channels with a dielectric metal oxide/ceramic layer. A electron beam deposition process was used to deposit a 100–150 nm nominal metal oxide layer on devices patterned with the 2023 mask using AZ® nLOF 2020 photoresist. As in Section 1.2.3, the developed photoresist pattern was exposed to O<sub>2</sub> plasma at 50 W for up to 5 s or at 20 W for 20 – 25 s in a PE-50 plasma cleaner

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(Plasma Etch, Inc.) before ceramic deposition. Before May 2023, devices were left in TechniStrip® MLO 07 (MicroChemicals) for 5 – 10 min for lift-off. However, due to concerns over the impact of the constituent chemical DMSO on the nanomaterial region (see Figure 1.3), the lift-off process was altered from May 2023 onwards. After May 2023, devices were soaked in acetone for at least 4 hours and sonicated in clean acetone for 30 – 60 s to lift-off the photoresist, then washed in IPA and dried with nitrogen.

The initial attempt at fabricating a dielectric encapsulation layer used silicon dioxide as the dielectric. However, silicon dioxide adheres poorly to gold without an metallic adhesive layer present, as shown in Figure 1.8a. Aluminium oxide was chosen as an alternative as it sticks well to bulk electrode materials, is heat and chemical resistant, has a relatively high dielectric constant and is bio-compatible [3], [9], [10]. Figure 1.8 shows the aluminium oxide successfully adhered to the electrodes and had a clean profile comparable to that of the SU-8 encapsulation layer after lift-off. As noted earlier, aluminium oxide should not be subsequently exposed to its etchant TMAH.

### **1.3. Characterisation via Atomic Force Microscopy**

Atomic force microscopy in this thesis was taken using a Nanosurf NaioAFM in dynamic force mode (also known as tapping mode, oscillating mode, acoustic AC mode or intermittent-contact mode). An ACLA probe (AppNano) was used with a tip diameter of 12 nm, height of 14 – 16  $\mu\text{m}$  and a nominal cantilever spring constant of 58 N/m. All atomic force microscopy was performed with the Nanosurf NaioAFM on a stabilising table under a Faraday cage to minimise mechanical and electromagnetic interference. A  $256 \times 256$  pixel resolution was typically used. Imaging was performed in air at room temperature.

Atomic force microscope (AFM) images could not be taken from the small exposed channel region on the encapsulated devices, so were instead taken on a representative carbon nanotube or graphene film sample fabricated on the same wafer as the device being tested. Moisture adversely affected the AFM imaging process. Therefore, films functionalised with biological materials were washed with DI water and gently dried with  $\text{N}_2$  before atomic force microscope images were taken.

The open source data analysis software Gwyddion (version 2.59) was used to analyse AFM images. This included levelling the background with the polynomial background removal function, removing scarring and zeroing the z-scale.

### **1.4. Characterisation via Fluorescence Microscopy**

Fluorescence microscopy was taken using an Olympus BX63 fluorescence microscope controlled using cellSens imaging software. Microscope objectives used were all Olym-

pus UPLSAPO/UPlanSApo, apochromat objectives which compensate for spherical and chromatic aberrations. Objectives had infinite aperture and a field number of 26.5. Filter cubes used included the Olympus FITC filter (excitation wavelength range: 467–498 nm, emission wavelength range: 513–556 nm), Texas Red (excitation wavelength range: 542 – 582 nm, emission wavelength range: 604 – 644 nm) and GFP (excitation wavelength range: 604 – 644 nm, emission wavelength range: 502 – 538 nm). The ISO was kept at the lowest available setting, ISO200. All microscopy was performed in darkness with the screen turned away from the microscope. To ensure photobleaching did not adversely affect imaging, images were taken soon after initial exposure to fluorescence and taking repeated photos of the same region was avoided. Various useful and thorough introductions to fluorescence microscopy can be found online [11], [12].

## 1.5. Electrical Characterisation

Both back-gated and liquid-gated measurements were taken of carbon nanotube and graphene devices. Liquid-gated measurements were taken using the configuration shown in Figure 1.9. Back-gated measurements were taken with a copper plane placed underneath the Si/SiO<sub>2</sub> wafer and connected to SMU 3 instead of the reference electrode.

All measurement setups used had the same basic configuration, with two source measure units (SMUs) attached to the source and gate. Voltage from the source and gate SMUs was either kept constant or varied, with only one SMU varied at a time. Three different measurement setups were used for taking these measurements, the Keysight (Agilent/HP) 4156C Semiconductor Parameter Analyser, the Keysight B1500A Semiconductor Device Analyser, and a National Instruments NI-PXIe modular measurement system with a 8 GB PXIe-8821 controller and two NI-4138 source measure units. For measurements with the Keysight instruments, a third, drain SMU was attached and kept at a constant 0 V (as shown in Figure 1.9).

When using the Keysight 4156C Semiconductor Parameter Analyser or Keysight B1500A Semiconductor Device Analyser for liquid-gated measurements, a Rucker and Kolls with micromanipulators was used to contact the devices; when using the National Instruments NI-PXIe for liquid-gated measurements, a custom-made chip carrier with spring-loaded, pointed-tip, gold-coated pogo pins was used. Ag/AgCl standard electrodes were used as the liquid-gate electrode. The electrode was submerged in 80 µL of PBS buffer in a polydimethylsiloxane (PDMS) well with outer dimensions of 12 mm × 6 mm × 6 mm. This PDMS well was sonicated in isopropanol for 10 min and thoroughly N<sub>2</sub> dried before use. The microscope images seen in Figure 1.10 show the PDMS surface before and after this cleaning step. The end of Ag/AgCl standard electrode to be submerged should be rinsed in DI water and left to sit in DI water for 15 minutes before characterisation is performed.

The Keysight 4156C Semiconductor Parameter Analyser and Keysight B1500A Semiconductor Device Analyser were also used for back-gated measurements of devices within

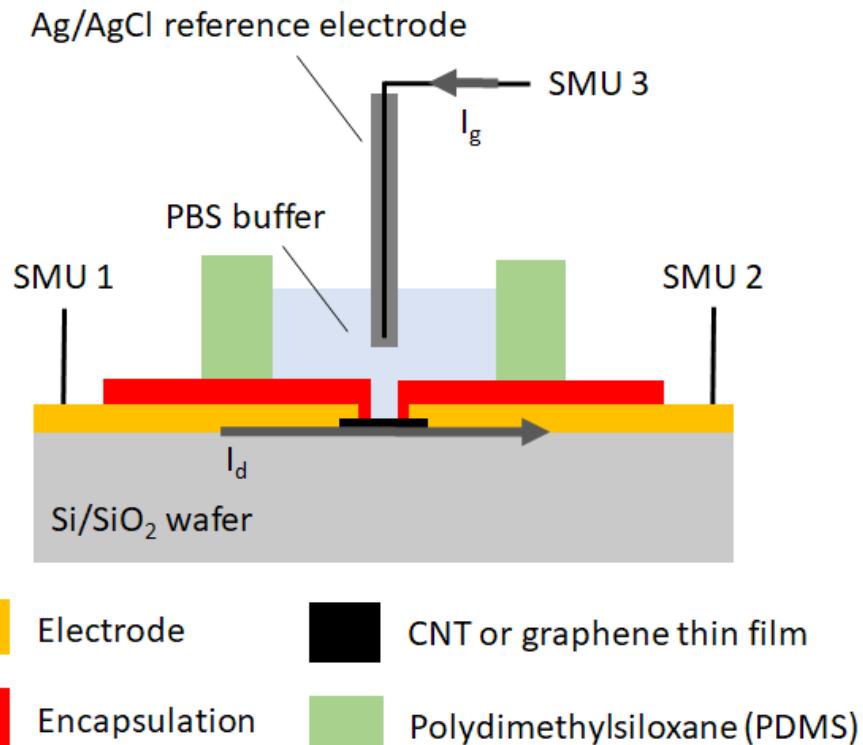
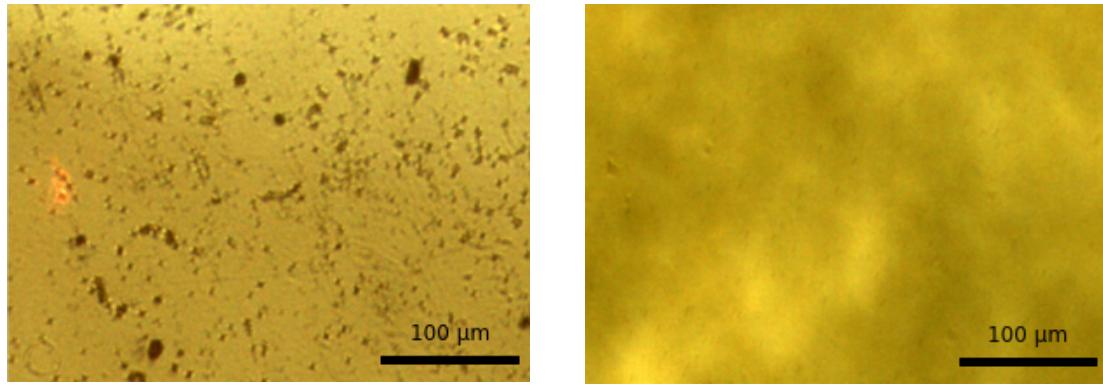


Figure 1.9.: Liquid-gated device schematic showing electrical connections to the three source measure units.  $V_{ds}$  is applied between the source SMU (SMU 1) and the drain SMU (SMU 2), while  $V_{lg}$  is applied between the gate SMU (SMU 3) and the drain SMU. The drain SMU is held at 0 V or connected to a ground plane. Drain current  $I_d$  is measured at the drain SMU, and gate leakage current  $I_g$  is measured at the gate SMU.



(a) PDMS surface before sonication in IPA for 10 min

(b) PDMS surface after sonication in IPA for 10 min

Figure 1.10.: Polydimethylsiloxane (PDMS) surface before and after isopropanol (IPA) sonication for 10 minutes.

the vapour delivery system device chamber. This chamber acted as a Faraday cage for another custom-made chip carrier with spring-loaded gold-coated pogo pins, able to contact four channel electrode pairs at once. The silicon back of the device was pressed by the pins against a copper block, connected to the gate SMU.

Custom programs for National Instruments LabView 2017 were used for measurements from the Keysight 4156C Semiconductor Parameter Analyser and the National Instruments NI-PXIe. Keysight EasyEXPERT software was used for characterisation with the Keysight B1500A Semiconductor Device Analyser.

Liquid-gated transfer characteristics of carbon nanotube FETs were measured at  $V_{ds} = 100$  mV and liquid-gated transfer characteristics of graphene FETs were measured at  $V_{ds} = 1$  V, where  $V_{lg}$  was swept between -0.5 V and 1 V in both the forward and reverse direction with a step size of either 10 or 20 mV. Backgated transfer characteristics of carbon nanotube FETs were either measured at  $V_{ds} = 100$  mV or  $V_{ds} = 1$  V, where  $V_{bg}$  was swept between -5 V and 5 V or -10 V and 10 V in the forward and reverse directions with a step size of 50 mV or 100 mV.

### 1.5.1. Sensing Measurements

A liquid-gated setup was used for aqueous-phase sensing and a back-gated setup in the vapour delivery system was used for vapour-phase sensing, as described above.

Sensing measurements were performed with constant source-drain and gate voltages. The gate voltage used was chosen by locating the subthreshold region of the device transfer characteristics and choosing a voltage that fell within this region, usually  $V_g = 0$  V.

## *1. Fabrication of Carbon Nanotube Network and Graphene Field-Effect Transistors*

Using the NI-PXIe with the PXIe-2737 module, eight-channel multiplexed current measurements could be taken in rapid succession. An integration time of 200 or 400 ms was used for sampling with each channel, with the actual sampling rate set by the NI-PXIe. In practice this meant a sampling rate of 1.81 s (for 200 ms integration time) or 3.41 s (for 400 ms integration time) for any given channel. A 200 ms integration time meant the time between samples from successive channels varied between 220ms – 230 ms, while a 400 ms integration time meant the time between samples was consistently 426 ms. The Keysight equipment used a constant 1 s sampling interval.

### **Aqueous Sensing**

Before the sensing process, 200  $\mu\text{L}$  of PBS was added to the PDMS well and 100-120  $\mu\text{L}$  of PBS was removed. This initial step was performed to wet the sides of the PDMS well, and check that the attachment of the PDMS well to the device would not unseal when larger volumes of PBS were added during sensing. From Feb 2022 onwards, a 1800 s control series was performed as part of each sensing experiment to test for unwanted responses to PBS and to allow baseline drift to settle. 20  $\mu\text{L}$  additions of PBS were added to the PDMS well at 100 s, 200 s and 300 s, and 20  $\mu\text{L}$  of PBS were removed from the PDMS well at 400 s, 500 s and 600 s. Immediately after the control series, a sensing sequence was performed as part of the same continuous measurement set. Most commonly, this would consist of a final PBS addition at 2100 s, then analyte additions every 300 s after that. The experimental series was set to finish at 4000 s. The exact timings, analyte concentrations and gate voltage used in a given sensing sequence is discussed alongside the relevant experimental results.

### **Vapour Sensing**

A variety of vapour sensing sequences were used in this work, which are discussed in [?@sec-vapour-sensing-biosensors](#) in detail.

## **1.6. Summary**

A variety of approaches were trialled when depositing a carbon nanotube network for the fabrication of transistor devices, and the resultant morphology of these networks are discussed in the next chapter. Standard photolithographic methods were used to successfully fabricate carbon nanotube and graphene field effect transistor devices. A range of photolithography types and electrode/encapsulation materials were trialled to find the optimal device composition for sensing, also discussed in the next chapter. Atomic force microscopy, fluorescence microscopy and a variety of electrical measurement setups were used to characterise the devices.

## 2. Characteristics of Pristine Carbon Nanotube & Graphene Field Effect Transistors

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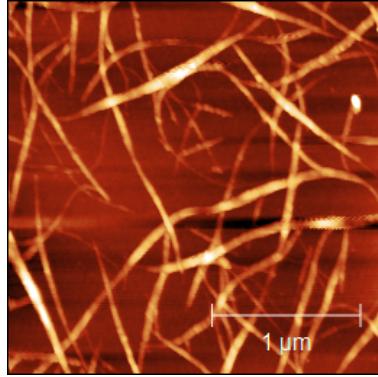
### 2.1. Carbon Nanotube Network Morphology

Figure 2.1 shows a side-by-side comparison of the surface morphology of carbon nanotube films fabricated using the methods described in Section 1.1. These images were collected using an atomic force microscope and processed in the manner described in Section 1.3. They each show bundles of carbon nanotubes with a range of diameters and lengths, with each bundle containing one or multiple nanotubes. As discussed in previous works using solvent-based deposition techniques for depositing carbon nanotubes, multi-tube bundles form due to strong mutual attraction between nanotubes [4], [5], [13], [14]. However, when surfactants are present, they adsorb onto the carbon nanotubes and form a highly repulsive structure able to overcome the strong attraction between nanotubes. This repulsion then keeps the individual carbon nanotubes isolated [15], [16]. The diameter range provided by the supplier for the individual carbon nanotubes used is 1.2 – 1.7 nm, while the length range is 0.3 – 5.0  $\mu\text{m}$  (Nanointegris).

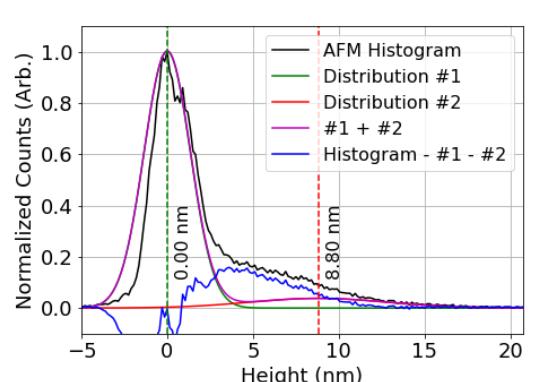
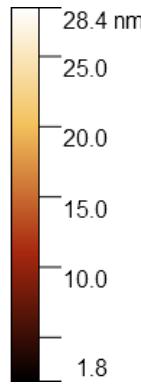
The diameter range of deposited single-walled carbon nanotubes can be modelled via a normal or Gaussian distribution [4], [17]–[19]. However, when we extract and bin the height profiles from the  $2.5 \mu\text{m} \times 2.5 \mu\text{m}$  AFM images, plotted in black in Figure 2.1, the histograms do not follow a normal distribution. The reason for this result is that the carbon nanotubes do not lie perfectly level on a perfectly level silicon oxide substrate - the atomic force microscope histogram would only be a single normal distribution in this ideal case. In practice, the  $\text{SiO}_2$  substrate and carbon nanotube surface both have a degree of roughness, which may in part be due to the presence of atmospheric contaminants. In the case of the surfactant-deposited networks, residual surfactant may also contribute to surface roughness [19]. Furthermore, nanotubes overlap and cross over each other, creating junctions with the combined height of the overlapping nanotubes.

It has been demonstrated that the surface roughness of a bare  $\text{SiO}_2$  substrate can also be modelled with a normal distribution. This normal distribution can be set as the reference or zero point for other height measurements [20]. As both the carbon nanotube and

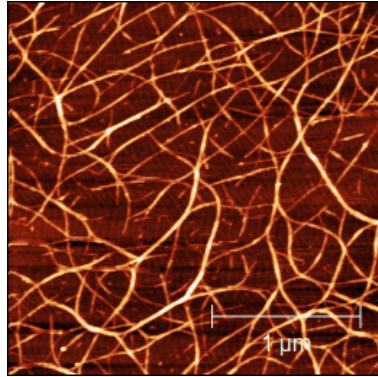
## 2. Characteristics of Pristine Carbon Nanotube & Graphene Field Effect Transistors



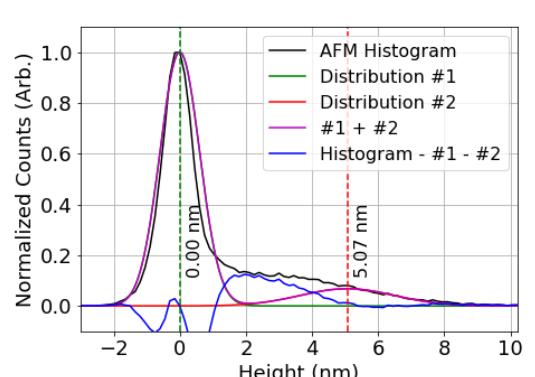
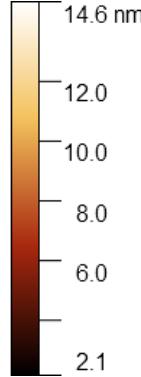
(a) Solvent-based deposition



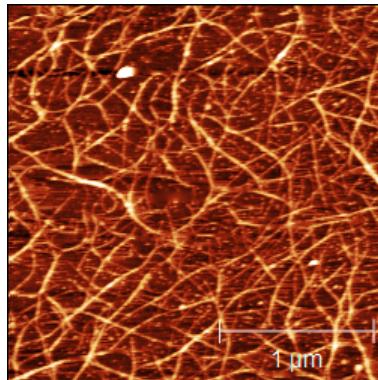
(b) Solvent based deposition histogram



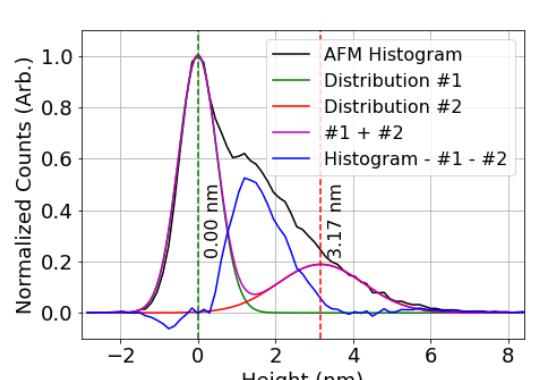
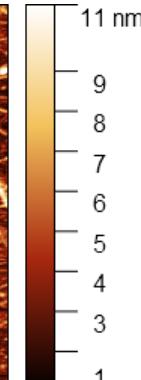
(c) Dropcast surfactant-based deposition



(d) Dropcast surfactant-based deposition histogram



(e) Steam-assisted dropcast surfactant-based deposition



(f) Steam-assisted dropcast surfactant-based deposition

Figure 2.1.:  $2.5 \mu\text{m} \times 2.5 \mu\text{m}$  atomic force microscope (AFM) images of carbon nanotube films deposited using various methods, shown side-by-side with surface profile histograms extracted from the AFM profile. Each histogram is shown alongside a linear combination of normal distributions #1 and #2, corresponding to the silicon and carbon nanotube distribution respectively. The counts remaining after #1 and #2 have been subtracted from the AFM histogram are shown in blue.

## 2.1. Carbon Nanotube Network Morphology

silicon dioxide background heights can each be modelled using a normal distribution, we make an initial assumption that a linear combination of normal distributions can be used to model the AFM histograms in Figure 2.1. Using the process discussed in Section B.2, we approximate the normal distributions corresponding to the silicon oxide substrate and carbon nanotube network, shown in Figure 2.1 as green and red curves respectively. The silicon oxide peak appears to fit more closely to the distribution with smaller carbon nanotube heights, which could be due to measurement of the silicon background being improved when feature height is smaller. We notice that the distribution for the carbon nanotube bundles drops to approximately zero before reaching 0 nm, which is physically appropriate.

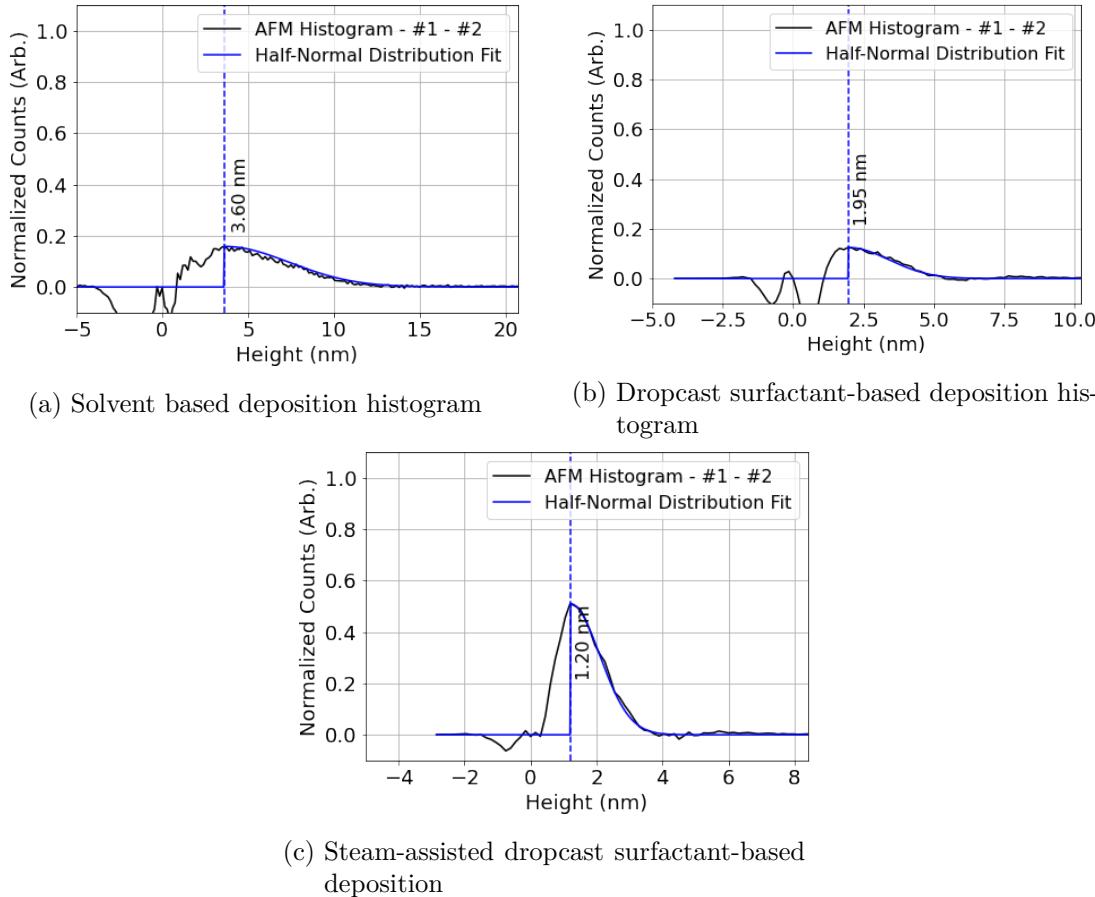


Figure 2.2.: The counts which remain after #1 and #2 have been subtracted from the AFM histogram are shown in black. The counts have been overlaid with half a Gaussian distribution, manually fitted.

By subtracting the modelled silicon and carbon nanotube normal distributions from the AFM histogram, we find a remaining distribution spread roughly between 0 nm and the mean of the carbon nanotube bundle distribution. Interestingly, the peak of the carbon

## 2. Characteristics of Pristine Carbon Nanotube & Graphene Field Effect Transistors

nanotube distribution occurs at a height approximately  $2.5 \times$  the height corresponding to the peak of the remaining distribution. It is also apparent that the remaining distribution consistently follows a normal distribution after a sharp rise to maximum, as shown in Figure 2.2. This distribution appears to correspond to surface roughness due to the presence of contaminants, or possibly to broken pieces of individual nanotubes with various lengths. Contaminants could be residual surfactant or other atmospheric contamination resistant to acetone and isopropanol rinsing. Such contamination may or may not have implications for biosensing suitability, but surfactant contamination could certainly have negative effects on biological elements sensitive to surfactant. The area of this central peak may be useful for determining the extent of contamination on a carbon nanotube film, discussed further in [?@sec-contamination](#).

If we model carbon nanotube bundles as cylinders, and we assume the component nanotubes follow 2D packing and are of equal diameter, we can give an estimate the mean bundle size for each deposition type in terms of number of nanotubes  $n$  [4], [21], [22].

Table 2.1.: The first eight optimised ratios of 2D packed circle diameter to encompassing circle diameter, given to 3 s.f. (encompassing circle diameter =  $d$ , number of packed circles =  $n$ , approximate packed circle diameter =  $d_n$ ).

$n$	2	3	4	5	6	7	8	9
$d/d_n$	2.00	2.15	2.41	2.70	3.00	3.00	3.30	3.61

Table 2.1 shows the relationship between the diameter of a bundle and the constituent diameters of up to nine 2D packed carbon nanotubes within that bundle. Assuming an average carbon nanotube diameter of 1.45 nm, we can use the  $d/d_n$  packing ratios to obtain an estimate of the number of nanotubes in the mean bundle size for each deposition [22]. We can also give an approximate range which this estimate falls within using the provided range of individual carbon nanotube diameters (1.2 – 1.7 nm) and the 95% confidence interval of the mean bundle size ( $2\sigma$ ). These estimates are shown in Table 2.2. Also shown is an estimate of the ratio of single- to multi-tube bundles for each deposition, found by comparing the proportion of each carbon nanotube curve below and above 2.9 nm, the minimum multi-tube bundle size for 1.45 nm diameter nanotubes. It should be noted that the force of the atomic force microscope tip may cause some degree of nanotube bundle compression, leading to a systematic underestimate of nanotube height [19]. The relative proportion of multi-tube bundles shown in Table 2.2 should therefore be treated as a lower-limit estimate of the true proportion.

When surfactant is used in the deposition process, both the carbon nanotube bundle diameter mean and standard deviation are small compared to the mean and standard deviation of solvent deposited films. However, despite the presence of surfactant, it is apparent both from Figure 2.1 and Table 2.2 that not all surfactant-dispersed carbon

## 2.2. Electrical Characteristics of Pristine Devices

Table 2.2.: The mean of histogram distributions for carbon nanotube films deposited using various methods, alongside estimates for the number of nanotubes present per bundle (within a 95% confidence interval) and the proportion of multi-tubed bundles present across the network. The value in brackets corresponds to an estimate for the number of nanotubes present in the mean bundle size.

	Distribution Mean (nm)			Bundle Attributes	
	Silicon	Bundles	Contaminant	Tubes/Bundle	% Multi-Tube
Solvent deposited	$0.0 \pm 1.4$	$8.8 \pm 4.0$	$3.6 \pm 3.8$	1–162 (28)	~95%
Surfactant deposited	$0.0 \pm 0.6$	$5.1 \pm 1.4$	$2.0 \pm 1.5$	2–34 (8)	~94%
Surfactant deposited with steam	$0.0 \pm 0.5$	$3.2 \pm 1.1$	$1.2 \pm 0.9$	1–15 (3)	~60%

nanotubes are deposited individually. Bundling may occur during the process of deposition onto the substrate, which could disrupt the repulsive forces from the surfactant coating and allow attractive forces to temporarily dominate.

It is possible that the bundling of surfactant-dispersed carbon nanotubes is a consequence of dynamics introduced by the coffee-ring effect [23], [24]. The coffee-ring effect refers to a build-up of dispersed solid forming around the edges of a dispersion evaporating on a surface. This process occurs due to the dispersion edges being fixed by surface forces, leading to capillary flow outwards to replace liquid evaporating at the edges, bringing solid material along with it. The presence of vapour is known to disrupt this capillary effect [25].

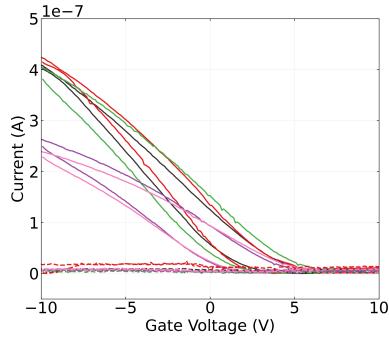
## 2.2. Electrical Characteristics of Pristine Devices

### 2.2.1. Carbon Nanotube Network Devices

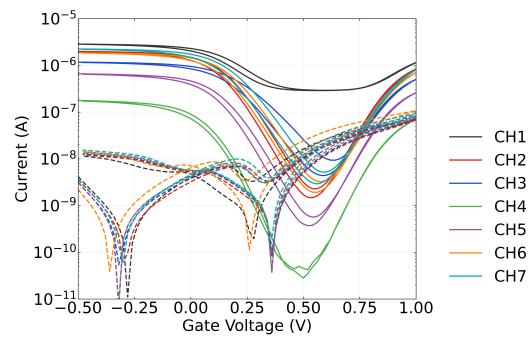
Each carbon nanotube device fabricated was electrically characterised as described in Section 1.5, and electrical data was analysed using the Python code discussed in Section B.3.

Figure 2.3 displays multi-channel measurements of representative devices fabricated as described in Chapter 1. To ensure a consistent comparison, each device here was encapsulated with AZ® 1518 encapsulation before measurements were taken. The channels

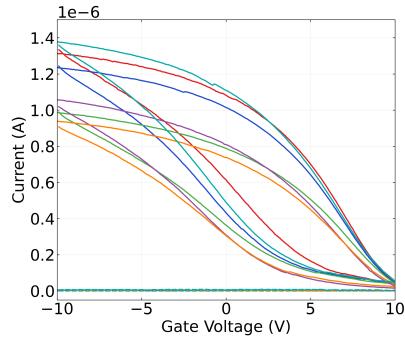
## 2. Characteristics of Pristine Carbon Nanotube & Graphene Field Effect Transistors



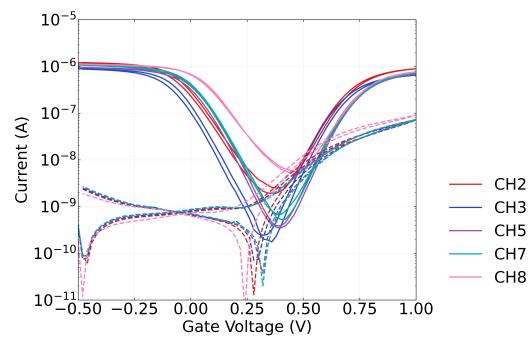
(a) Solvent-based deposition, back-gated



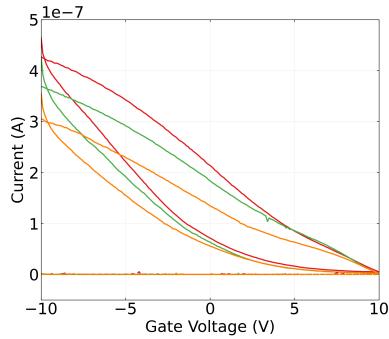
(b) Solvent-based deposition, liquid-gated



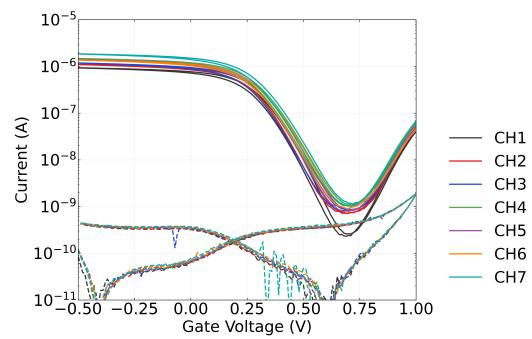
(c) Dropcast surfactant-based deposition, back-gated



(d) Dropcast surfactant-based deposition, liquid-gated



(e) Steam-assisted dropcast surfactant-based deposition, back-gated



(f) Steam-assisted dropcast surfactant-based deposition, liquid-gated

Figure 2.3.: Transfer characteristics of AZ® 1518 encapsulated field-effect transistors with carbon nanotube network channels deposited using various methods. 1XPBS was used as the buffer for the liquid-gated measurements here. The source-drain voltage used for all sweeps was  $V_{ds} = 100\text{mV}$ . A step size of 20 mV was used for the liquid-gated sweeps, while a step size of 100 mV was used for the backgated sweeps. Each pair of sweeps was taken from a separate device. Devices with a 100 nm SiO<sub>2</sub> layer were used for backgated measurements, and devices with a 300 nm SiO<sub>2</sub> layer were used for liquid gated measurements.

## 2.2. Electrical Characteristics of Pristine Devices

which did not exhibit reliable transistor characteristics are not shown. These ‘non-working’ channels were either shorted, due to metal remaining on the channel after lift-off, or were very low current, due to a very sparse carbon nanotube network. Devices shown here with a solvent-deposited carbon nanotube network were fabricated prior to Jan 2022; devices with a surfactant-deposited network without steam present were fabricated prior to Jun 2021; devices with a surfactant-deposited network without steam were fabricated prior to Sep 2022.

When backgated, devices exhibited *p*-type transistor behaviour with significant hysteresis and negligible gate current leakage. The presence of hysteresis can be explained by the presence of charge traps on the surface of the silicon dioxide and at interfaces between the silicon dioxide and carbon nanotubes [26], [27]. The devices fabricated with a solvent-based deposition were switched off at a lower voltage than the devices which used surfactant during deposition.

When the devices were liquid-gated with 1XPBS electrolyte, they exhibited ambipolar characteristics, commonly observed in carbon nanotube network FETs [4], [9], [28]–[31]. Devices generally exhibited significantly less hysteresis than in the backgated case. When devices were appropriately configured, leakage current did not exceed  $\sim 1 \times 10^{-7}$  V across the forward and reverse sweep. The devices shown which used carbon nanotube films deposited in surfactant with steam present had significantly less channel-to-channel variation in electrical characteristics than the devices fabricated using other approaches. A summary of key parameters of pristine liquid-gated devices is shown in Figure 2.4. The full dataset consists of three sets of 21 liquid-gated transfer characteristics of working channels, with each set corresponding to the use of a particular method of carbon nanotube network deposition in the device fabrication. Measurements from at least three devices are included in each set. Each entry in the summary corresponds to the average of the specific parameter in the forward and reverse sweep direction.

Channels from surfactant-deposited film devices usually showed a larger on-off ratio and subthreshold slope than those from solvent-deposited devices. When the transistor is gated in the subthreshold range, a larger on-off ratio and subthreshold slope results in a larger change in conductance in response to changes in the transfer characteristic curve. Therefore, a larger on-off ratio and subthreshold slope is desirable for improved sensor performance [28], [29], [32]. The larger on-off ratio for surfactant-deposited film devices is likely a result of the reduced bundling of nanotubes, as discussed in Section 2.1. Carbon nanotube pathways across the channel with a lower degree of bundling will have a lower number of component metallic tubes in the network, which increases the on-off ratio [4], [17], [33]. The effect of metallic nanotubes increasing the off current of a device channel is illustrated by channel 1 in Figure 2.3b. The larger subthreshold slope is likely due to increased mobility from a denser nanotube network in surfactant-deposited films [33], as seen in Figure 2.1.

When steam is used for surfactant deposition of films, the resulting devices showed highly consistent channel-to-channel electrical properties. As the carbon nanotube films on these devices are relatively dense, as seen in Figure 2.1, we know that the network

2. Characteristics of Pristine Carbon Nanotube & Graphene Field Effect Transistors

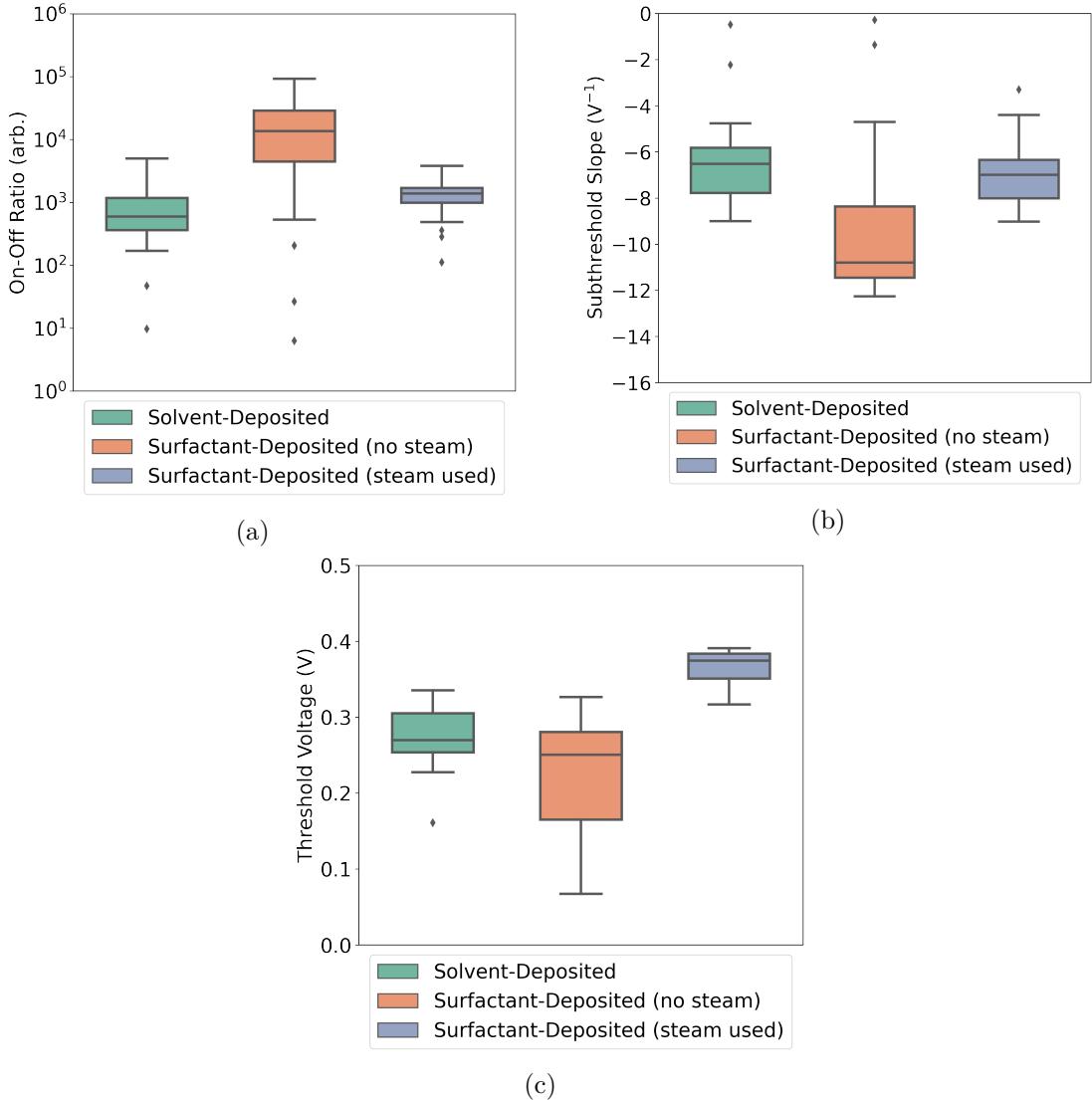


Figure 2.4.: These boxplots illustrate the statistical distribution of (a) the on-off ratio, (b) the subthreshold slope, and (c) the threshold voltage of AZ® 1518 encapsulated liquid-gated transistor channels corresponding to each type of carbon nanotube film deposition. For each deposition type, electrical characteristics were taken of 21 channels of at least three separate devices. The boxes indicate the 25th and 75th percentile of the distribution.

## 2.2. Electrical Characteristics of Pristine Devices

is well above the percolation threshold. As many carbon nanotube pathways connect across the channel in parallel, small variations in the network morphology have less of an impact on the overall channel behaviour [4]. We also see from Table 2.2 that the range of bundle sizes is relatively low in the steam-deposited films used in these devices. The low range of bundle sizes means the semiconducting-metallic nanotube ratio is far more consistent for these devices, leading to more consistent electrical device characteristics. Being able to achieve consistent subthreshold regime behaviour between channels on the same device is a desirable attribute for reliable real-time multiplexed biosensing [28], [29], [32].

All channels characterised had a positive threshold voltage ( $V_{th}$ ). The threshold voltage was largest and most consistent for steam-assisted surfactant-deposited films. The marked increase in  $V_{th}$  for channel measurements from surfactant-deposited devices with steam present relative to other channel measurements indicates *p*-doping of the carbon nanotubes has occurred [4], [34]. It is highly likely the dopant is present due to the steam deposition, and may be related to the large contamination peak for steam-deposited films seen in Figure 2.1 and Figure 2.2. One possibility is that this dopant is residual surfactant, which can *p*-dope carbon nanotubes and lead to enhanced *p*-doping from adsorbed oxygen and water [35], [36]. We have seen that steam prevents bundling of carbon nanotubes during deposition. This effect is likely due to persistence of the surfactant keeping nanotubes separate during this process. Presence of surfactant may also explain the lowered subthreshold slope and therefore mobility of the surfactant-deposited devices with steam relative to the surfactant-deposited devices without steam. The analysis by Kane *et al.* shows that the thermal annealing at 150°C used in this work to remove residual surfactant is likely inadequate for this purpose [35].

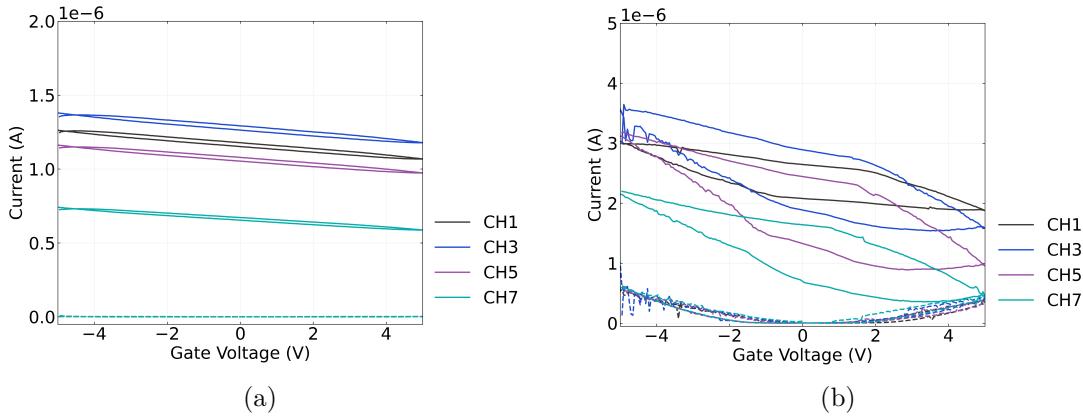


Figure 2.5.: Backgated transfer sweeps were taken of a single unencapsulated device with a 300 nm SiO<sub>2</sub> layer and steam assisted surfactant-deposited carbon nanotube network channels before and after being covered in 50 $\mu$ L 1XPBS electrolyte.

Figure 2.5 shows the behaviour of an unencapsulated backgated device with a 300 nm

## 2. Characteristics of Pristine Carbon Nanotube & Graphene Field Effect Transistors

$\text{SiO}_2$  layer before and after being covered by 50  $\mu\text{L}$  of 1XPBS (phosphate buffered saline). The on-off ratio and hysteresis of the channels increase significantly. The presence of water increases hysteresis through introducing charge traps at the silicon dioxide surface around the carbon nanotubes and at the surface of the nanotubes themselves [26], [27], [37]. The use of alternative transistor dielectrics and/or device functionalisation could potentially be used to reduce this hysteresis, as the time variation in threshold voltage due to hysteresis is unwanted for biosensing work [26], [27]. The electrical double layer formed by the electrolyte at the surface of the carbon nanotubes will also have contributed to the observed change in electrical properties, as it screens surface charge present on the surface around the nanotubes [38].

There is also a significant increase in current leakage to the backgate for larger applied voltages, despite the electrolyte having no visible physical contact with the silicon backgate or copper plane. This leakage current may simply be due to an increase in relative humidity around the device due to the presence of water [39].

### 2.2.2. Graphene Devices

Graphene devices were electrically characterised in the manner described in Section 1.5 and analysed using the Python code discussed in Section B.3.

Figure 2.6 shows the liquid-gated transfer characteristics of two graphene devices. These devices were fabricated prior to Jun 2021. Both devices exhibit the ambipolar characteristics typical of liquid-gated graphene devices [38], [40]–[42]. As with the carbon nanotube network devices, leakage current remained below  $\sim 1 \times 10^{-7} \text{ V}$  across both the forward and reverse sweep. Hysteresis between the forward and reverse sweep results from charge traps within and on the surface of the  $\text{SiO}_2$  dielectric [43]. The major Dirac point for these devices is slightly to the right of  $V_{\text{Dirac}} \approx 0 \text{ V}$ , which indicates *p*-doping of the channel. This slight *p*-doping is likely a result of a adsorption of oxygen and water from the air and residue resist from photolithography [42], [44], [45].

Some devices exhibited a double-minima feature, indicating the presence of two Dirac points. This effect arises due to doping of graphene by the metal contacts. In shorter length channels, metal doping affects the entire channel length, leading to a consistent Fermi level and a single Dirac point. However, for longer channel lengths like ours, the doping effect from metal contact no longer reaches the entire channel, leading to a difference in Fermi level between the graphene in the channel and graphene under the metal contact. The difference in Fermi levels results in the presence of a second Dirac point [43], [46], [47]. The global minimum of the transfer characteristic can be referred to as the ‘major’ Dirac point.

Figure 2.6 also shows the effect of 1XPBS on the graphene channels. The channels were measured on exposure to 1XPBS, after exposure to 1XPBS for one hour, and after the device surface was rinsed and 1XPBS was replaced in the well one time, two times and three times successively. A slight leftward shift of the major Dirac point was observed,

## 2.2. Electrical Characteristics of Pristine Devices

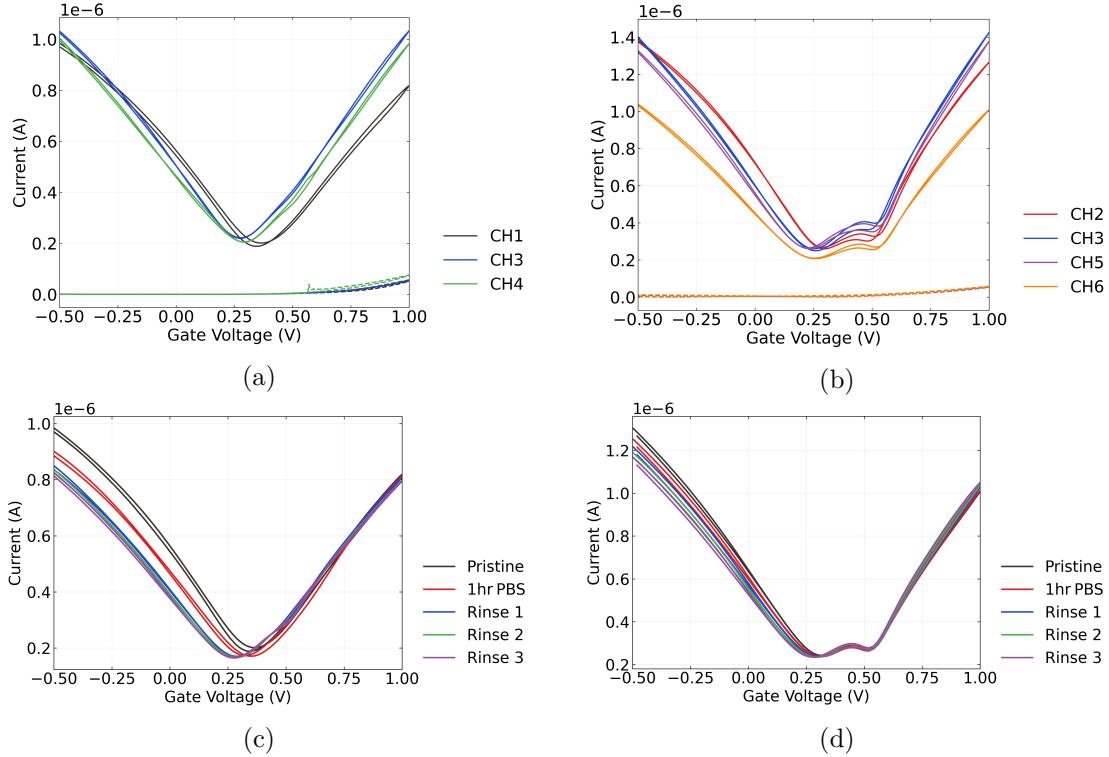


Figure 2.6.: These figures show liquid-gated transfer characteristics of channels from two AZ® 1518 encapsulated graphene devices. In (a) and (b), the characteristics of working device channels upon initial exposure to 1XPBS are displayed alongside gate current. The transfer characteristics of channel 1 in (a) and channel 5 in (b) after various degrees of exposure to 1XPBS are shown in (c) and (d) respectively.

## 2. Characteristics of Pristine Carbon Nanotube & Graphene Field Effect Transistors

Table 2.3.: Average on-off ratio and major Dirac point voltage for AZ® 1518 encapsulated liquid-gated graphene transistor channels at various stages of exposure to 1XPBS. Electrical characteristics were taken of 6 channels total, three channels from each of two devices.

	1XPBS: Initial	1XPBS: After 1 hr	1XPBS: Rinse
On-Off Ratio (arb.)	$5.1 \pm 0.3$	$5.0 \pm 0.7$	$5.0 \pm 0.6$
Dirac Point Voltage (V)	$0.28 \pm 0.04$	$0.31 \pm 0.03$	$0.28 \pm 0.02$

which Kireev *et al.* speculate is due to gate current having an annealing effect on the channel and removing *p*-dopant from the graphene surface [42]. Kireev *et al.* also found that continuing to perform liquid-gated sweeps reduced the size of the second Dirac point, and suggested that it was related removal of atmospheric contaminants from the graphene surface [42]. When this occurs, it may be due to the removal of contaminants improving contact between the metal and graphene surface, and thus increasing metal doping and consistency of the Fermi level across the channel.

Table 2.3 shows the on-off ratio and major Dirac point voltage of the graphene devices. Apart from the previously-mentioned slight leftward shift of the major Dirac point, these values were highly consistent before and after exposure to 1XPBS.

### 2.3. Salt Concentration Sensing with Phosphate Buffered Saline

#### 2.3.1. Control Series and Baseline Drift

The total interval for the control series was 1800 s, with  $20\mu\text{L}$  1XPBS additions at 100 s, 200 s and 300 s, and  $20\mu\text{L}$  subtractions at 400 s, 500 s and 600 s. Devices were left untouched over the next 1200 s to allow the current level to settle. Figure 2.7a shows the transfer sweep of a single channel of a steam-assisted surfactant-deposited device encapsulated with SU8, fabricated after Jun 2023. The threshold voltage of the channel is  $V_{\text{th}} = 140$  mV, and the voltage corresponding to minimum current is  $V_{\text{gap}} = 310$  mV. The variable symbol  $V_{\text{gap}}$  denotes the center of the transistor bandgap, has been labeled in this manner to be consistent with previous work [29].

Figure 2.7b shows two control series performed using the same channel on different days, with a different gate voltage used during each series. In both series, there is no clear stepwise response to any addition or subtraction of 1XPBS, as expected. Linear fits were performed on each control series from 1200 – 1800 s. The gradient of the  $V_{\text{lg}} - V_{\text{gap}} = -200$  mV gated control series was  $m_1 = -0.95 \pm 0.02$  pA/s, while the gradient of the  $V_{\text{lg}} - V_{\text{gap}} = -150$  mV gated control series was  $m_2 = -0.69 \pm 0.02$  pA/s.

### 2.3. Salt Concentration Sensing with Phosphate Buffered Saline

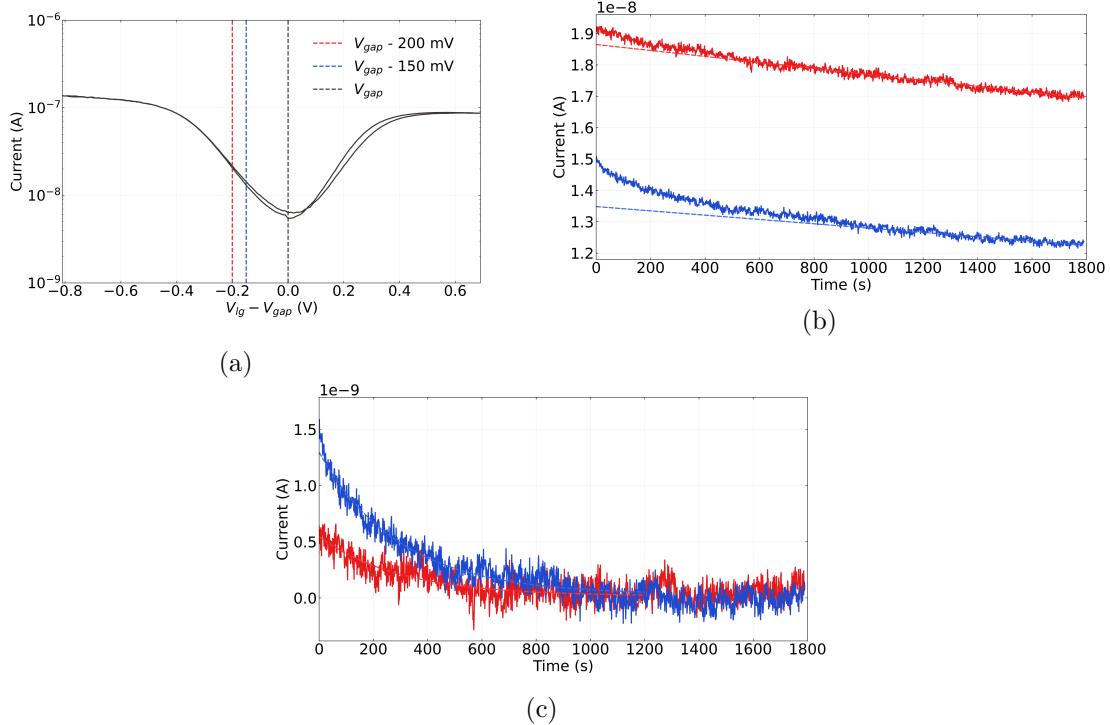


Figure 2.7.: These figures show The linear fits in (b) had R squared values of 0.78 and 0.70 for the traces with gate voltage  $V_{lg} - V_{gap} = -200$  mV and  $V_{lg} - V_{gap} = -150$  mV respectively. The exponential fits in (c) had R squared values of 0.71 and 0.93 for the  $V_{lg} - V_{gap} = -200$  mV and  $V_{lg} - V_{gap} = -150$  mV traces respectively.

## 2. Characteristics of Pristine Carbon Nanotube & Graphene Field Effect Transistors

The equations for the two linear fits were proportional to each other, with  $m_2 = (0.73 \pm 0.03) \times m_1 t + b_1$ .

When the linear fits were subtracted from the raw data, the remaining dataset exhibited an exponential decay for each control series. Figure 2.7c shows exponential fits to the remaining curve from 0–1200 s. Both exponentials have a characteristic time constant of  $\tau = 300 \pm 20$  s, indicating the rate of decay is independent of the gate voltage used to gate the transistor. As both exponentials decay to zero, they are therefore also proportional to each other, with  $a_2 \exp(-t/\tau) = (2.39 \pm 0.05) \times a_1 \exp(-t/\tau)$ . The  $V_{lg} - V_{gap} = -200$  mV measurement was performed 3 days after the  $V_{lg} - V_{gap} = -150$  mV measurement. It is possible that the amplitude ratio is history dependent, where the amplitude of the initial decay curve of the channel is reduced with each subsequent control series.

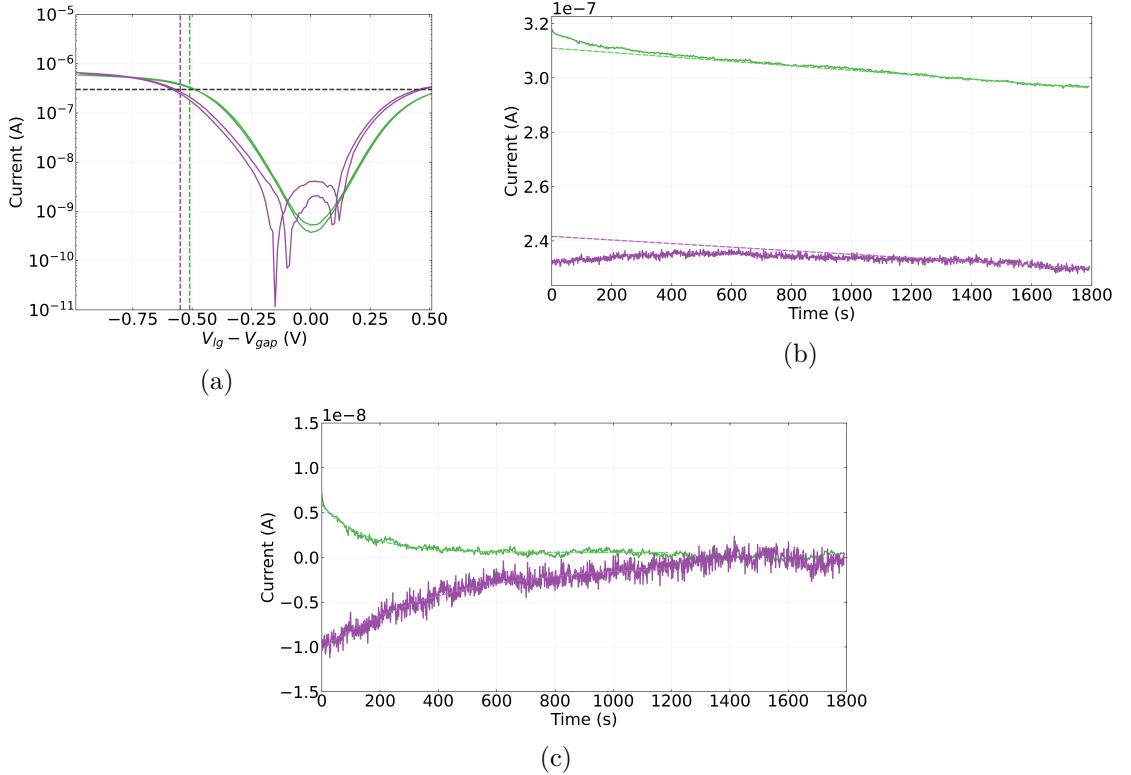


Figure 2.8.: These figures show The linear fits in (b) had R squared values of 0.96 and for Device 1 and Device 2 respectively. The exponential fits in (c) had R squared values of for the  $V_{lg} - V_{gap} = -200$  mV and  $V_{lg} - V_{gap} = -150$  mV traces respectively.

Figure 2.8a shows channel transfer characteristics from two different steam-assisted surfactant-deposited, AZ® 1518 encapsulated devices fabricated in different device batches. Device 1, with the channel characteristic curve shown in green, was fabricated in Mar 2023. Device 2, with the channel characteristic curve shown in purple, was

### 2.3. Salt Concentration Sensing with Phosphate Buffered Saline

fabricated after Jun 2023. Device 2 was rinsed with AZ® 326 developer and annealed at 150°C before measurement. When taking control series measurements, the devices were gated so that the current level for each control series would be as similar as possible, as illustrated by the dotted lines in Figure 2.8a.

As in Figure 2.7b, linear fits were performed on each control series from 1200 – 1800 s, shown in Figure 2.8b. The gradient of the control series corresponding to Device 1 was  $m_1 = -8.2 \pm 0.1$  pA/s, while the gradient of the control series corresponding to Device 2 was  $m_2 = -6.6 \pm 0.2$ . Again, the equations for the two linear fits were proportional to each other, where  $m_2 t + b_2 = (0.81 \pm 0.03) \times m_1 t + b_1$ , despite being different channels from a different device batch.

As with the SU8 device, subtracting the linear fit resulted in a dataset which could be fitted with an exponential function. Figure 2.8c shows exponential fits from 0 – 1200 s to the AZ® 1518 devices. Both exponentials have a characteristic time constant of  $\tau = 300 \pm 20$  s, indicating the rate of decay is independent of the gate voltage used to gate the transistor. As both exponentials decay to zero, they are therefore also proportional to each other, with  $a_2 \exp(-t/\tau) = (2.39 \pm 0.05) \times a_1 \exp(-t/\tau)$ . The  $V_{lg} - V_{gap} = -200$  mV measurement was performed 3 days after the  $V_{lg} - V_{gap} = -150$  mV measurement. It is possible that the amplitude ratio is history dependent, where the amplitude of the initial decay curve of the channel is reduced with each subsequent control series.

From this analysis it appears that the baseline drift for the liquid-gated carbon nanotube devices can be modelled as a combination of an exponential, linear and constant term. The linear term appears to be consistent between channels of a particular device type,

#### 2.3.2. Sensing Series

-nLOF2020 resist being used leads to devices with less drift!!

-low pass filter??



## A. Photolithography

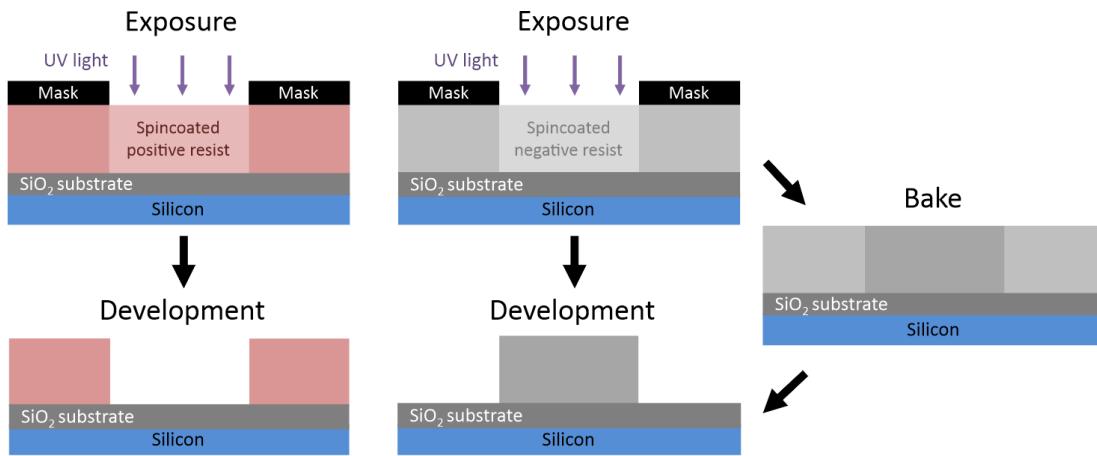


Figure A.1.: A side-view comparison of generic photolithography processes for positive and negative resists in the ideal case. Photolithography with a positive resist requires a single softbake step before exposure, while for negative resists a second baking step is required after exposure (Thicknesses shown not to scale).

This section details some of the standard photolithography procedures used in the device fabrication processes detailed in Chapter 1. Photoresists, also referred to here as “resists”, are UV light-sensitive polymeric resins used for photolithography. Both positive and negative photoresists were used in various fabrication processes. Positive resists are made soluble in alkalines by UV light exposure, meaning exposed areas are removed in the development process. Conversely, negative resists are cross-linked by exposure and a post-exposure bake step. The unexposed areas of the negative resist are then removed in the development process [48]. Figure A.1 gives a visual representation of these differences.

The specific photoresist selected for photolithography depends on the specific use case. The types used in this thesis are positive and negative AZ® photoresists (AZ® 1518, Microchemicals GmbH; AZ® nLOF 2020, Microchemicals GmbH) and SU-8 (SU8-2150, Kayaku Advanced Materials, formerly Microchem). The AZ® resists used here have a minimum film thickness of  $1.5 \mu\text{m}$  [48], while the SU8-2150 has a minimum film thickness of  $0.5 \mu\text{m}$  [49]. Positive resists which have not been thermally crosslinked will soften at higher temperatures ( $\gtrsim 100^\circ\text{C}$  for AZ® 1518), leading to a rounded profile. This is not

### A. Photolithography

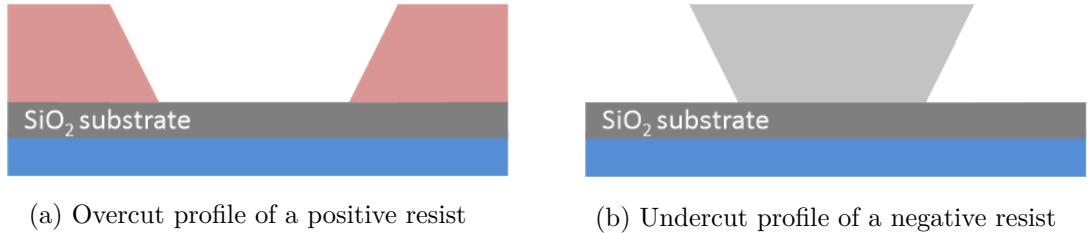


Figure A.2.: Two different resist profiles seen for different types of photoresist. Each profile has had the central region of the substrate exposed to UV light prior to development. The undercut profile is ideal for thin-film metal deposition and subsequent patterned removal, known as “lift-off”.

the case for negative resists, which are more thermally stable [48]. Each resist therefore has a different cross-section profile, as shown in Figure A.2.

If metal deposition is performed on a positive resist, some metal can collect on the outwardly-sloped sidewalls of the resist (see Figure A.2) which forms significant spikes on the edges of the deposited metal upon lift-off. On the other hand, metal cannot collect on top of the inwardly-sloped negative profile sidewalls, which avoids the formation of large edge spikes. Therefore, the negative resist profile is more suited to metal or metal oxide deposition and lift-off processes, though the process is more sensitive to human error due to requiring more processing steps than positive resist [48]. Finally, when it is suitably processed SU-8 is considered to be more stable and biocompatible than other photoresists [9]. It is especially biocompatible when chemically modified via processes such as isopropanol sonication and O<sub>2</sub> plasma treatment [8].

All photolithographic exposure was performed using a Karl Suss MJB3 Contact Aligner with a USHIO super-high pressure 350 W mercury lamp (USH-350DS, Japan). When performing photolithography, the intensity reading from the aligner was 20.8 – 24.2 mW/cm<sup>2</sup> (Note however that an external photometer reading at 400 nm found an intensity output of 17.2 mW/cm<sup>2</sup> when the aligner read 21.0 mW/cm<sup>2</sup>).

In general, photolithography procedures should be performed under yellow lighting, as light wavelengths from 320 – 450 nm can promote reactions in the photoresist used. Aging of photoresist over time can also significantly affect the photolithography process, and therefore all processes should be re-optimised regularly over time to give the desired result [48]. The range in processing times for some steps of the processes used here are largely due to the effects of aging on the photoresist.

The step-by-step processes for each resist are detailed in the subsequent sections.

## **A.1. AZ® 1518 photoresist**

1. Spincoat at a final speed of 4000 rotations per minute (rpm) for 1 minute, with an initial acceleration of 500 rpm/s (notes: clean the substrate with acetone, isopropanol (IPA) and nitrogen before spincoating; use only the minimum amount of photoresist required to fully cover the wafer surface; avoid any gaps or bubbles in the photoresist).
2. Softbake 2 – 4 minutes at 95°C on the hotplate (2 min for individual devices, 4 min for a quarter wafer)
3. Mask expose for 10 – 12 s (note: clean mask with acetone/IPA and N<sub>2</sub> dry before use)
4. Develop with 3 parts AZ® 326 (2.38 % TMAH metal-ion free developer, Microchemicals GmbH) in 1 part deionised (DI) water for 30 – 45 s (note: rinse for 10 – 15 s in one development solution, then perform the rest of the development in clean developer for a cleaner profile; lightly agitate the solution throughout the development process)
5. Rinse device for 30 s in DI water to remove excess developer, then dry under nitrogen

## **A.2. AZ® nLOF 2020 photoresist**

1. Spincoat at final speed of 3000 rotations per minute (rpm) for 1 minute, with an initial acceleration of 500 rpm/s (notes: clean the substrate with acetone, isopropanol (IPA) and nitrogen before spincoating; avoid any gaps or bubbles in the photoresist)
2. Softbake for precisely 60 s at 110°C on the hotplate
3. Mask expose for 2.7 – 3 s (note: clean mask with acetone/IPA and N<sub>2</sub> dry before use)
4. Post-exposure bake for precisely 60 s at 110°C on the hotplate to cross-link exposed resist
5. Develop with 3 parts AZ® 326 in 1 part DI water for 60 – 70 s (note: rinse for 30 s in one development solution, then perform the rest of the development in clean developer for a cleaner profile; lightly agitate the solution throughout the development process)
6. Rinse device for 30 s in DI water to remove excess developer, then dry under nitrogen

*A. Photolithography*

**A.3. SU8-2150 photoresist**

1. SU-8 was diluted in cyclopentanone until viscosity was low enough to spincoat on substrate and then sonicated at 50°C for 3 – 4 hours (Note: The dilution ratio used was ~1 part SU-8 to 5 parts cyclopentanone. However, the age of the SU-8 may mean that significant evaporation had occurred prior to use, and the amount of SU-8 actually present is underrepresented by this ratio)
2. Spincoat first with a final speed of 500 rpm (acceleration 500 rpm/s) for 10 seconds, followed by spincoating at 4000 rpm (acceleration 7500 rpm/s) for 40 s.
3. Softbake for 10 minutes at 95°C on the hotplate
4. Mask expose for 6 – 8 s (note: clean mask with acetone/IPA and N<sub>2</sub> dry before use)
5. Post-exposure bake for 10 minutes at 95°C on the hotplate to cross-link exposed resist
6. Develop with SU-8 developer (Kayaku Advanced Materials, formerly Microchem) for 10 – 15 s, then clean in IPA for 30 s, repeat this step once then dry under nitrogen (note: lightly agitate the solution throughout the development process)

## B. Python Code for Data Analysis

### B.1. Code Repository

The code used for general analysis of field-effect transistor devices in this thesis was written with Python 3.8.8. Contributors to the code used include Erica Cassie, Erica Happe, Marissa Dierkes and Leo Browning. The code is located on GitHub and the research group OneDrive, and is available on request.

### B.2. Atomic Force Microscope Histogram Analysis

The purpose of this code is to analyse atomic force microscope (AFM) images of carbon nanotube networks in .xyz format taken using an atomic force microscope and processed in Gwyddion (see Section 1.3). It was originally designed by Erica Happe in Matlab, and adapted by Marissa Dierkes and myself for use in Python.

$$f(x) = k_1 \exp\left(-\frac{(x - m_1)^2}{2s_1^2}\right) + k_2 \exp\left(-\frac{(x - m_2)^2}{2s_2^2}\right) + \dots \quad (\text{B.1})$$

The .xyz data is initially sorted into bins with 0.15 nm size. The bin with the maximum number of counts is set at 0 nm, as this peak represents the mean of the surface roughness of the bare silicon. The parameters  $m_i$ ,  $s_i$ ,  $k_i$  ( $i = 1, 2, 3$ ) are used with objective function Equation B.1 to overlay the data with normal distributions. These fitting parameters represent the mean (m), standard deviation (s) and amplitude (k) of each normal distribution. We can make approximations of some of these fitting parameters using the histogram data.

$k_1$  is taken to be the maximum y-value of the data being fitted,  $m_1$  is set to zero (used as a point of reference) and  $s_1$  is taken as one-third of the difference between  $m_1$  and the x-value of the first datapoint where the y-value is greater than 1% of  $k_1$  (approximating one standard deviation). We find the distribution given by these values using Equation B.1, and subtract it from the existing dataset.

Then, using the analysis technique outlined by Vobornik *et al.* [19] in Gwyddion, we manually find estimates for the mean  $m_2$  and standard deviation  $s_2$  of the carbon nanotube bundle distribution. We then take  $k_2$  to be the maximum y-value of this modified

## B. Python Code for Data Analysis

dataset, and  $m_1$  to be the x-value of the maximum y-value. We then set  $k_2$  so that the height of the resulting distribution at one standard deviation matches the height of the .xyz data histogram. We take this distribution, and subtract it from the existing dataset.

The code also allows for discretely binning continuous data from fitted normal distributions and examining the proportion of counts above or below a particular height. 2.9 nm is roughly where 2 bundles with average size 1.45 nm can start to be present, and is used as an estimate of the boundary value between single-tube bundle diameters and multi-tube bundle diameters.

## B.3. Field-Effect Transistor Analysis

The purpose of this code is to analyse electrical measurements taken of field-effect transistor (FET) devices. Electrical measurements were either taken from the Keysight 4156C Semiconductor Parameter Analyser, National Instruments NI-PXIe or Keysight B1500A Semiconductor Device Analyser as discussed in Section 1.5; the code is able to analyse data taken from all three measurement setups. The code consists of three related but independent modules: the first analyses and plots sensing data from the FET devices, the second analyses and plots transfer characteristics from channels across a device, and the third compares individual channel characteristics before and after a modification or after each of several modifications. These modules were designed collaboratively by myself and Erica Cassie over GitHub using the Sourcetree Git GUI.

$$f(x) = k_1 \exp\left(-\frac{t}{\tau_1}\right) + k_2 \exp\left(-\frac{t}{\tau_2}\right) + \dots + c \quad (\text{B.2})$$

## C. Vapour Delivery System

### C.1. Technical Notes

Two LabView Virtual Instruments (VIs) were adapted from pre-existing VIs for operating the mass flow controllers and monitoring vapour flow into the device chamber, as well as monitoring temperature and humidity in the vapour delivery system's manifold. These VIs were named “ ” A third VI was developed in parallel which combined the first two Virtual Instruments, alongside allowing the sequence of values to control the mass flow controllers.

From Honours report: “ ” Figure 12 gives the right side of the front panel of the LabView VI sample with `vapour.VI`, which lets us preset an autonomously-performed vapour sensing sequence. Each row in each array module corresponds to a different step in this sequence. The ‘`howManySteps`’ module lets us set how many of these steps are performed. The ‘`Durations Array`’ module determines the length of time in seconds each step is performed over. The ‘`Carrier Flows Array`’ and ‘`Dilution Flows Array`’ modules let us set the carrier flow and dilution flow, respectively, in standard cubic centimetres per minute (sccm) through the gas rig at each step. The carrier flow pushes analyte vapour into the vapour-sensing device chamber, while dilution flow is used to modify the flow behaviour of the analyte vapour entering the chamber. The vapour sensing sequence as depicted in Figure 12 was used for all vapour sensing runs in this investigation. At the end of the sequence, the data collected about the vapour sensing process was saved as an `.lvm` file. “ ”

### C.2. Future Improvements



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