

Fabrication of Carbon Nanotube Network and Graphene Field-Effect Transistors

This chapter discusses the fabrication processes for both the carbon nanotube network and graphene field-effect transistors (FETs). Experimental optimisation of the transducer element is critical for biosensor work, and large numbers of transducers were required for testing various biosensor functionalisation processes. Therefore, these processes were developed to rapidly fabricate devices with reproducible device characteristics appropriate for biosensing work. Also outlined in this chapter are the characterisation techniques taken to test the quality and reproducibility of these fabrication processes.

The nitrogen ($\geq 99.99\%$) and oxygen (99.7%) used in fabrication work was supplied by BOC Limited New Zealand. All acetone and isopropanol used for wafer/device processing had a minimum 99.9% purity (HPLC grade). Deionised (DI) water was taken from a Synergy[®] UV Water Purification System. The DI water had a measured conductivity of $(1.4 \pm 0.1) \mu\text{S cm}^{-1}$, compared to tap water with a measured conductivity of $(7.8 \pm 0.2) \mu\text{S cm}^{-1}$.

Photolithography for Carbon Nanotube and Graphene Field-Effect Transistors

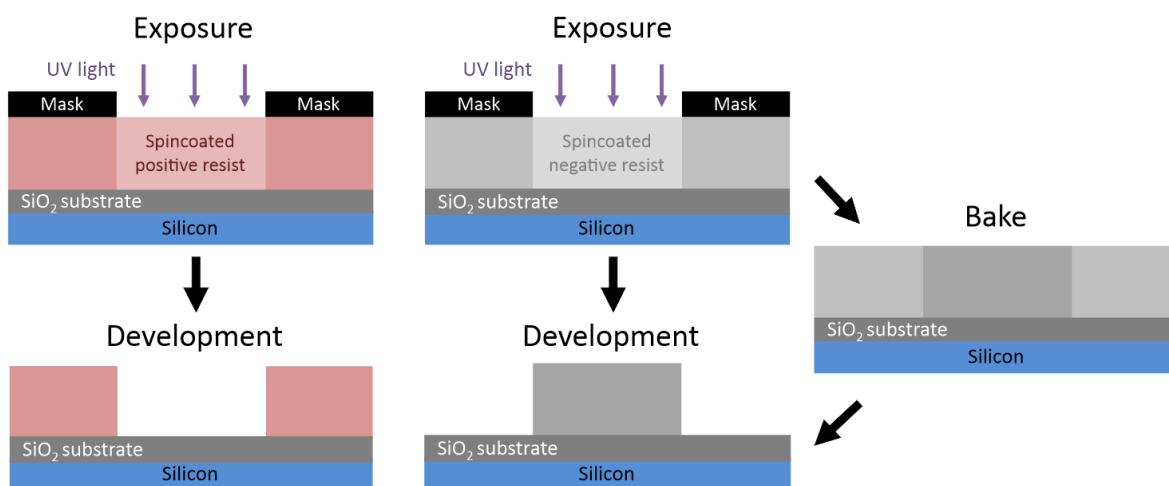


Figure 1: A side-view comparison of generic photolithography processes for positive and negative resists in the ideal case. Photolithography with a positive resist requires a single softbake step before exposure, while for negative resists a second baking step is required after exposure (Thicknesses shown not to scale).

This section details some of the standard photolithography procedures used in the quarter wafer processing detailed in Section . Photoresists, also referred to here as “resists”, are UV light-sensitive polymeric resins used for photolithography. Both positive and negative photoresists

were used in various fabrication processes. Positive resists are made soluble in alkalines by UV light exposure, meaning exposed areas are removed in the development process. Conversely, negative resists are cross-linked by exposure and a post-exposure bake step. The unexposed areas of the negative resist are then removed in the development process [@Microchemicals]. Figure 1 gives a visual representation of these differences.

The specific photoresist selected for photolithography depends on the specific use case. The types used in this thesis are positive and negative AZ® photoresists (AZ® 1518, Microchemicals GmbH; AZ® nLOF 2020, Microchemicals GmbH) and SU-8 (SU8-2150, Kayaku Advanced Materials, formerly Microchem). The AZ® resists used here have a minimum film thickness of $1.5 \mu\text{m}$ [@Microchemicals], while the SU8-2150 has a minimum film thickness of $0.5 \mu\text{m}$ [@Kayaku]. Positive resists which have not been thermally crosslinked will soften at higher temperatures ($\gtrsim 100^\circ\text{C}$ for AZ® 1518), leading to a rounded profile. This is not the case for negative resists, which are more thermally stable [@Microchemicals]. Each resist therefore has a different cross-section profile, as shown in Figure 2.

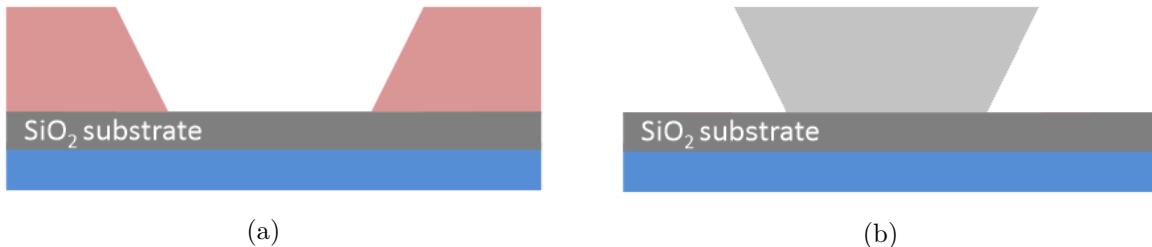


Figure 2: The overcut profile of a positive resist pattern is shown in (a). The undercut profile in (b) is ideal for thin-film metal deposition and subsequent patterned removal, known as “lift-off”. Each profile has had the central region of the substrate exposed to UV light prior to development.

If metal deposition is performed on a positive resist, some metal can collect on the outwardly-sloped sidewalls of the resist (see Figure 2) which forms significant spikes on the edges of the deposited metal upon lift-off. On the other hand, metal cannot collect on top of the inwardly-sloped negative profile sidewalls, which avoids the formation of large edge spikes. Therefore, the negative resist profile is more suited to metal or metal oxide deposition and lift-off processes, though the process is more sensitive to human error due to requiring more processing steps than positive resist [@Microchemicals]. Finally, when it is suitably processed SU-8 is considered to be more stable and biocompatible than other photoresists [@Albarghouthi2022]. It is especially biocompatible when chemically modified via processes such as isopropanol sonication and O₂ plasma treatment [@Chen2021].

All photolithographic exposure was performed using a Karl Suss MJB3 Contact Aligner with a USHIO super-high pressure 350 W mercury lamp (USH-350DS, Japan). When performing photolithography, the intensity reading from the aligner was $20.8\text{--}24.2 \text{ mW/cm}^2$ (Note however

that an external photometer reading at 400 nm found an intensity output of 17.2 mW/cm² when the aligner read 21.0 mW/cm²).

In general, photolithography procedures should be performed under yellow lighting, as light wavelengths from 320 – 450 nm can promote reactions in the photoresist used. Aging of photoresist over time can also significantly affect the photolithography process, and therefore all processes should be re-optimised regularly over time to give the desired result [Microchemicals]. The range in processing times for some steps of the processes used here are largely due to the effects of aging on the photoresist.

The step-by-step processes for each resist are detailed in the subsequent sections.

AZ® 1518 photoresist

1. Spincoat at a final speed of 4000 rotations per minute (rpm) for 1 minute, with an initial acceleration of 500 rpm/s (notes: clean the substrate with acetone, isopropanol (IPA) and nitrogen before spincoating; use only the minimum amount of photoresist required to fully cover the wafer surface; avoid any gaps or bubbles in the photoresist).
2. Softbake 2 – 4 minutes at 95°C on the hotplate (2 min for individual devices, 4 min for a quarter wafer)
3. Mask expose for 10 – 12 s (note: clean mask with acetone/IPA and N₂ dry before use)
4. Develop with 3 parts AZ® 326 (2.38 % TMAH metal-ion free developer, Microchemicals GmbH) in 1 part deionised (DI) water for 30 – 45 s (note: rinse for 10 – 15 s in one development solution, then perform the rest of the development in clean developer for a cleaner profile; lightly agitate the solution throughout the development process)
5. Rinse device for 30 s in DI water to remove excess developer, then dry under nitrogen

AZ® nLOF 2020 photoresist

1. Spincoat at final speed of 3000 rotations per minute (rpm) for 1 minute, with an initial acceleration of 500 rpm/s (notes: clean the substrate with acetone, isopropanol (IPA) and nitrogen before spincoating; avoid any gaps or bubbles in the photoresist)
2. Softbake for precisely 60 s at 110°C on the hotplate
3. Mask expose for 2.7 – 3 s (note: clean mask with acetone/IPA and N₂ dry before use)
4. Post-exposure bake for precisely 60 s at 110°C on the hotplate to cross-link exposed resist
5. Develop with 3 parts AZ® 326 in 1 part DI water for 60 – 70 s (note: rinse for 30 s in one development solution, then perform the rest of the development in clean developer for a cleaner profile; lightly agitate the solution throughout the development process)

6. Rinse device for 30 s in DI water to remove excess developer, then dry under nitrogen

SU8-2150 photoresist

1. SU-8 was diluted in cyclopentanone until viscosity was low enough to spincoat on substrate and then sonicated at 50°C for 3 – 4 hours (Note: The dilution ratio used was ~1 part SU-8 to 5 parts cyclopentanone. However, the age of the SU-8 may mean that significant evaporation had occurred prior to use, and the amount of SU-8 actually present is underrepresented by this ratio)
2. Spincoat first with a final speed of 500 rpm (acceleration 500 rpm/s) for 10 seconds, followed by spincoating at 4000 rpm (acceleration 7500 rpm/s) for 40 s.
3. Softbake for 10 minutes at 95°C on the hotplate
4. Mask expose for 6 – 8 s (note: clean mask with acetone/IPA and N₂ dry before use)
5. Post-exposure bake for 10 minutes at 95°C on the hotplate to cross-link exposed resist
6. Develop with SU-8 developer (Kayaku Advanced Materials, formerly Microchem) for 10 – 15 s, then clean in IPA for 30 s, repeat this step once then dry under nitrogen (note: lightly agitate the solution throughout the development process)

Quarter Wafer Processing of Carbon Nanotube and Graphene Field-Effect Transistors

Photolithography was used to define eight channel regions on each device and subsequently to define metal contacts for each of these channels. A schematic demonstrating these photolithography processes on a quarter wafer is shown in Figure 3. Masks for photolithography were designed in-house using LayoutEditor CAD software and patterned externally with a UV laser writer.

Thermal evaporation was used when depositing chromium (Cr-plated tungsten rods, Kurt J. Lesker) and gold (Au wire, 99.99%, Regal Castings Ltd.), while electron beam evaporation was used when depositing titanium (Ti pieces, 99.99%, Kurt J. Lesker) and metal oxides (*e.g.* Al₂O₃ pieces, 99.99%, Kurt J. Lesker). Metal and metal oxide deposition was performed using an Angstrom Engineering Nexdep 200 Vacuum Deposition System. Deposition thickness was monitored by a Inficon quartz piezoelectric sensor and controlled using an Inficon Deposition Controller. Electron beam power was provided by a Telemark TT-6 power supply. For metals, the chamber was initially evacuated to a pressure 5×10^{-6} mTorr, while for metal oxides the chamber was initially evacuated to a pressure of 1×10^{-5} mTorr. After evaporation, the chamber was cooled and vented with nitrogen.

Carbon nanotube network field-effect transistors were fabricated using 4-inch *p*-type (B-doped) silicon wafers with either a 100 nm or 300 nm SiO₂ layer (WaferPro LLC) as the substrate.

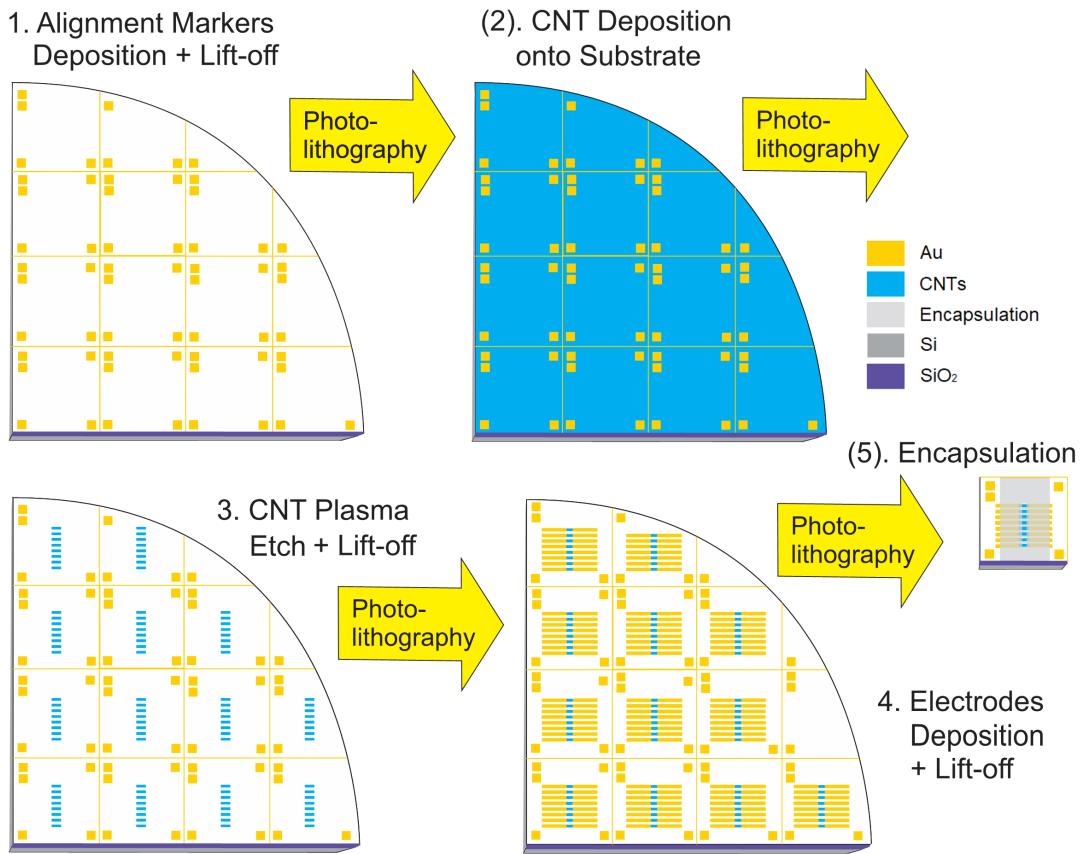


Figure 3: The photolithographic processes used for fabrication of both carbon nanotube and graphene devices (graphene devices were fabricated individually for every step. Step #2 is passed over for graphene devices).

Devices intended for backgated measurements were fabricated with a 100 nm SiO₂ layer. Before photolithographic processing, the wafers were spin-coated with AZ® 1518 photoresist, placed photoresist-side down onto a cleanroom wipe, fixed in place using vacuum suction, then cleaved into quarters using a diamond-tipped scribe tool. For fabrication performed before June 2023, the protective photoresist layer was then removed by soaking the quarter-wafers in acetone for 15 minutes, then rinsed with isopropyl alcohol (IPA) and dried with N₂ gas. However, for complete removal of photoresist, we found it was necessary to flood expose the wafer with the Karl Suss Aligner for 1 min and then place it in AZ326 developer for 3 min, as discussed further in [?@sec-photoresist-contamination](#).

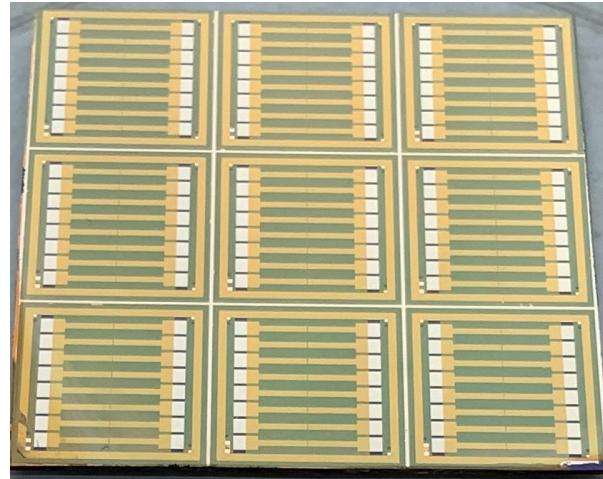
Graphene field-effect transistors were fabricated using 300 nm SiO₂/p-type Si substrates covered with a monolayer of mechanically transferred CVD graphene (Advanced Chemical Supplier). This substrate was cleaved into equal-sized square chips before photolithography, with side length between 11.6 – 11.7 mm, subject to variability in wafer size. The same cleaving process outlined in Section was used for cleaving the chips, but the photoresist was not rinsed off after cleaving. Devices were exposed to a brief burst of N₂ gas to remove any dust from the cleaving process from the surface of devices. When not being used in photolithography, graphene-based devices were stored in a vacuum desiccator to prevent the quality of the graphene deteriorating with exposure to air over time. The limited adhesion of graphene to the wafer meant that photolithographic processing had to be performed particularly carefully when fabricating graphene devices.

From Jul 2023 onwards, after each photolithography step using negative resist, quarter wafers/chips were placed in AZ® 326 or SU8 developer for 3 min to ensure complete removal of photoresist residue. For each step with positive resist, the same procedure was performed but with a flood exposure with UV light for 1 min before being placed in developer. The exception to this rule was for devices with an aluminium oxide layer present. Tetramethylammonium hydroxide (TMAH), the active ingredient of AZ® 326, etches through aluminium oxide and causes electrical shorts through the dielectric layer [[@Oh2011](#); [@Ali2021](#)]. A further discussion showing the results of this process is given in [?@sec-photoresist-contamination](#).

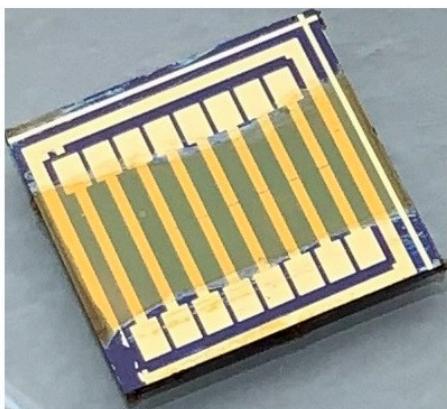
Figure 4a shows a completed quarter-wafer of carbon nanotube field-effect transistors, where partial (unusable) devices at the edges of the wafer have been cleaved off so that only a square of nine devices remains. An individual FET device after the completed fabrication process is shown in Figure 4b, and Figure 4c shows cross-section and top view schematics of the completed device with the component parts labelled.

Alignment Markers

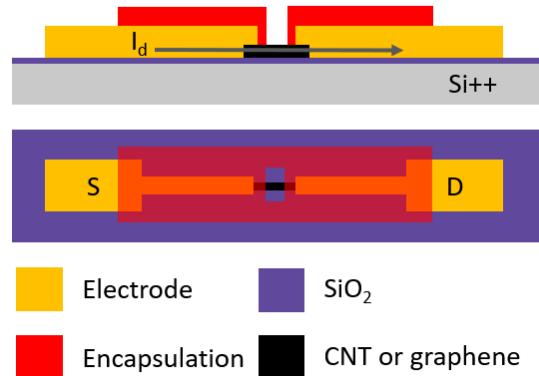
Metal alignment markers were deposited in order to accurately align the device channels with device electrodes in subsequent photolithography steps. These alignment markers were asymmetric to indicate the orientation of the device for subsequent photolithography steps and



(a)



(b)



(c)

Figure 4: A finished quarter-wafer with the unusable edges cleaved off is shown in (a), while an individual carbon nanotube field-effect transistor device is shown in (b). The component parts of the field-effect transistor are labelled on device cross-section and channel top view schematics in (c).

electrical characterisation. In later discussion, channel 1 is defined as the channel placed closest to the large double square alignment marker feature. For carbon nanotube quarter wafers, alignment markers were deposited either directly before or after carbon nanotube deposition (see Section for discussion). For graphene devices, alignment markers were deposited directly after cleaving using the protective photoresist layer spincoated prior to cleaving. AZ® 1518 was used for alignment marker photolithography.

For carbon nanotube devices made before Jun 2022, chromium was used as an adhesive layer for gold, while for all graphene devices and carbon nanotube devices made after Jun 2022, titanium was used as the adhesive layer. Metal layer thickness values quoted here are as stated on the Inficon controller. Without first corroborating these measurements with the Dektat profiler, these values should be treated as being strictly nominal. For chromium/gold depositions, 10 nm of chromium was deposited followed by a 100 nm Au layer. For titanium/gold depositions, a 10 – 20 nm of titanium was deposited followed by a 50 nm Au layer. Devices were then soaked in acetone for at least 2 hours for photoresist lift-off, washed in IPA and dried with nitrogen. The use of titanium gave rise to a cleaner lift-off and improved gold adhesion. Using a relatively thin gold layer (50 nm nominal instead of 100 nm) proved to still be clearly visible but to a cleaner lift-off. Profiler measurements of combined metal layer thicknesses after lift-off are described in Section .

Deposition of Carbon Nanotubes

Carbon nanotubes were deposited before the alignment markers photolithography step on all wafers fabricated between Aug 2021–Feb 2023, while devices fabricated before Aug 2021 and after Feb 2023 had the alignment markers photolithography step performed before the deposition of carbon nanotubes. The process order was first switched in Aug 2021 as this order led to faster processing times. However, the order was switched back in Feb 2023 to minimise the exposure of carbon nanotubes to photolithographic chemical processes.

*** Solvent-Based**

The solvent-based deposition process for the carbon nanotube network in the second fabrication protocol is as follows. 10 mg of 2-mercaptopurine (99%, Sigma-Aldrich) was dissolved in 1 ml ethanol by sonication until clear. Quarter wafers were sonicated in acetone for 3 min, then exposed to O₂ plasma at 100 W for at least 2 min in a small plasma cleaner (Plasma Etch, Inc., PE-50 Compact Benchtop Plasma Cleaning System) or reactive ion etcher (Oxford Instruments, Plasmalab® 80 Plus) under 300 mTorr pressure. The cleaned SiO₂/Si surface was then coated with 2-mercaptopurine for 10 minutes, rinsed with ethanol to remove residual 2-mercaptopurine, and then nitrogen dried.

Meanwhile, 5 µg of 99% semiconducting carbon nanotube bucky paper (NanoIntegris, IsoNanotubes S-99) was dispersed in 10 mL of anhydrous 1,2-dichlorobenzene (DCB, Sigma Aldrich)

by ultrasonication until no particles were visible to the naked eye. During this time, the ultrasonic bath temperature was kept between 20 – 30°C or the buckypaper would not disperse successfully. The substrates were then placed into a dish with CNT-DCB suspension and left covered for 1 hour, dipped into ethanol for 10 min to remove residual solvent and any unattached carbon nanotube bundles, and then dried with nitrogen.

* Surfactant-Based

Two different approaches were used to attach the surfactant-dispersed carbon nanotubes (CNTs) to the substrate surface. The first approach was a simple drop-casting method, while the second was performed in the presence of steam ('steam-assisted'). In both approaches, the quarter wafers were first rinsed with ultrapure deionised water (DI water), acetone and IPA. Next, they were placed into a small plasma cleaner (Plasma Etch, Inc, PE-50 Compact Benchtop Plasma Cleaning System) or reactive ion etcher (Oxford Instruments, Plasmalab 80 Plus) and exposed to O₂ plasma at 100 W for at least 2 min under 300 mTorr pressure to make the surface hydrophilic. 1 mL of poly-L-lysine (PLL) was immediately deposited onto each quarter wafer and left for 5 minutes. The quarter wafers were then rinsed for 30 s with DI water and dried with N₂ gas. The presence of the PLL on the plasma cleaned surface strengthens the surface adhesion of semiconducting single carbon nanotubes after the surfactant dispersion has been dropcast onto the substrate.

For carbon nanotube network films deposited in surfactant without steam present, 2 mL of IsoNanotubes-S 90% or 99% dispersion (NanoIntegris) was decanted into a small bottle and sonicated for 5 s to break up bundles of CNTs. (Note: The composition of the surfactant used in the dispersion is proprietary to NanoIntegris.) An even spread of 400 µL carbon nanotube dispersion was placed in the centre of the PLL-functionalised quarter wafer, covered with a glass dish and left for 10 minutes. The dispersion was then rinsed off with DI water and IPA, and the quarter wafer was dried with N₂ gas. Next, the quarter wafer was annealed in a vacuum oven at 150° C for 1 hour to remove residual surfactant. This method would often lead to an inhomogeneous spread of CNTs across the quarter wafer surface, detailed further in section [?@sec-cnt-deposition-effects](#).

For carbon nanotube network films deposited in surfactant in the presence of steam, 2 mL of IsoNanotubes-S 90% or 99% dispersion (NanoIntegris) was decanted into a small bottle and burst-sonicated once (on then off again) to break up bundles of carbon nanotubes. 75 mL of 95° C water was then placed into a glass dish on a hotplate held at 95° C. After this, the PLL-functionalised quarter wafer was placed in the centre of an insulating surface on the same hotplate. The carbon nanotube dispersion was carefully spread across the surface of the wafer without spilling any over the wafer edges. The wafer on the insulating surface and glass dish were then left under the same glass dish for 2 minutes to expose the wafer to steam from the glass dish. The use of an insulating surface meant that the wafer and dispersion were not heated from below while exposed to steam. The steam-assisted deposition setup is shown in Figure 5.

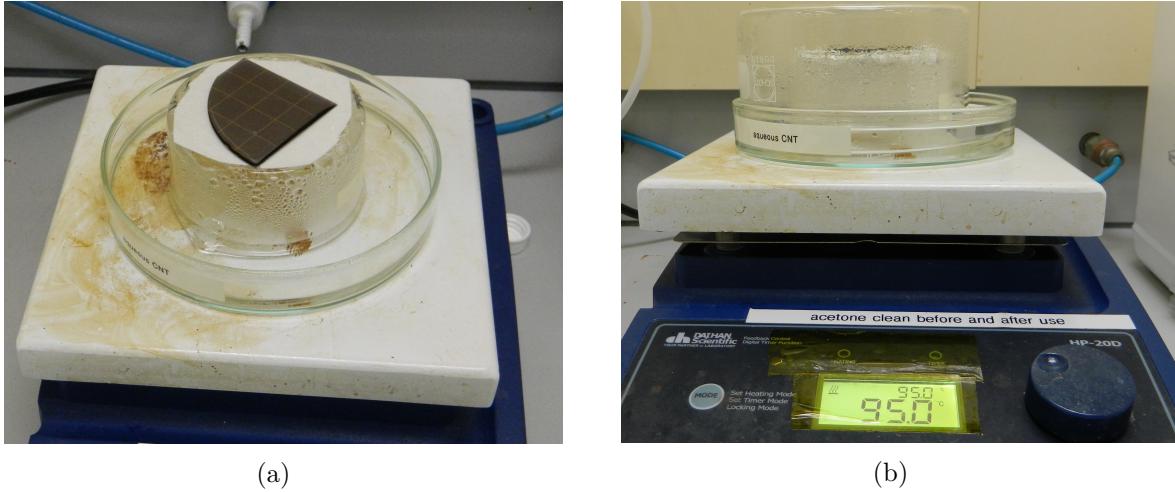


Figure 5: Top view (a) and side view (b) of the steam-assisted method setup, with and without the glass steam cover above the quarter wafer.

The carbon nanotube dispersion was then rinsed off the wafer with DI water, ethanol, acetone and IPA, and then the quarter wafer was dried with N₂ gas. As in the original method, the quarter wafer was then annealed in a vacuum oven at 150° C for 1 hour to remove residual surfactant. This method gave an even spread of CNTs across the quarter wafer surface, leading to a greater consistency in performance between devices. Further details can be found in [?@sec-cnt-deposition-effects](#).

Channel Etching

Eight channel features, each 1000 μm in length and 100 μm in width with a pitch of 1200 μm , were patterned using AZ® 1518 photolithography on each carbon nanotube or graphene-covered substrate. Unwanted nanomaterial not covered with photoresist was then etched away with 200 W oxygen plasma at 600 mTorr using a reactive ion etcher or RIE (Plasmalab® 80 Plus, Oxford Instruments). The etch time was 3 minutes for carbon nanotube quarter wafers, and 1 minute for graphene chips. The protective photoresist was then removed by soaking in acetone for at least 5 minutes.

Source and Drain Electrodes

The source and drain electrodes for each channel were patterned using photolithography with either AZ® 1518 photoresist (pre-Mar 2023) or AZ® nLOF 2020 photoresist (post-Mar 2023). Before metal deposition, the developed photoresist pattern was exposed to O₂ plasma at 50 W for up to 5 s or at 20 W for 20 – 25 s in a PE-50 plasma cleaner (Plasma Etch, Inc.) to

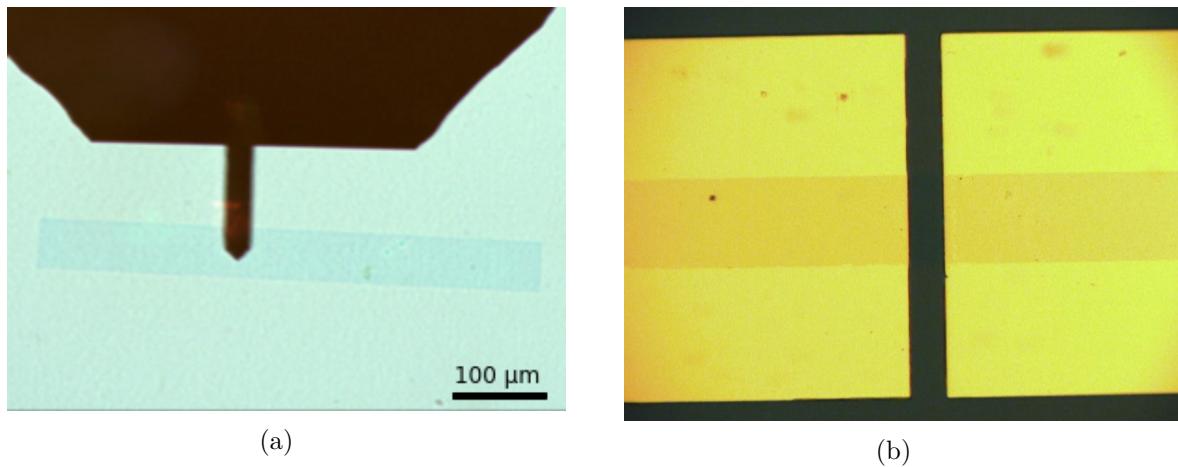


Figure 6: A graphene channel after the plasma etch step is shown in (a), and (b) shows another graphene channel after the metal electrode deposition and liftoff step.

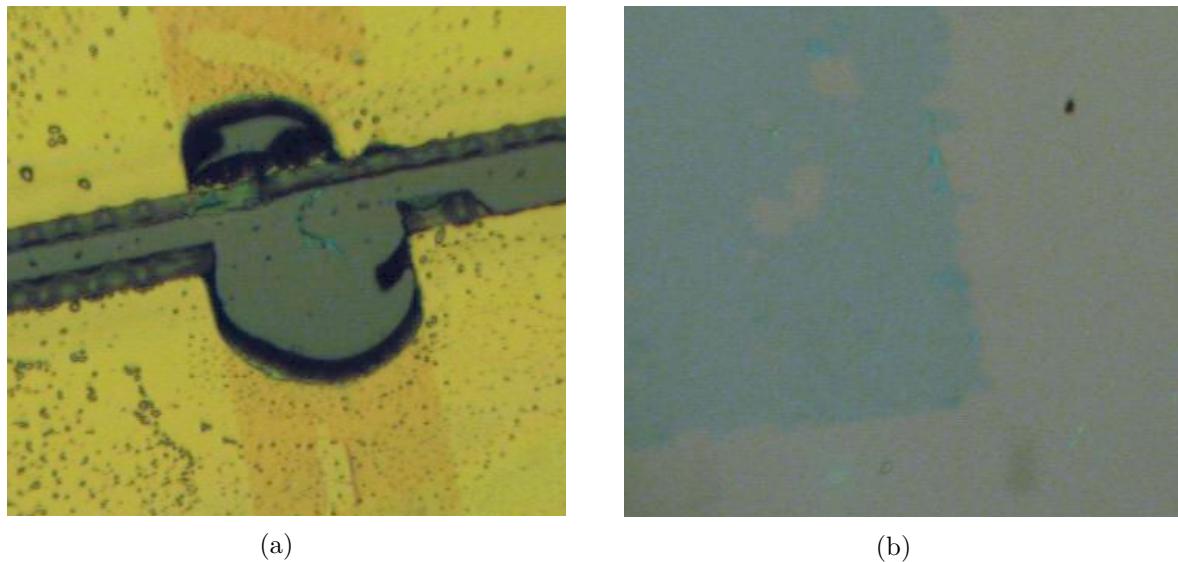


Figure 7: Damage to the gold electrode in the graphene channel region after dimethyl sulfoxide lift-off is shown in (a), while (b) shows damage to a graphene film (blue-green region) after dimethyl sulfoxide lift-off.

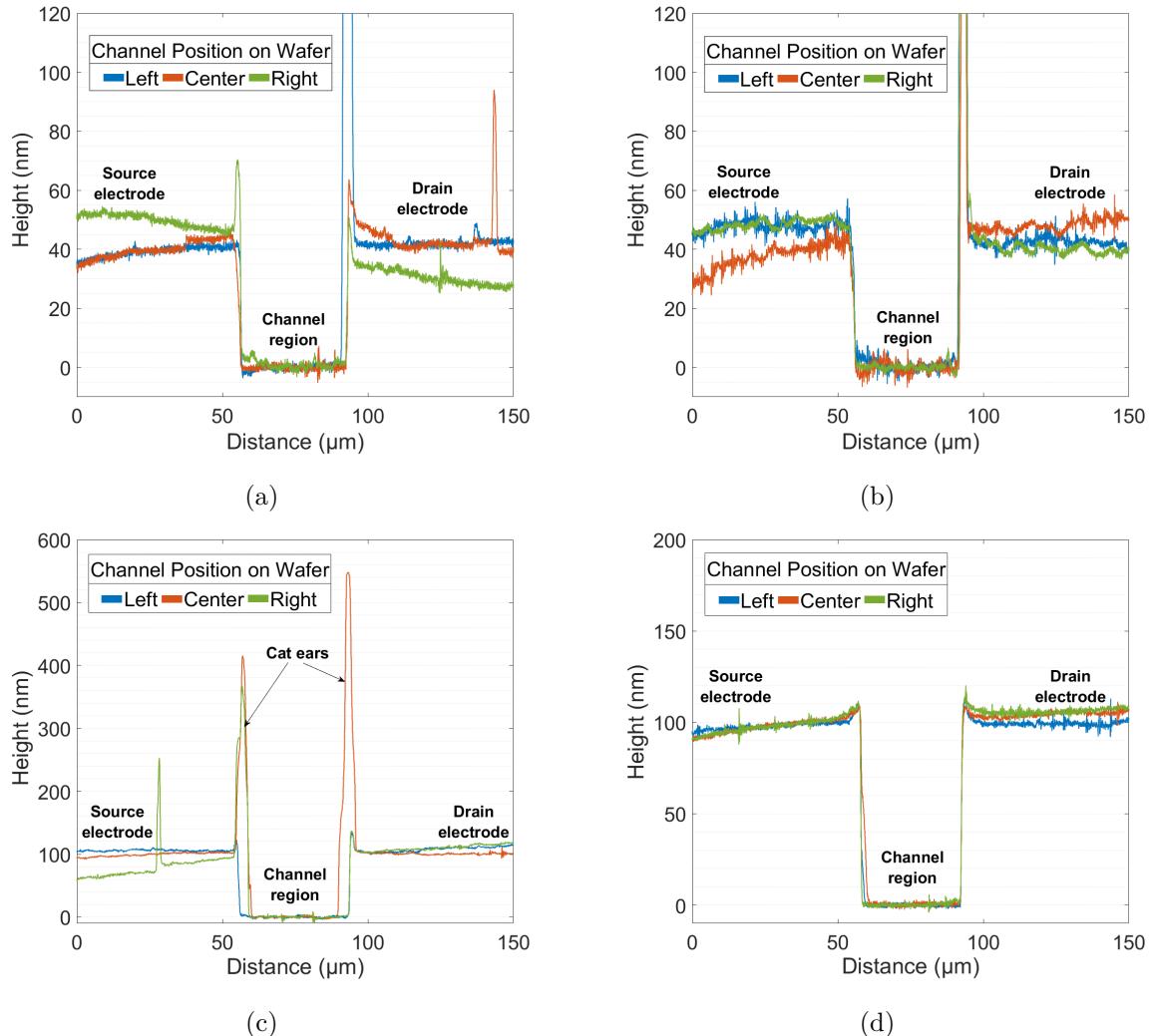


Figure 8: The Dektat height profile measurements for source and drain electrodes taken at different locations on four different quarter wafers are shown here. Chromium was used as an adhesion layer for the wafer in (a), while titanium was used as the adhesion layer in (b) and (c). AZ® 1518 photolithography was used for patterning before metal deposition on both quarter wafers, which led to the formation of edge features or “cat ears”, with (c) illustrating the full height of these features. In comparison, (d) shows the profile of electrodes from a quarter wafer patterned with AZ® nLOF2020, where edge features are greatly reduced.

remove residual photoresist on the developed regions and ensure a clean lift-off. After metal deposition, wafers/devices were soaked in acetone for at least 2 hours for photoresist lift-off, washed in IPA and dried with nitrogen.

As with the alignment markers deposition (see Section), before Jun 2022 chromium was used for the gold adhesion layer, and after Jun 2022 titanium was used. Adhesion layers are required to stick metals such as gold and platinum to silicon dioxide [Guarnieri2014]. A 20 nm nominal titanium layer instead of 10 nm nominal was found to give better electrode adhesion, and devices after Feb 2023 were made using this thicker adhesion layer. Good electronic contact could be made with electrodes with a nominal gold layer thickness of 60 – 100 nm, and a Au layer nominally 100 nm thick was most commonly used.

Dimethyl sulfoxide (DMSO) was sometimes used in electrodes lift-off instead of acetone between Jul 2021 and Feb 2023 because of its effectiveness as a photoresist stripping agent. However, it was abandoned due to some indications it was unsuitable for the devices being fabricated, as shown in Figure 7 and also as detailed in ?@sec-cnt-deposition-effects. It is possible that heat from the electrodes deposition sometimes crosslinked residual photoresist on the nanomaterial, and then during lift-off was removed together with any attached nanomaterial by the DMSO. However, it is also possible that prolonged exposure to DMSO alone was sufficient to detach nanomaterial from the substrate. Therefore, acetone was the preferred agent for lift-off despite being a less efficient stripping agent than DMSO.

Example height profiles of quarter wafer channels taken using a Veeco Dektat 150 profiler are shown in Figure 8. AZ® 1518 photoresist was used in Figure 8a and Figure 8b for photolithographic patterning. A 10 nm adhesion layer and 100 nm Au layer were used for each quarter wafers to ensure a consistent comparison. From these figures, we find an measured Cr/Au electrode height of 42 ± 1 nm and an measured Ti/Au electrode height of 48 ± 2 nm, slightly less than half the respective heights stated on the Inficon Deposition Controller.

Although using AZ® nLOF 2020 photolithography involves more processing steps, it gave rise to more cleanly-defined electrodes with a more consistent height profile. Often electrode deposition using AZ® 1518 photoresist would lead to sharp vertical spikes along the edge of the electrode, as seen in Figure 8c. These edge spikes or “cat ears” can partially or fully protrude through thin encapsulation materials such as SU8 and Al₂O₃, leading to significant leakage currents from the electrodes into the FET top gate. This effect is due to the profile of positive resists being suboptimal for lift-off processes, as discussed in Section .

The height profile corresponding to a wafer with electrodes fabricated using AZ® nLOF 2020 is shown in Figure 8d. A 20 nm titanium adhesion layer and 100 nm Au layer were used for both Figure 8c and Figure 8d to ensure a consistent comparison, resulting in a measured electrode height of 103 ± 2 nm for both wafers. By comparing these figures, we see AZ® nLOF 2020 photoresist has a more consistent electrode height profile across the wafer surface than the wafer which used AZ® 1518 resist. The measured edge features for the AZ® 1518 resist electrodes vary in size from 20 nm to 450 nm above the bulk electrode surface, whereas the edge features for the AZ® nLOF 2020 resist do not exceed 14 nm in height.

Encapsulation

Several different approaches were used for the encapsulation, or contact protection, of devices. The encapsulation of graphene and carbon-nanotube transistors for biosensing is essential to improve transistor characteristics, passivate the electrodes and ensure only the nanomaterial region is active during biosensing, as discussed in [?@sec-biosensor-methods](#).

Before encapsulation photolithography the carbon-nanotube network quarter wafers were cleaved into individual 11 mm × 11 mm chips, using the cleaving process outlined in Section . Cleaving the devices at this step simplified mask alignment and ensured consistent thickness across photoresist encapsulated devices.

Two different photolithography masks were used for encapsulation photolithography in this work, with different exposed areas of active nanomaterial. The first mask was used for devices made before Jan 2023, and was designed to leave a region of 500 μm × 10 μm unencapsulated for each channel. The second mask was used exclusively after Jan 2023, and was designed to leave a region of 200 μm × 20 μm unencapsulated for each channel. This change was made to double the area of carbon nanotubes exposed to electrolyte while halving the area of SiO₂ dielectric exposed to electrolyte during aqueous sensing.

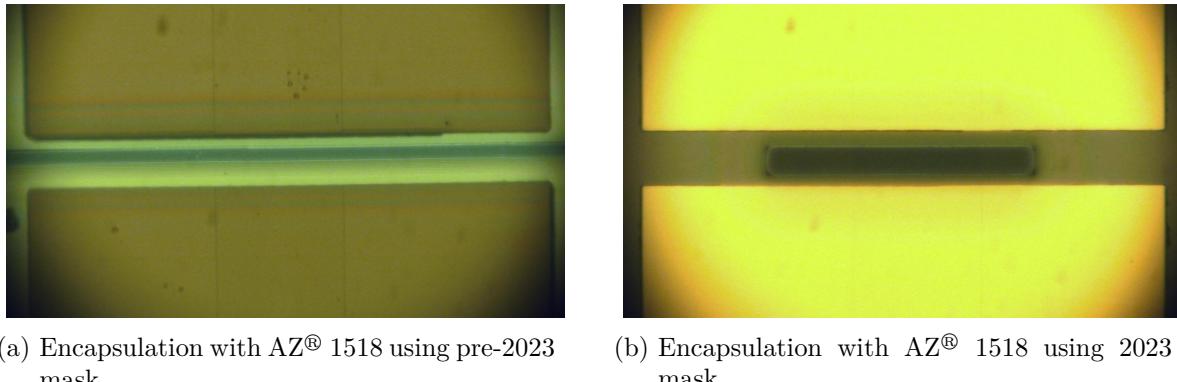


Figure 9: Microscope images of carbon nanotube devices after encapsulation photolithography with hardbaked AZ® 1518.

A side-by-side microscope comparison of hardbaked AZ® 1518 processed with each mask is given in Figure 9, while a Dektat profile comparison corresponding to Figure 9 is shown in [?@fig-old-new-mask](#). The profiles corresponding to the mask used after Jan 2023 clearly exhibit greater device-to-device consistency, partly due to the mask requiring a greater level of accuracy when aligning the encapsulation pattern with the electrode channel. The larger feature size also means development time has less of an impact on the quality of the encapsulation opening.

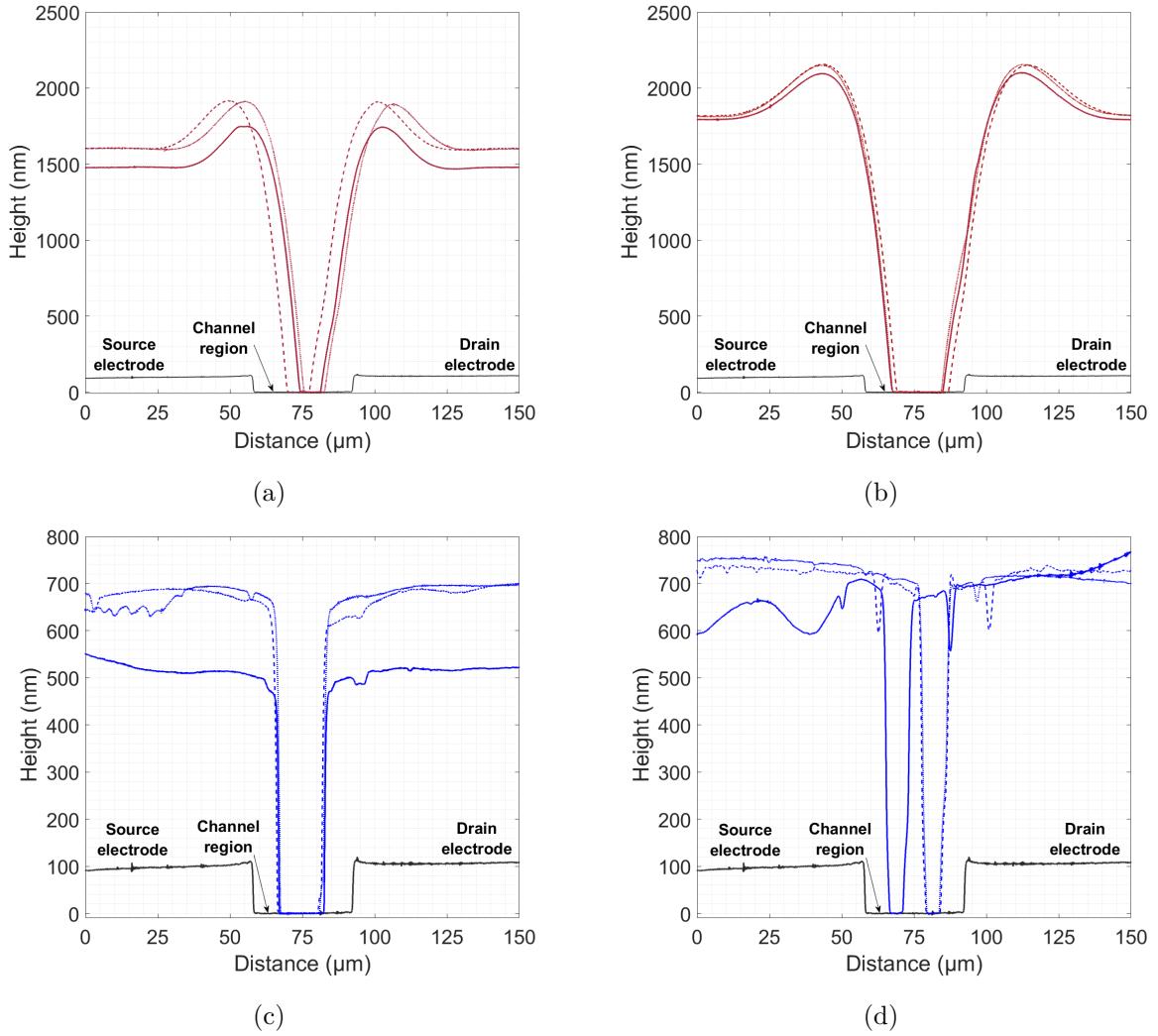


Figure 10: Dektat of carbon nanotube devices after encapsulation photolithography using hard-baked AZ® 1518 and SU-8 2150, taken from various devices. (a) and (c) show photolithography performed with the old, pre-2023 mask, using AZ® 1518 and SU-8 2150 respectively. (b) and (d) show photolithography performed with the new mask from 2023 onwards, using AZ® 1518 and SU-8 2150 respectively.

* Photoresist encapsulation

Two types of photoresist were initially trialled for encapsulation of carbon nanotube network devices, AZ® 1518 and SU8-2150. Both AZ® 1518 [@Thanihaichelvan2018; @Thanihaichelvan2019; @Shkodra2021] and SU-8 have been previously used for device encapsulation, with SU-8 noted for being particularly stable and biocompatible [@Lee2006; @Chen2021; @Albarghouthi2022].

Once developed, the photoresist pattern was exposed to O₂ plasma at 50 W for up to 5 s or at 20 W for 20 – 25 s to remove excess photoresist from the encapsulation opening. Devices were then hardbaked at 200°C for 1 hour to fully crosslink the encapsulation layer. This crosslinking ensured subsequent device exposure to solvent did not remove the photoresist encapsulation.

The exposed region clear of AZ® 1518 resist was $6.8 \pm 0.3 \mu\text{m}$ in width when using the old, pre-2023 mask, while the exposed region was $16.6 \pm 0.4 \mu\text{m}$ when using AZ® 1518 with the new mask from 2023, as seen in Figure 10a and Figure 10b. However, the exposed region was reduced for the SU-8 encapsulation relative to the AZ® 1518, with an width of only $3.6 \pm 0.5 \mu\text{m}$ for the pre-2023 mask, as seen in Figure 10d. Photoresist development using SU-8 was significantly more time-sensitive than for the AZ® 1518. This meant when the development time was increased to create a wider encapsulation opening, it was difficult to avoid removing large areas of photoresist across the entire surface of the encapsulation. This meant using the new mask from 2023 was especially important for maximising the exposed channel region of SU-8 devices. From Figure 10c, we see the new mask from 2023 with the SU-8 resist gave a significantly improved width of $13.8 \pm 1.0 \mu\text{m}$ for the exposed region.

A relatively thin SU-8 encapsulation layer could be deposited when compared to the AZ® 1518 encapsulation profile. From Figure 10, we see that the AZ® 1518 encapsulation layer had a average height of $1.7 \pm 0.2 \mu\text{m}$, while the SU-8 encapsulation layer had a average height of $680 \pm 20 \text{ nm}$. The SU-8 also had much less significant edge features than the AZ® 1518, regardless of the profiles of the source and drain electrodes.

As noted previously, for both resists the overall profile was more consistent for the new, 2023 mask from device to device than for the old pre-2023 mask.

AZ® 1518 encapsulation was used for all graphene devices fabricated.

* Dielectric encapsulation

Another approach taken was encapsulation of electrode channels with a dielectric metal oxide/ceramic layer. A electron beam deposition process was used to deposit a 100 – 150 nm nominal metal oxide layer on devices patterned with the 2023 mask using AZ® nLOF 2020 photoresist. As in Section , the developed photoresist pattern was exposed to O₂ plasma at 50 W for up to 5 s or at 20 W for 20 – 25 s in a PE-50 plasma cleaner (Plasma Etch, Inc.) before ceramic deposition. Before May 2023, devices were left in TechniStrip® MLO 07 (MicroChemicals) for 5 – 10 min for lift-off. However, due to concerns over the impact of the

constituent chemical DMSO on the nanomaterial region (see Figure 7), the lift-off process was altered from May 2023 onwards. After May 2023, devices were soaked in acetone for at least 4 hours and sonicated in clean acetone for 30 – 60 s to lift-off the photoresist, then washed in IPA and dried with nitrogen.

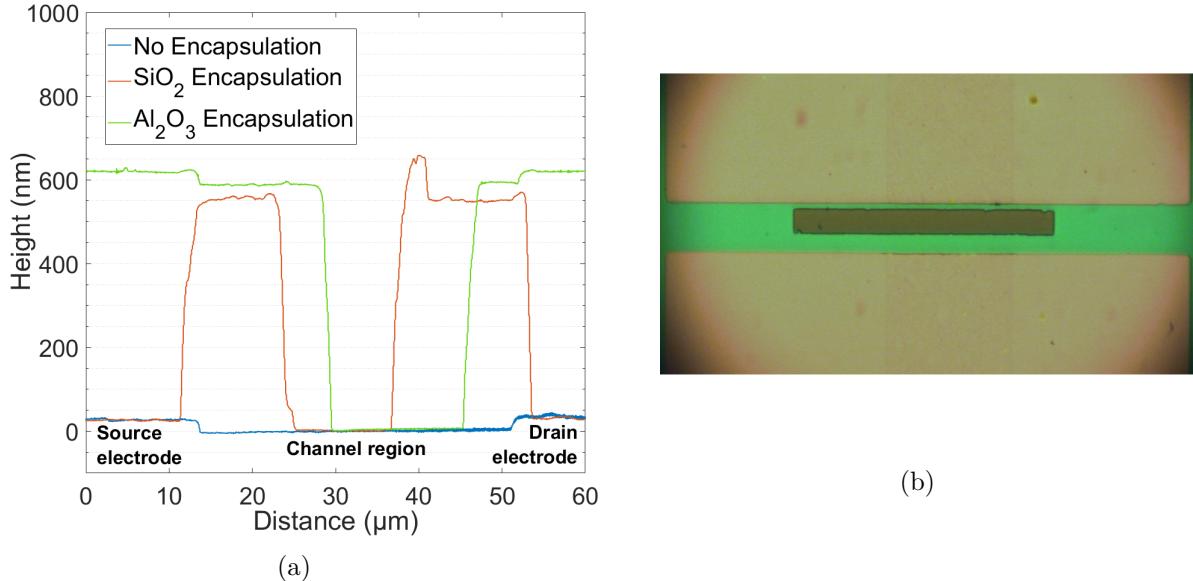


Figure 11: A profile comparison of dielectric materials used for encapsulation is shown in (a), alongside a microscope image of a device encapsulated with aluminium oxide in (b). Note that the layer thicknesses in (a) were from initial tests of the process and are used for illustrative purposes.

The initial attempt at fabricating a dielectric encapsulation layer used silicon dioxide as the dielectric. However, silicon dioxide adheres poorly to gold without an metallic adhesive layer present, as shown in Figure 11a. Aluminium oxide was chosen as an alternative as it sticks well to bulk electrode materials, is heat and chemical resistant, has a relatively high dielectric constant and is bio-compatible [Guarnieri2014; Albarghouthi2022; Kolodzey2000]. Figure 11 shows the aluminium oxide successfully adhered to the electrodes and had a clean profile comparable to that of the SU-8 encapsulation layer after lift-off.

Unfortunately, when aluminium oxide layers which were thicker than ~ 100 nm were deposited, there was found to be a significant drop in current relative to the unencapsulated device. This drop was significant enough to make devices unsuitable for sensing. Meanwhile, devices with encapsulation ~ 100 nm thick had significant gate current leakage through the encapsulation layer when liquid-gated. This leakage was present even when AZ® nLOF 2020 was used for electrode patterning to avoid edge spikes (as discussed in Section). Furthermore, aluminium oxide should not be subsequently exposed to its etchant TMAH, meaning it was difficult to completely remove residual photoresist from device channels after encapsulation. Possible future approaches to ceramic encapsulation are discussed in ?@sec-future-work.

Characterisation via Atomic Force Microscopy

Atomic force microscopy in this thesis was taken using a Nanosurf NaioAFM in dynamic force mode (also known as tapping mode, oscillating mode, acoustic AC mode or intermittent-contact mode). An ACLA probe (AppNano) was used with a tip diameter of 12 nm, height of $14 - 16 \mu\text{m}$ and a nominal cantilever spring constant of 58 N/m. All atomic force microscopy was performed with the Nanosurf NaioAFM on a stabilising table under a Faraday cage to minimise mechanical and electromagnetic interference. A 256×256 pixel resolution was typically used. Imaging was performed in air at room temperature.

Atomic force microscope (AFM) images could not be taken from the small exposed channel region on the encapsulated devices, so were instead taken on a representative carbon nanotube or graphene film sample fabricated on the same wafer as the device being tested. Moisture adversely affected the AFM imaging process. Therefore, films functionalised with biological materials were washed with DI water and gently dried with N_2 before atomic force microscope images were taken.

The open source data analysis software Gwyddion (version 2.59) was used to analyse AFM images. This included levelling the background with the polynomial background removal function, removing scarring and zeroing the z-scale.

Characterisation via Fluorescence Microscopy

Fluorescence microscopy was performed using an Olympus BX63 fluorescence microscope controlled using cellSens imaging software. Microscope objectives used were all Olympus UPLSAPO/UPlanSApo, apochromat objectives which compensate for spherical and chromatic aberrations. Objectives had infinite aperture and a field number of 26.5. Filter cubes used included the Olympus FITC filter (excitation wavelength range: 467 – 498 nm, emission wavelength range: 513 – 556 nm), Texas Red (excitation wavelength range: 542 – 582 nm, emission wavelength range: 604 – 644 nm) and GFP (excitation wavelength range: 604 – 644 nm, emission wavelength range: 502 – 538 nm). The ISO was kept at the lowest available setting, ISO200. All microscopy was performed in darkness with the screen turned away from the microscope. To ensure photobleaching did not adversely affect imaging, images were taken soon after initial exposure to fluorescence and taking repeated photos of the same region was avoided. Various useful and thorough introductions to fluorescence microscopy can be found online [@Nikon; @Zeiss].

Electrical Characterisation

Both back-gated and liquid-gated measurements were taken of carbon nanotube and graphene devices. Liquid-gated measurements were taken using the configuration shown in Figure 12.

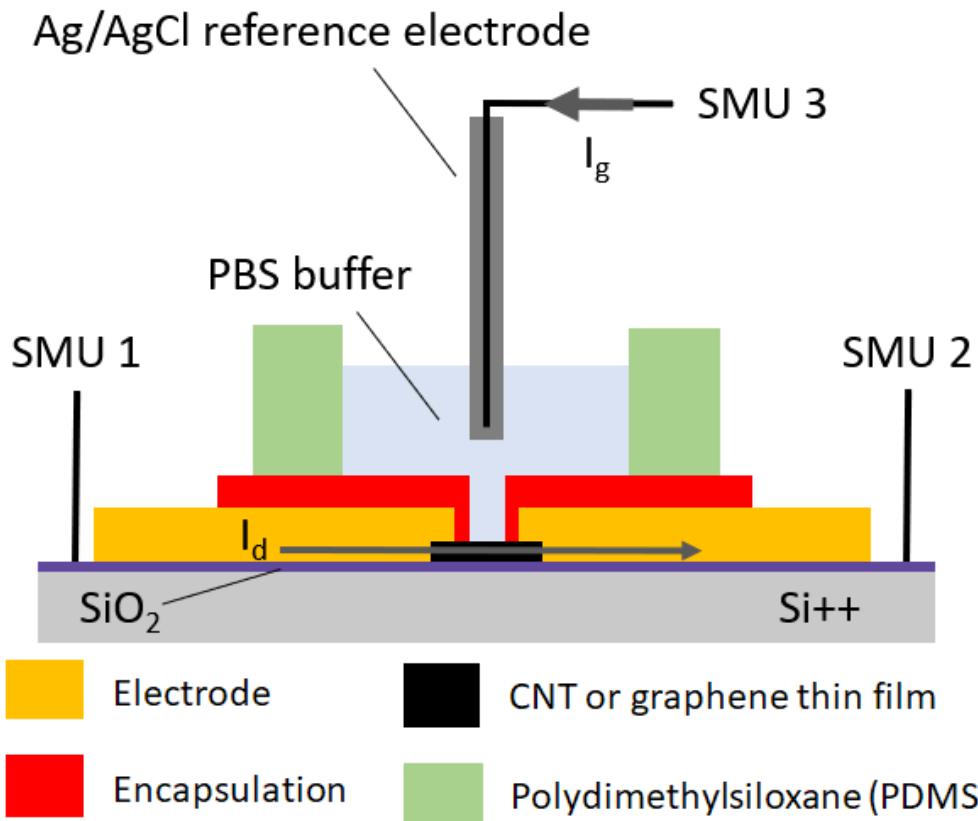


Figure 12: Liquid-gated device schematic showing electrical connections to the three source measure units. V_{ds} is applied between the source SMU (SMU 1) and the drain SMU (SMU 2), while V_{lg} is applied between the gate SMU (SMU 3) and the drain SMU. The drain SMU is held at 0 V or connected to a ground plane. Drain current I_d is measured at the drain SMU, and gate leakage current I_g is measured at the gate SMU.

Back-gated measurements were taken with a copper plane placed underneath the Si/SiO₂ wafer and connected to SMU 3 instead of the reference electrode.

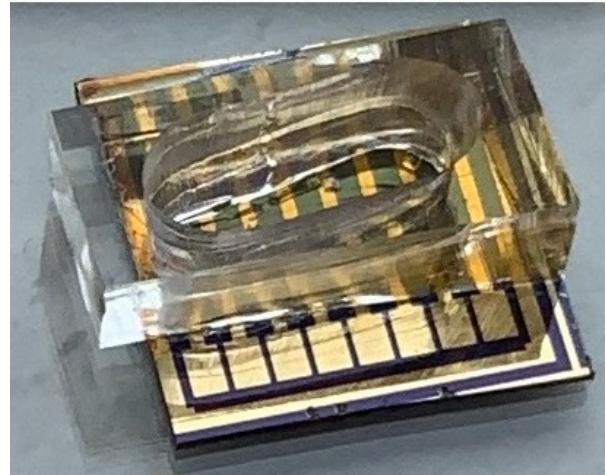
All measurement setups used had the same basic configuration, with two source measure units (SMUs) attached to the source and gate. Voltage from the source and gate SMUs was either kept constant or varied, with only one SMU varied at a time. Three different measurement setups were used for taking these measurements, the Agilent (Keysight/HP) 4156C Semiconductor Parameter Analyser, the Keysight B1500A Semiconductor Device Analyser, and a National Instruments NI-PXIe modular measurement system with a 8 GB PXIE-8821 controller and two NI-4138 source measure units. For measurements with the Keysight instruments, a third, drain SMU was attached and kept at a constant 0 V (as shown in Figure 12).

When using the Agilent 4156C Semiconductor Parameter Analyser or Keysight B1500A Semiconductor Device Analyser for liquid-gated measurements, a Rucker and Kolls with micromanipulators was used to contact the devices; when using the National Instruments NI-PXIe for liquid-gated measurements, a custom-made chip carrier with spring-loaded, pointed-tip, gold-coated pogo pins was used. Ag/AgCl standard electrodes were used as the liquid-gate electrode. The electrode was submerged in 80 μ L of PBS buffer in a polydimethylsiloxane (PDMS) ‘well’ – a flexible structure used to contain the electrolyte solution – with outer dimensions of 12 mm \times 6 mm \times 6 mm. This PDMS well was sonicated in isopropanol for 10 min and thoroughly N₂ dried before use. The microscope images seen in Figure 13 show the PDMS surface before and after this cleaning step. The end of Ag/AgCl standard electrode to be submerged should be rinsed in DI water and left to sit in DI water for 15 minutes before characterisation is performed.

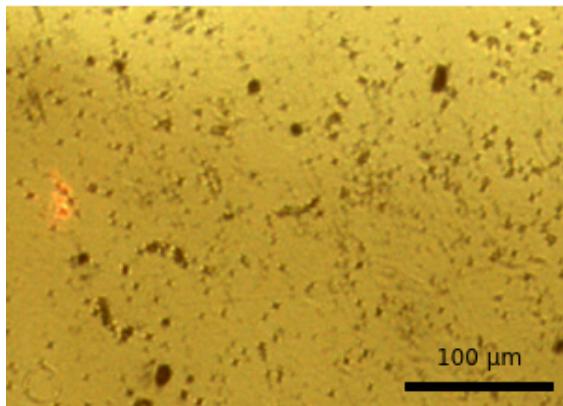
The Agilent 4156C Semiconductor Parameter Analyser and Keysight B1500A Semiconductor Device Analyser were also used for back-gated measurements of devices within the vapour delivery system device chamber. When the lid of this chamber was tightly sealed, it acted a Faraday cage for another custom-made chip carrier with spring-loaded gold-coated pogo pins, able to contact four channel electrode pairs at once. The silicon back of the device was pressed by the pins against a copper block, connected to the gate SMU.

Custom programs for National Instruments LabView 2017 were used for measurements from the Agilent 4156C Semiconductor Parameter Analyser and the National Instruments NI-PXIe. Keysight EasyEXPERT software was used for characterisation with the Keysight B1500A Semiconductor Device Analyser.

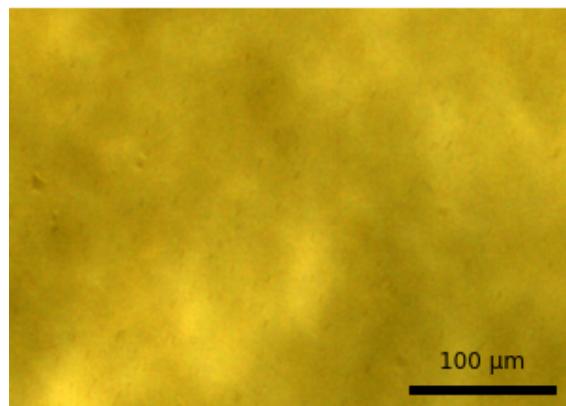
Liquid-gated transfer characteristics of carbon nanotube FETs were measured at V_{ds} = 100 mV and liquid-gated transfer characteristics of graphene FETs were measured at V_{ds} = 1 V, where V_{lg} was swept between -0.5 V and 1 V in both the forward and reverse direction with a step size of either 10 or 20 mV. Backgated transfer characteristics of carbon nanotube FETs were either measured at V_{ds} = 100 mV or V_{ds} = 1 V, where V_{bg} was swept between -5 V and 5 V or -10 V and 10 V in the forward and reverse directions with a step size of 50 mV or 100 mV.



(a)



(b)



(c)

Figure 13: A carbon nanotube field-effect transistor device with a polydimethylsiloxane (PDMS) ‘well’ placed on the device surface is seen in (a), followed by microscope images of the surface of a well before (b) and after (c) isopropanol (IPA) sonication for 10 minutes.

Sensing Measurements

A liquid-gated setup was used for aqueous-phase sensing and a back-gated setup in the vapour delivery system was used for vapour-phase sensing, as described above.

Sensing measurements were performed with constant source-drain and gate voltages. The gate voltage used was chosen by locating the subthreshold region of the device transfer characteristics and choosing a voltage that fell within this region, usually $V_g = 0$ V.

Using the NI-PXIe with the PXIe-2737 module, eight-channel multiplexed current measurements could be taken in rapid succession. An integration time of 200 or 400 ms was used for sampling with each channel, with the actual sampling rate set by the NI-PXIe. In practice this meant a sampling rate of 1.81 s (for 200 ms integration time) or 3.41 s (for 400 ms integration time) for any given channel. A 200 ms integration time meant the time between samples from successive channels varied between 220ms – 230 ms, while a 400 ms integration time meant the time between samples was consistently 426 ms. The Keysight equipment used a constant 1 s sampling interval.

* Aqueous Sensing

Before the sensing process, 200 μ L of PBS was added to the PDMS well and 100-120 μ L of PBS was removed. This initial step was performed to wet the sides of the PDMS well, and check that the attachment of the PDMS well to the device would not unseal when larger volumes of PBS were added during sensing. Before any sensing measurement, a transfer characteristic curve was taken of the liquid-gated device.

From February 2022 onwards, the standard sensing addition series used comprised of a control series and an analyte sensing series. The initial amount of buffered electrolyte in the well was 100 μ L, unless specified otherwise. The total interval for the control series was 1800 s. Electrolyte additions of 20 μ L were made at 100 s, 200 s and 300 s, while electrolyte subtractions of 20 μ L were made at 400 s, 500 s and 600 s. The control series was performed as part of each sensing experiment to test for unwanted responses to electrolyte and to allow baseline drift to settle. Immediately after the control series, a sensing sequence was performed as part of the same continuous measurement set. An initial electrolyte addition was performed at 2100s, to confirm no changes occurred during the control series that would interfere with sensing. Unless specified otherwise, five analyte additions were then made with a time spacing of 300 s, at 2400 s, 2700 s, 3000 s, 3300 s and 3600 s. The experimental series was set to finish at 4000 s. The exact timings, analyte concentrations and gate voltage used in a given sensing sequence are discussed alongside the relevant experimental results.

* Vapour Sensing

A variety of vapour sensing sequences were used in this work, which are discussed in [?@sec-vapour-sensing-biosensors](#) in detail.

Summary

A variety of approaches were trialled when depositing a carbon nanotube network for the fabrication of transistor devices, and the resultant morphology of these networks are discussed in the next chapter. Standard photolithographic methods were used to successfully fabricate carbon nanotube and graphene field effect transistor devices. A range of photolithography types and electrode/encapsulation materials were trialled to find the optimal device composition for sensing, also discussed in the next chapter. Atomic force microscopy, fluorescence microscopy and a variety of electrical measurement setups were used to characterise the devices.