

Developing an Insect Odorant Receptor Bioelectronic Nose
for Vapour-Phase Sensing

by

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A thesis submitted in fulfilment of the
requirements of the degree of
Doctor of Philosophy in Physics
School of Physical and Chemical Sciences
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Abstract

This is a thesis skeleton written with quarto. Make a copy of this thesis repo and start to write!

Make a new paragraph by leaving a blank line.

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B3 partnership!

At the university

Rifat, Alex - vapour sensor design and construction Peter Coard - electronics work Erica Cassie - FET sensing setup Rob Keyzers and Jennie Ramirez-Garcia - NMR spectra Patricia Hunt - Computational chemistry Erica Happe - steaming method Danica- AFM imaging Sushila Pillai - Fluorescence microscope training Jenna and Ali - Device functionalisation

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List of Abbreviations

Ab	Antibody
AB	Amyl Butyrate
AFM	Atomic Force Microscope/Microscopy
Avi-tag	Avidin-tag
BMIM	1-Butyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide
CAD	Computer Aided Design
CNT	Carbon Nanotube
CVD	Chemical Vapour Deposition
DAN	1,5-diaminonaphthalene
DCB	1,2-dichlorobenzene
DI	Deionised
DMT-MM	4-(4,6-dimethoxy-1,3,5-triazin-2-yl)-4 methylmorpholinium chloride
DMMP	Dimethyl Methylphosphonate
DNA	Deoxyribonucleic Acid
EB	Ethyl Butyrate
EDL	Electric Double Layer
FET	Field-Effect Transistor
FITC	Fluorescein isothiocyanate
GA	Glutaraldehyde
GFET	Graphene Field-Effect Transistor
GFP	Green Fluorescent Protein
GPCR	G-protein Coupled Receptor
HEK	Human Embryonic Kidney
His-tag	Histidine-tag
hOR	Human Odorant Receptor
HPLC	High-performance Liquid Chromatography
iOR	Insect Odorant Receptor
IPA	Isopropanol
LOD	Limit of Detection
m-CNT	Metallic Carbon Nanotube
mOR	Mouse Odorant Receptor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor

MSP	Membrane Scaffold Protein
MWCNT	Multi-Walled Carbon Nanotube
NSB	Non-Specific Binding
NTA	Nitrilotriacetic Acid
OBP	Odorant Binding Protein
OR	Odorant Receptor
ORCO	Odorant Receptor Co-Receptor
PBASE	1-Pyrenebutanoic Acid N-hydroxysuccinimide Ester
PBS	Phosphate-Buffered Saline
PDL	Poly- <i>D</i> -lysine
PDMS	Polydimethylsiloxane
PCB	Printed Circuit Board
PEG	Polyethylene Glycol
PLL	Poly- <i>L</i> -lysine
PTFE	Polytetrafluoroethylene (Teflon TM)
RNA	Ribonucleic Acid
s-CNT	Semiconducting Carbon Nanotube
SEM	Scanning Electron Microscope
SMU	Source Measure Unit
SWCNT	Single-Walled Carbon Nanotube
TFTFET	Thin-Film Field-Effect Transistor
TMAH	Tetramethylammonium hydroxide
TX	Transfer Characteristics
UV	Ultraviolet
VUAA1	N-(4-Ethylphenyl)-2-[4-ethyl-5-(pyridin-3-yl)-4H-1,2,4-triazol-3-yl]sulfanylacetamide

1. Introduction

My aim is to develop a ‘bioelectronic nose’, a biosensor device which couples sensitive biological recognition elements with an electronic transducer for the detection of vapour phase compounds [1]–[3]. The transducer converts the interaction or interactions between the recognition element and analyte or analytes of interest into a measurable electronic signal. The sensitive biological component used here are *Drosophila melanogaster* insect odorant receptors (iORs), while the electronic transducer element is a carbon nanotube- or graphene-based field effect transistor (CNTFET or GFET). Carbon-based 2D nanomaterials are promising for use in novel biosensors as they are highly sensitive, biocompatible and cheap to fabricate [4]. I created a purpose-built vapour delivery system apparatus in order to test these devices. Initially, however, iOR-functionalised CNTFETs and GFETs (iOR-FETs) were first tested in the liquid phase to corroborate previous findings within my research group [5], [6].

There has been a significant amount of work done towards creating bioelectronic noses over the last twenty years. This is largely due to their promisingly high level of sensitivity and specificity in real-time in the gas phase, with the ability to signal the presence of volatile organic compound (VOC) traces at lower concentrations than traditional chemical sensors or the human nose in a timescale of seconds [1], [3], [7]. The implications of successful development of a portable and robust bioelectronic nose are significant and varied. Applications could be found in high-importance fields such as biosecurity, medicine, environmental protection and food or water safety [2], [8]–[10]. It has been demonstrated that it is possible to detect invasive brown marmorated stinkbugs based on their volatile trace [11]. A bioelectronic nose could potentially accomplish this task far more cheaply and efficiently than trained sniffer dogs.

As well as a variety of practical applications, development of a bioelectronic nose may give us a greater understanding of the mechanisms underlying insect olfaction, as well as novel understandings of the transducer devices used to register the electronic response to VOCs [1]. The transduction mechanism of nanomaterial-based iOR sensors is still unknown, and I hope to shed further light on the biological and electronic processes underpinning this mechanism [6], [12].

2. Fabrication and Characterisation of Carbon Nanotube Network and Graphene Field-Effect Transistors

2.1. Introduction

This chapter discusses the fabrication processes for both the carbon nanotube network and graphene field-effect transistors (FETs). Experimental optimisation of the transducer element is critical for biosensor work, and large numbers of transducers were required for testing various biosensor functionalisation processes. Therefore, these processes were developed to rapidly fabricate devices with reproducible device characteristics appropriate for biosensing work. Also outlined in this chapter are the characterisation techniques taken to test the quality and reproducibility of these fabrication processes.

The nitrogen ($\geq 99.99\%$) and oxygen (99.7%) used in fabrication work was supplied by BOC Limited New Zealand. All acetone and isopropanol used for wafer/device processing had a minimum 99.9% purity (HPLC grade). Deionised (DI) water was taken from a Synergy[®] UV Water Purification System. The DI water had a measured conductivity of $(1.4 \pm 0.1) \mu\text{S cm}^{-1}$, compared to tap water with a measured conductivity of $(7.8 \pm 0.2) \mu\text{S cm}^{-1}$.

2.2. Photolithography for Carbon Nanotube and Graphene Field-Effect Transistors

2.2.1. General Overview

This section details some of the standard photolithography procedures used in the quarter wafer processing detailed in Section 2.3. Photoresists, also referred to here as ‘resists’, are UV light-sensitive polymeric resins used for photolithography. ‘Positive’ resists are made soluble in alkalines by UV light exposure, meaning exposed areas are removed in the development process. Conversely, ‘negative’ resists are cross-linked by exposure and a post-exposure bake step. The unexposed areas of the negative resist are then removed in the development process [13]. Both positive and negative resists are used in this thesis. The processes for each type of resist are shown in Figure 2.1. The specific photoresist

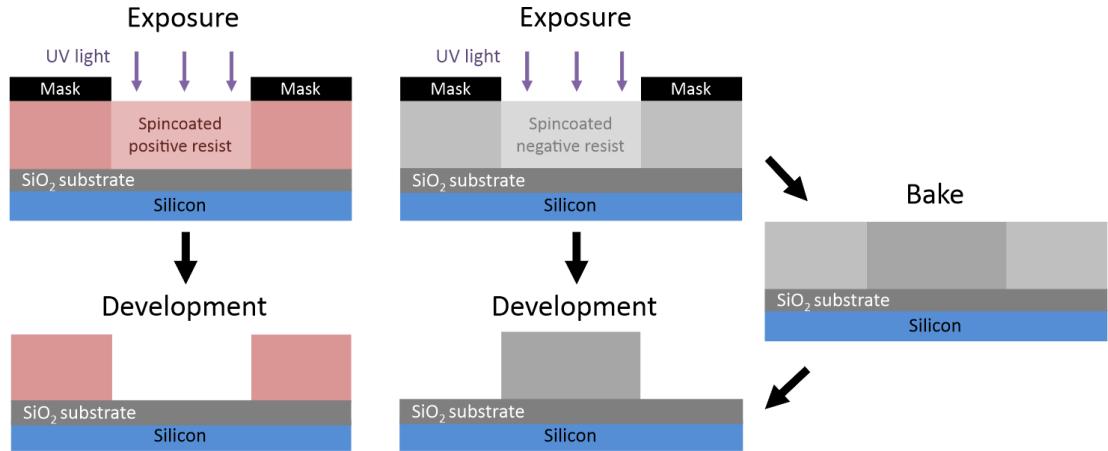


Figure 2.1.: A side-view comparison of generic photolithography processes for positive and negative resists in the ideal case. Photolithography with a positive resist requires a single softbake step before exposure, while for negative resists a second baking step is required after exposure (Thicknesses shown not to scale).

selected for photolithography depends on the specific use case. The types used in this thesis are positive and negative AZ® photoresists (AZ® 1518, Microchemicals GmbH; AZ® nLOF 2020, Microchemicals GmbH) and SU8 (SU8-2150, Kayaku Advanced Materials, formerly Microchem). The AZ® resists used have a minimum film thickness of 1.5 µm [13], while the SU8-2150 has a minimum film thickness of 0.5 µm [14].

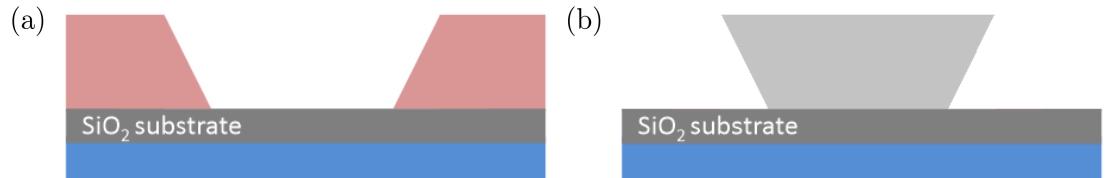


Figure 2.2.: The overcut profile of a positive resist pattern is shown in (a). The undercut profile in (b) is ideal for thin-film metal deposition and subsequent patterned removal, known as “lift-off”. Each profile has had the central region of the substrate exposed to UV light prior to development.

Positive resists which have not been thermally crosslinked will soften at higher temperatures ($\gtrsim 100^\circ\text{C}$ for AZ® 1518), leading to a rounded profile. This is not the case for negative resists, which are more thermally stable [13]. Each resist therefore has a different cross-section profile, as shown in Figure 2.2. If metal deposition is performed on a positive resist, some metal can collect on the outwardly-sloped sidewalls of the resist which forms significant spikes on the edges of the deposited metal upon lift-off. The outwardly-sloped or ‘overcut’ resist profile is illustrated in Figure 2.2 (a). On the other

hand, metal cannot collect on top of the inwardly-sloped negative profile sidewalls, which avoids the formation of large edge spikes. The inwardly-sloped or ‘undercut’ profile is shown in Figure 2.2 (b). Therefore, the negative resist profile is more suited to metal or metal oxide deposition and lift-off processes, though the process is more sensitive to human error due to requiring more processing steps than positive resist [13]. Finally, when it is suitably processed, SU8 is considered to be more stable and biocompatible than other photoresists [15]. It is especially biocompatible when chemically modified via processes such as isopropanol sonication and O₂ plasma treatment [16].

All photolithographic exposure was performed using a Karl Suss MJB3 Contact Aligner with a USHIO super-high pressure 350 W mercury lamp (USH-350DS, Japan). When performing photolithography, the intensity reading from the aligner was 20.8 – 24.2 mW/cm² (Note however that an external photometer reading at 400 nm found an intensity output of 17.2 mW/cm² when the aligner read 21.0 mW/cm²). In general, photolithography procedures should be performed under yellow lighting, as light wavelengths from 320 – 450 nm can promote reactions in the photoresist used and lead to a decline in photolithography quality. Aging of photoresist over time can also significantly affect the photolithography process, and therefore all processes should be re-optimised regularly over time to give the desired result [13]. The range in processing times for some steps of the processes used here are largely due to the effects of aging on the photoresist. The step-by-step processes for each resist are detailed in the subsequent sections.

2.2.2. AZ® 1518 photoresist

1. Spincoat at a final speed of 4000 rotations per minute (rpm) for 1 minute, with an initial acceleration of 500 rpm/s (notes: clean the substrate with acetone, isopropanol (IPA) and nitrogen before spincoating; use only the minimum amount of photoresist required to fully cover the wafer surface; avoid any gaps or bubbles in the photoresist).
2. Softbake 2 – 4 minutes at 95°C on the hotplate (2 min for individual devices, 4 min for a quarter wafer)
3. Mask expose for 10 – 12 s (note: clean mask with acetone/IPA and N₂ dry before use)
4. Develop with 3 parts AZ® 326 (2.38 % TMAH metal-ion free developer, Microchemicals GmbH) in 1 part deionised (DI) water for 30 – 45 s (note: rinse for 10 – 15 s in one development solution, then perform the rest of the development in clean developer for a cleaner profile; lightly agitate the solution throughout the development process)
5. Rinse device for 30 s in DI water to remove excess developer, then dry under nitrogen

2.2.3. AZ® nLOF 2020 photoresist

1. Spincoat at final speed of 3000 rotations per minute (rpm) for 1 minute, with an initial acceleration of 500 rpm/s (notes: clean the substrate with acetone, isopropanol (IPA) and nitrogen before spincoating; avoid any gaps or bubbles in the photoresist)
2. Softbake for precisely 60 s at 110°C on the hotplate
3. Mask expose for 2.7 – 3 s (note: clean mask with acetone/IPA and N₂ dry before use)
4. Post-exposure bake for precisely 60 s at 110°C on the hotplate to cross-link exposed resist
5. Develop with 3 parts AZ® 326 in 1 part DI water for 60 – 70 s (note: rinse for 30 s in one development solution, then perform the rest of the development in clean developer for a cleaner profile; lightly agitate the solution throughout the development process)
6. Rinse device for 30 s in DI water to remove excess developer, then dry under nitrogen

2.2.4. SU8-2150 photoresist

1. SU8 was diluted in cyclopentanone until viscosity was low enough to spincoat on substrate and then sonicated at 50°C for 3 – 4 hours (Note: The dilution ratio used was ~ 1 part SU8 to 5 parts cyclopentanone. However, the age of the SU8 may mean that significant evaporation had occurred prior to use, and the amount of SU8 actually present is underrepresented by this ratio)
2. Spincoat first with a final speed of 500 rpm (acceleration 500 rpm/s) for 10 seconds, followed by spincoating at 4000 rpm (acceleration 7500 rpm/s) for 40 s.
3. Softbake for 10 minutes at 95°C on the hotplate
4. Mask expose for 6 – 8 s (note: clean mask with acetone/IPA and N₂ dry before use)
5. Post-exposure bake for 10 minutes at 95°C on the hotplate to cross-link exposed resist
6. Develop with SU8 developer (Kayaku Advanced Materials, formerly Microchem) for 10 – 15 s, then clean in IPA for 30 s, repeat this step once then dry under nitrogen (note: lightly agitate the solution throughout the development process)

2.3. Fabrication of Carbon Nanotube and Graphene Field-Effect Transistors

2.3.1. Overview

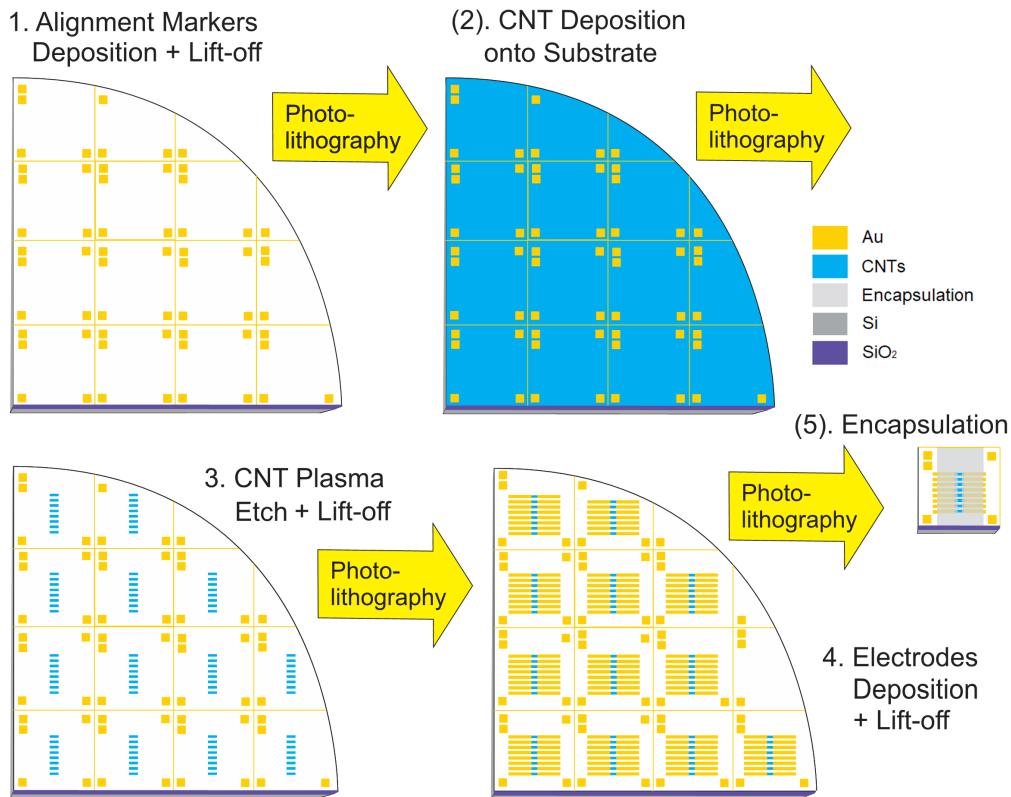


Figure 2.3.: The photolithographic processes used for fabrication of both carbon nanotube and graphene devices (graphene devices were fabricated individually for every step. Step 2 is passed over for graphene devices).

Photolithography was used to define eight channel regions on each device and subsequently to define metal contacts for each of these channels. A schematic demonstrating these photolithography processes on a quarter wafer is shown in Figure 2.3. Masks for photolithography were designed in-house using LayoutEditor CAD software and patterned externally with a UV laser writer. Thermal evaporation was used when depositing chromium (Cr-plated tungsten rods, Kurt J. Lesker) and gold (Au wire, 99.99%, Regal Castings Ltd.), while electron beam evaporation was used when depositing titanium (Ti pieces, 99.99%, Kurt J. Lesker) and metal oxides (*e.g.* Al₂O₃ pieces, 99.99%, Kurt J. Lesker). Metal and metal oxide deposition was performed using an Angstrom Engineering Nexdep 200 Vacuum Deposition System. Deposition thickness was monitored by a Inficon quartz piezoelectric sensor and controlled using an Inficon Deposition Controller.

Electron beam power was provided by a Telemark TT-6 power supply. For metals, the chamber was initially evacuated to a pressure 5×10^{-6} mTorr, while for metal oxides the chamber was initially evacuated to a pressure of 1×10^{-5} mTorr. After evaporation, the chamber was cooled and vented with nitrogen.

Carbon nanotube network field-effect transistors were fabricated using 4-inch *p*-type (B-doped) silicon wafers with either a 100 nm or 300 nm SiO₂ layer (WaferPro LLC) as the substrate. Devices intended for backgated measurements were fabricated with a 100 nm SiO₂ layer. Before photolithographic processing, the wafers were spin-coated with AZ® 1518 photoresist, placed photoresist-side down onto a cleanroom wipe, fixed in place using vacuum suction, then cleaved into quarters using a diamond-tipped scribe tool. For fabrication performed before Jun 2023, the protective photoresist layer was then removed by soaking the quarter-wafers in acetone for 15 minutes, then rinsed with isopropyl alcohol (IPA) and dried with N₂ gas. However, for complete removal of photoresist, it was necessary to flood expose the wafer with the Karl Suss Aligner for 1 min and then place it in AZ® 326 developer for 3 min, as discussed further in [?@sec-photoresist-contamination](#).

Graphene field-effect transistors were fabricated using 300 nm SiO₂/*p*-type Si substrates covered with a monolayer of mechanically transferred CVD graphene (Advanced Chemical Supplier). This substrate was cleaved into equal-sized square chips before photolithography, with side length between 11.6 – 11.7 mm, subject to variability in wafer size. The same cleaving process outlined in Section 2.3.3 was used for cleaving the chips, but the photoresist was not rinsed off after cleaving. Devices were exposed to a brief burst of N₂ gas to remove any dust from the cleaving process from the surface of devices. When not being used in photolithography, graphene-based devices were stored in a vacuum desiccator to prevent the quality of the graphene deteriorating with exposure to air over time. The limited adhesion of graphene to the wafer meant that photolithographic processing had to be performed particularly carefully when fabricating graphene devices.

From Jul 2023 onwards, after each photolithography step using negative resist, quarter wafers/chips were placed in AZ® 326 or SU8 developer (depending on the type of resist) for 3 min to ensure complete removal of photoresist residue. For each step with positive resist, the same procedure was performed but with a flood exposure with UV light for 1 min before being placed in developer. The exception to this rule was for devices with an aluminium oxide layer present. Tetramethylammonium hydroxide (TMAH), the active ingredient of AZ® 326, etches through aluminium oxide and causes electrical shorts through the dielectric layer [17], [18]. A further discussion showing the results of this process is given in [?@sec-photoresist-contamination](#). Figure 2.4 (a) shows a completed quarter-wafer of carbon nanotube field-effect transistors, where partial (unusable) devices at the edges of the wafer have been cleaved off so that only a square of nine devices remains. Figure 2.4 (b) shows cross-section and top view schematics of the completed device with the component parts labelled.

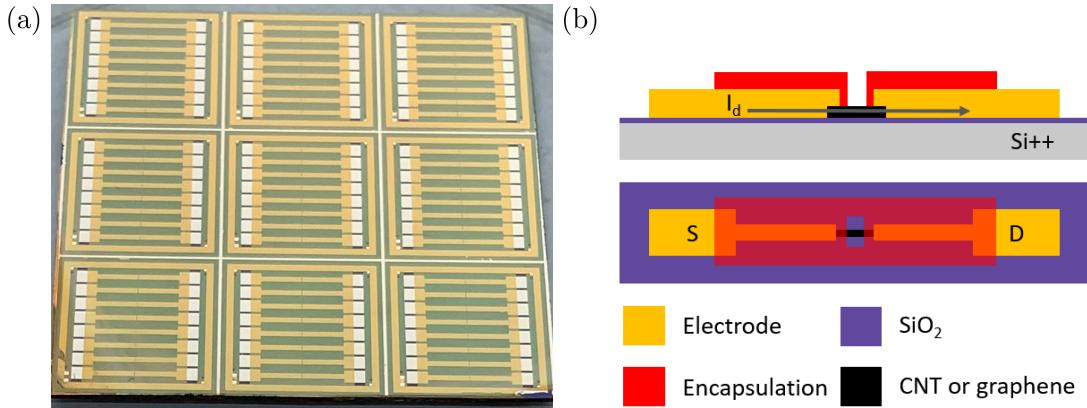


Figure 2.4.: A finished quarter-wafer with the unusable edges cleaved off is shown in (a). Note the double alignment markers feature in the bottom left corner of each device in (a), indicating channel 1 ‘CH1’. The component parts of the field-effect transistor are labelled on device cross-section and channel top view schematics in (b).

2.3.2. Alignment Markers

Metal alignment markers were deposited in order to accurately align the device channels with device electrodes in subsequent photolithography steps. These alignment markers were asymmetric to indicate the orientation of the device for subsequent photolithography steps and electrical characterisation. In later discussion, channel 1 is defined as the channel placed closest to the large double square alignment marker feature. For carbon nanotube quarter wafers, alignment markers were deposited either directly before or after carbon nanotube deposition (see Section 2.3.3 for discussion). For graphene devices, alignment markers were deposited directly after cleaving using the protective photoresist layer spincoated prior to cleaving. AZ® 1518 was used for alignment marker photolithography.

Adhesion layers are required to stick metals such as gold and platinum to silicon dioxide. Chromium and titanium are the most common adhesion metals, but palladium and nickel have also been used successfully[4], [19]. For carbon nanotube devices made before Jun 2022, chromium was used as an adhesive layer for gold, while for all graphene devices and carbon nanotube devices made after Jun 2022, titanium was used as the adhesive layer. Metal layer thickness values quoted here are as stated on the Inficon controller. These values are strictly nominal and must be corroborated, which was done here using a Dektat profiler. For chromium/gold depositions, 10 nm of chromium was deposited followed by a 100 nm Au layer. For titanium/gold depositions, 10 – 20 nm of titanium was deposited followed by a 50 nm Au layer. Devices were then soaked in acetone for at least 2 hours for photoresist lift-off, washed in IPA and dried with nitrogen. The use of titanium gave rise to a cleaner lift-off and improved gold adhesion. Using a relatively

thin gold layer (50 nm nominal instead of 100 nm) also improved lift-off quality. Dektat profiler measurements of combined metal layer thicknesses after lift-off are described in Section 2.3.5.

2.3.3. Deposition of Carbon Nanotubes

Carbon nanotubes were deposited before the alignment markers photolithography step on all wafers fabricated between Aug 2021 – Feb 2023, while devices fabricated before Aug 2021 and after Feb 2023 had the alignment markers photolithography step performed before the deposition of carbon nanotubes. The process order was first switched in Aug 2021 as this order led to faster processing times. However, the order was switched back in Feb 2023 to minimise the exposure of carbon nanotubes to photolithographic chemical processes. The original, solvent-based deposition process for the carbon nanotube network is as follows. 10 mg of 2-mercaptopurine (99%, Sigma-Aldrich) was dissolved in 1 mL ethanol by sonication until clear. Quarter wafers were sonicated in acetone for 3 min, then exposed to O₂ plasma at 100 W for at least 2 min in a small plasma cleaner (Plasma Etch, Inc., PE-50 Compact Benchtop Plasma Cleaning System) or reactive ion etcher (Oxford Instruments, Plasmalab® 80 Plus) under 300 mTorr pressure. The cleaned SiO₂/Si surface was then coated with 2-mercaptopurine for 10 minutes, rinsed with ethanol to remove residual 2-mercaptopurine, and then nitrogen dried.

Meanwhile, 5 µg of 99% semiconducting carbon nanotube bucky paper (NanoIntegris, IsoNanotubes S-99) was dispersed in 10 mL of anhydrous 1,2-dichlorobenzene (DCB, Sigma Aldrich) by ultrasonication until no particles were visible to the naked eye. During this time, the ultrasonic bath temperature was kept between 20-30°C or the buckypaper would not disperse successfully. The substrates were then placed into a dish with CNT-DCB suspension and left covered for 1 hour, dipped into ethanol for 10 min to remove residual solvent and any unattached carbon nanotube bundles, and then dried with nitrogen. Devices fabricated using films deposited in this manner are referred to in this thesis as ‘solvent-deposited’ networks.

Surfactant-Based

Two different approaches were used to attach the surfactant-dispersed carbon nanotubes (CNTs) to the substrate surface. The first approach was a simple drop-casting method, while the second was performed in the presence of steam ('steam-assisted'). In both approaches, the quarter wafers were first rinsed with ultrapure deionised water (DI water), acetone and IPA. Next, they were placed into a small plasma cleaner (Plasma Etch, Inc, PE-50 Compact Benchtop Plasma Cleaning System) or reactive ion etcher (Oxford Instruments, Plasmalab 80 Plus) and exposed to O₂ plasma at 100 W for at least 2 min under 300 mTorr pressure to make the surface hydrophilic. 1 mL of poly-L-lysine (PLL) was immediately deposited onto each quarter wafer and left for 5 minutes. The quarter

wafers were then rinsed for 30 s with DI water and dried with N₂ gas. The presence of the PLL on the plasma cleaned surface strengthens the surface adhesion of semiconducting single carbon nanotubes after the surfactant dispersion has been dropcast onto the substrate.

For carbon nanotube network films deposited in surfactant without steam present, 2 mL of IsoNanotubes-S 90% or 99% dispersion (NanoIntegris) was decanted into a small bottle and sonicated for 5 s to break up bundles of CNTs¹. An even spread of 400 µL carbon nanotube dispersion was placed in the centre of the PLL-functionalised quarter wafer, covered with a glass dish and left for 10 minutes. The dispersion was then rinsed off with DI water and IPA, and the quarter wafer was dried with N₂ gas. Next, the quarter wafer was annealed in a vacuum oven at 150°C for 1 hour to remove residual surfactant. This method would often lead to an inhomogeneous spread of CNTs across the quarter wafer surface, detailed further in section ?@sec-cnt-deposition-effects.

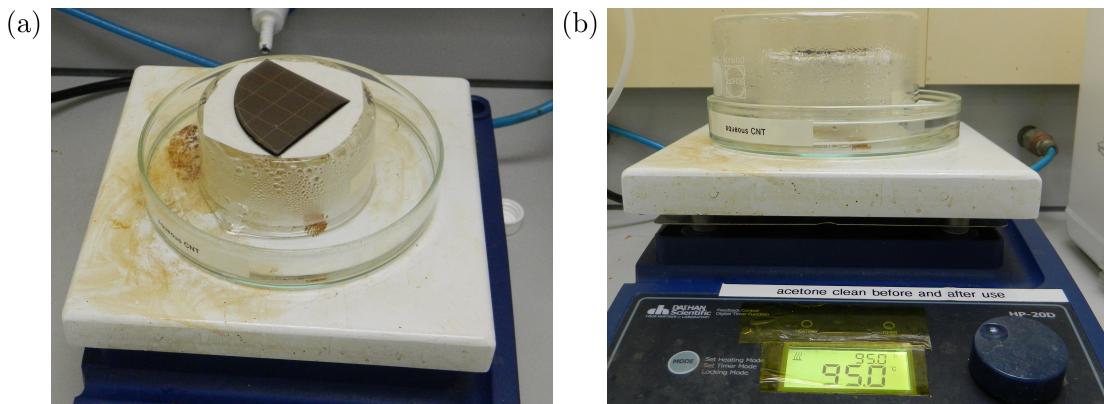


Figure 2.5.: Top view (a) and side view (b) of the steam-assisted method setup, with and without the glass steam cover above the quarter wafer.

For carbon nanotube network films deposited in surfactant in the presence of steam, 2 mL of IsoNanotubes-S 90% or 99% dispersion (NanoIntegris) was decanted into a small bottle and burst-sonicated once to break up bundles of carbon nanotubes. Subsequently, 75 mL of 95°C water was placed into a glass dish on a hotplate held at 95°C. After this, the PLL-functionalised quarter wafer was placed in the centre of an insulating surface on the same hotplate. The carbon nanotube dispersion was carefully spread across the surface of the wafer without spilling any over the wafer edges. The wafer on the insulating surface and glass dish were then left under the same glass dish for 2 minutes to expose the wafer to steam from the glass dish. The use of an insulating surface meant that the wafer and dispersion were not heated from below while exposed to steam. The steam-assisted deposition setup is shown in Figure 2.5, where (a) shows the top and (b) shows the side view of the process.

The carbon nanotube dispersion was then rinsed off the wafer with DI water, ethanol,

¹The composition of the surfactant used in the dispersion is proprietary to NanoIntegris.

acetone and IPA, and then the quarter wafer was dried with N₂ gas. As in the original method, the quarter wafer was then annealed in a vacuum oven at 150°C for 1 hour to remove residual surfactant. This method gave an even spread of CNTs across the quarter wafer surface, leading to a greater consistency in performance between devices. Further details can be found in ?@sec-cnt-deposition-effects. Devices fabricated using films deposited in this manner are sometimes referred to here as “steam-deposited” or “steam-assisted surfactant-deposited” networks (rather than simply “surfactant-deposited”, to avoid confusion with the steam-free method).

2.3.4. Channel Etching

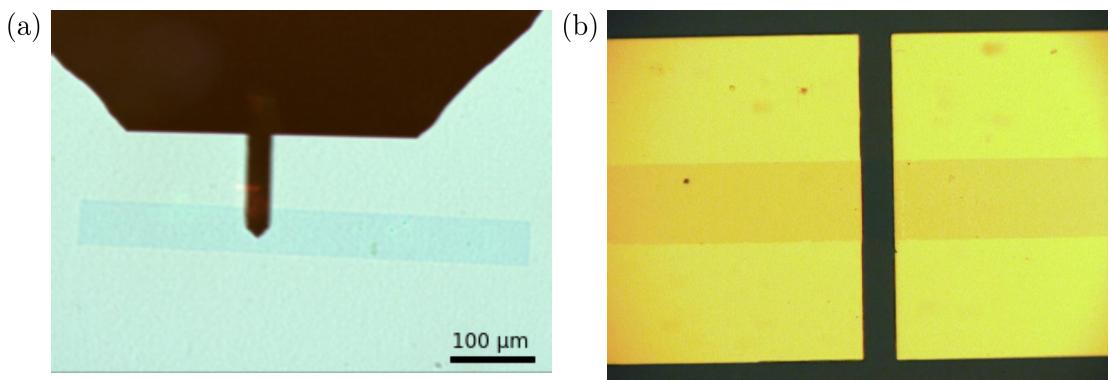


Figure 2.6.: A graphene channel after the plasma etch step is shown in (a), and (b) shows another graphene channel after the metal electrode deposition and liftoff step.

Eight channel features, each 1000 μm in length and 100 μm in width with a pitch of 1200 μm , were patterned using AZ® 1518 photolithography on each carbon nanotube or graphene-covered substrate. Unwanted nanomaterial not covered with photoresist was then etched away with 200 W oxygen plasma at 600 mTorr using a reactive ion etcher or RIE (Plasmalab® 80 Plus, Oxford Instruments). The etch time was 3 minutes for carbon nanotube quarter wafers, and 1 minute for graphene chips. The protective photoresist was then removed by soaking in acetone for at least 5 minutes. The graphene channel feature after etching is shown in Figure 2.6 (a).

2.3.5. Source and Drain Electrodes

The source and drain electrodes for each channel were patterned using photolithography with either AZ® 1518 photoresist (pre-Mar 2023) or AZ® nLOF 2020 photoresist (post-Mar 2023). Before metal deposition, the developed photoresist pattern was exposed to O₂ plasma at 50 W for up to 5 s or at 20 W for 20 – 25 s in a PE-50 plasma cleaner (Plasma Etch, Inc.) to remove residual photoresist on the developed regions and ensure

a clean lift-off. After metal deposition, wafers/devices were soaked in acetone for at least 2 hours for photoresist lift-off, washed in IPA and dried with nitrogen. A graphene channel feature after electrodes deposition is shown in Figure 2.6 (b). As with the alignment markers deposition (see Section 2.3.2), before Jun 2022 chromium was used for the gold adhesion layer, and after Jun 2022 titanium was used. A 20 nm nominal titanium thickness instead of 10 nm nominal thickness was found to give better electrode adhesion, and devices after Feb 2023 were made using this thicker adhesion layer. Good electronic contact could be made with electrodes with a nominal gold layer thickness of 60 – 100 nm, and a Au layer nominally 100 nm thick was most commonly used.

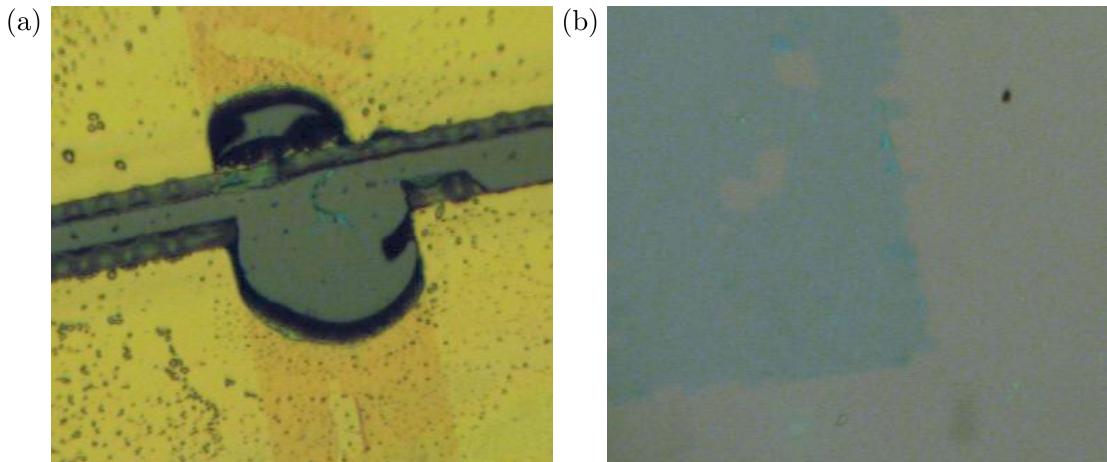


Figure 2.7.: Damage to the gold electrode in the graphene channel region after dimethyl sulfoxide lift-off is shown in (a), while (b) shows damage to a graphene film (blue-green region) after dimethyl sulfoxide lift-off.

Dimethyl sulfoxide (DMSO) was sometimes used in electrodes lift-off instead of acetone between Jul 2021 and Feb 2023 because of its effectiveness as a photoresist stripping agent. However, it was abandoned due to some indications it was unsuitable for the devices being fabricated. Figure 2.7 (a) shows damage by the DMSO to the gold electrodes, and Figure 2.7 (b) shows graphene damaged during the DMSO lift-off. also as detailed in [?@sec-cnt-deposition-effects](#). It is possible that heat from the electrodes deposition sometimes crosslinked residual photoresist on the nanomaterial, and then during lift-off was removed together with any attached nanomaterial by the DMSO. However, it is also possible that prolonged exposure to DMSO alone was sufficient to detach nanomaterial from the substrate. Therefore, acetone was the preferred agent for lift-off despite being a less efficient stripping agent than DMSO.

Example height profiles of quarter wafer channels taken using a Veeco Dektat 150 profiler are shown in Figure 2.8. AZ® 1518 photoresist was used in Figure 2.8 (a) and Figure 2.8 (b) for photolithographic patterning. A 10 nm adhesion layer and 100 nm Au layer were used for each quarter wafers to ensure a consistent comparison. From these figures, a Cr/Au electrode height of 42 ± 1 nm and a Ti/Au electrode height of 48 ± 2 nm were

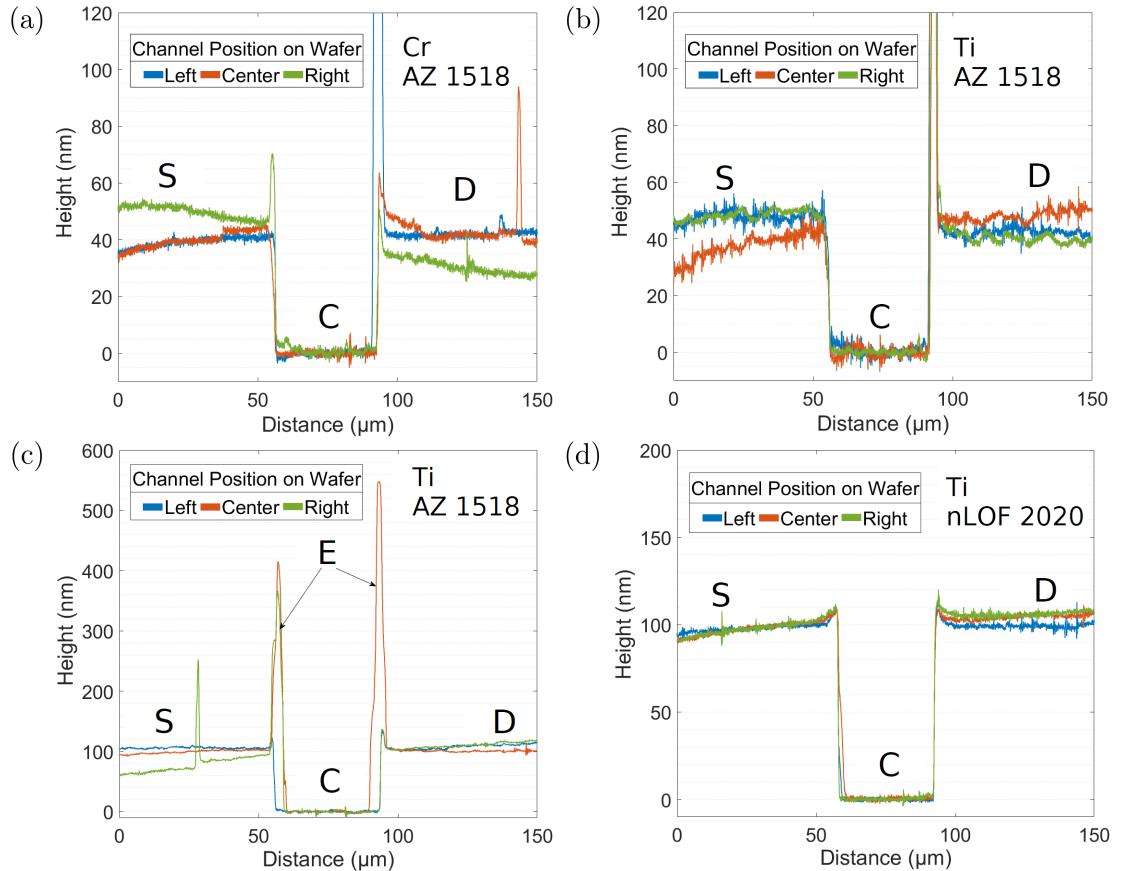


Figure 2.8.: The Dektat height profile measurements for source and drain electrodes taken at different locations on four different quarter wafers are shown here. A 10 nm adhesion layer and 100 nm Au layer were used for the wafers in (a) and (b), with chromium as the adhesion layer for (a) and titanium for (b). A 20 nm titanium adhesion layer and 100 nm Au layer were used for both (c) and (d). AZ® 1518 photolithography was used in (a)-(c), while AZ® nLOF2020 was used in (d). S is source electrode, D is drain electrode and C is the channel region. E indicates the edge spikes or ‘cat ears’ features.

measured, slightly less than half the respective heights stated on the Inficon Deposition Controller. Although using AZ® nLOF 2020 photolithography involves more processing steps, it gave rise to more cleanly-defined electrodes with a more consistent height profile. Often electrode deposition using AZ® 1518 photoresist would lead to sharp vertical spikes along the edge of the electrode, as seen in Figure 2.8 (c). These edge spikes or ‘cat ears’ can partially or fully protrude through thin encapsulation materials such as SU8 and Al₂O₃, leading to significant leakage currents from the electrodes into the FET top gate. This effect is due to the profile of positive resists being suboptimal for lift-off processes, as discussed in Section 2.2.

The height profile corresponding to a wafer with electrodes fabricated using AZ® nLOF 2020 is shown in Figure 2.8 (d). A 20 nm titanium adhesion layer and 100 nm Au layer were used for both Figure 2.8 (c) and Figure 2.8 (d) to ensure a consistent comparison, resulting in a measured electrode height of 103 ± 2 nm for both wafers. A comparison of these figures indicates that AZ® nLOF 2020 photoresist has a more consistent electrode height profile across the wafer surface than the wafer which used AZ® 1518 resist. The measured edge features for the AZ® 1518 resist electrodes vary in size from 20 nm to 450 nm above the bulk electrode surface, whereas the edge features for the AZ® nLOF 2020 resist do not exceed 14 nm in height.

2.3.6. Encapsulation

Several different approaches were used for the encapsulation, or contact protection, of devices. The encapsulation of graphene and carbon-nanotube transistors for biosensing is essential to improve transistor characteristics, passivate the electrodes and ensure only the nanomaterial region is active during biosensing, as discussed in [?@sec-biosensor-methods](#). Before encapsulation photolithography the carbon-nanotube network quarter wafers were cleaved into individual 11 mm × 11 mm chips, using the cleaving process outlined in Section 2.3.3. Cleaving the devices at this step ensured consistent thickness across photoresist encapsulated devices, giving a less variable photolithographic pattern after UV exposure and development.

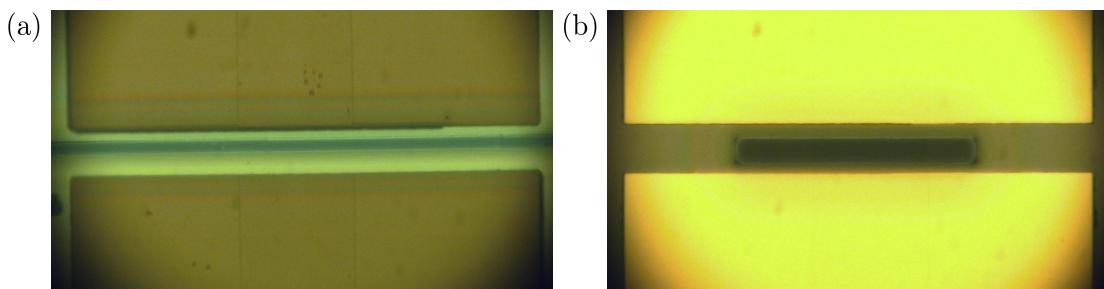


Figure 2.9.: A side-by-side microscope comparison of hardbaked AZ® 1518 processed using the pre-2023 mask, shown in (a), and the 2023 mask, shown in (b).

Two different photolithography masks were used for encapsulation photolithography in this work, with different exposed areas of active nanomaterial. The first mask was used for devices made before Jan 2023, and was designed to leave a region of $500\text{ }\mu\text{m} \times 10\text{ }\mu\text{m}$ unencapsulated for each channel. The second mask was used exclusively after Jan 2023, and was designed to leave a region of $200\text{ }\mu\text{m} \times 20\text{ }\mu\text{m}$ unencapsulated for each channel. This change was made to double the area of carbon nanotubes exposed to electrolyte while halving the area of SiO_2 dielectric exposed to electrolyte during aqueous sensing. Figure 2.9 (a) shows the encapsulation pattern resulting from using the old mask for UV exposure, while the encapsulation pattern resulting from using the new mask is shown in Figure 2.9 (b). The Dektat profiles of three different devices encapsulated using the old mask as used in Figure 2.9 (a) are shown in Figure 2.9 (a) and Figure 2.9 (b) for AZ® 1518 and SU8 resist respectively, while AZ® 1518 and SU8 profiles encapsulated using the new mask as used in Figure 2.9 (b) are shown for in Figure 2.10 (c) and Figure 2.10 (d) respectively. The profiles corresponding to the mask used after Jan 2023 clearly exhibit greater device-to-device consistency, partly due to the mask requiring a greater level of accuracy when aligning the encapsulation pattern with the electrode channel. The larger feature size also means development time has less of an impact on the quality of the encapsulation opening.

Two types of photoresist were initially trialled for encapsulation of carbon nanotube network devices, AZ® 1518 and SU8-2150. Both AZ® 1518 [4], [5], [20] and SU8 have been previously used for device encapsulation, with SU8 noted for being particularly stable and biocompatible [15], [16], [21]. Once developed, the photoresist pattern was exposed to O_2 plasma at 50 W for up to 5 s or at 20 W for 20 – 25 s to remove excess photoresist from the encapsulation opening. Devices were then hardbaked at 200°C for 1 hour to fully crosslink the encapsulation layer. This crosslinking ensured subsequent device exposure to solvent did not remove the photoresist encapsulation.

The exposed region clear of AZ® 1518 resist was $6.8 \pm 0.3\text{ }\mu\text{m}$ in width when using the old, pre-2023 mask, while the exposed region was $16.6 \pm 0.4\text{ }\mu\text{m}$ wide when using AZ® 1518 with the new mask from 2023, as seen in Figure 2.10 (a) and Figure 2.10 (c). However, the exposed region was reduced for the SU8 encapsulation relative to the AZ® 1518, with an width of only $3.6 \pm 0.5\text{ }\mu\text{m}$ for the pre-2023 mask, as seen in Figure 2.10 (b). Photoresist development using SU8 was significantly more time-sensitive than for the AZ® 1518. This meant when the development time was increased to create a wider encapsulation opening, it was difficult to avoid removing large areas of photoresist across the entire surface of the encapsulation. This meant using the new mask from 2023 was especially important for maximising the exposed channel region of SU8 devices. Figure 2.10 (d) shows that the new mask from 2023 with the SU8 resist gave a significantly improved exposed region width of $13.8 \pm 1.0\text{ }\mu\text{m}$.

A relatively thin SU8 encapsulation layer could be deposited when compared to the AZ® 1518 encapsulation profile. Figure 2.10 demonstrates that the AZ® 1518 encapsulation layer had a average height of $1.7 \pm 0.2\text{ }\mu\text{m}$, while the SU8 encapsulation layer had a average height of $680 \pm 20\text{ nm}$. The SU8 also had much less significant edge features than

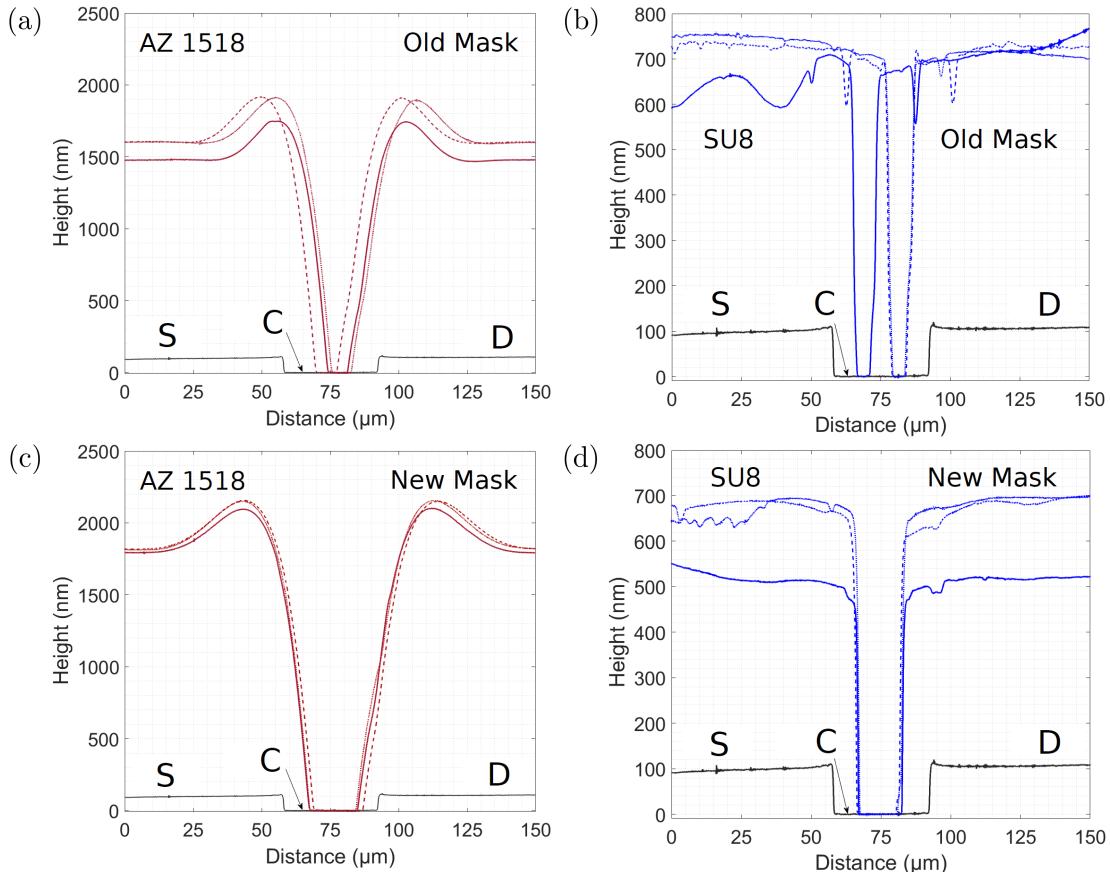


Figure 2.10.: Dektat of carbon nanotube devices after encapsulation photolithography using hardbaked AZ® 1518 and SU8-2150, taken from three different devices. (a) and (b) show photolithography performed with the old, pre-2023 mask, using AZ® 1518 and SU8-2150 respectively. (c) and (d) show photolithography performed with the new mask from 2023 onwards, using AZ® 1518 and SU8-2150 respectively. S is source electrode, D is drain electrode and C is the channel region.

the AZ® 1518, regardless of the profiles of the source and drain electrodes. As noted previously, for both resists the overall profile was more consistent for the new, 2023 mask from device to device than for the old pre-2023 mask. AZ® 1518 encapsulation was used for all graphene devices fabricated.

Dielectric encapsulation

Another approach taken was encapsulation of electrode channels with a dielectric metal oxide/ceramic layer. An electron beam deposition process was used to deposit a 100–150 nm nominal metal oxide layer on devices patterned with the 2023 mask using AZ® nLOF 2020 photoresist. As in Section 2.3.5, the developed photoresist pattern was exposed to O₂ plasma at 50 W for up to 5 s or at 20 W for 20–25 s in a PE-50 plasma cleaner (Plasma Etch, Inc.) before ceramic deposition. Before May 2023, devices were left in TechniStrip® MLO 07 (MicroChemicals) for 5–10 min for lift-off. However, due to concerns over the impact of the constituent chemical DMSO on the nanomaterial region (see Figure 2.7), the lift-off process was altered from May 2023 onwards. After May 2023, devices were soaked in acetone for at least 4 hours and sonicated in clean acetone for 30–60 s to lift-off the photoresist, then washed in IPA and dried with nitrogen.

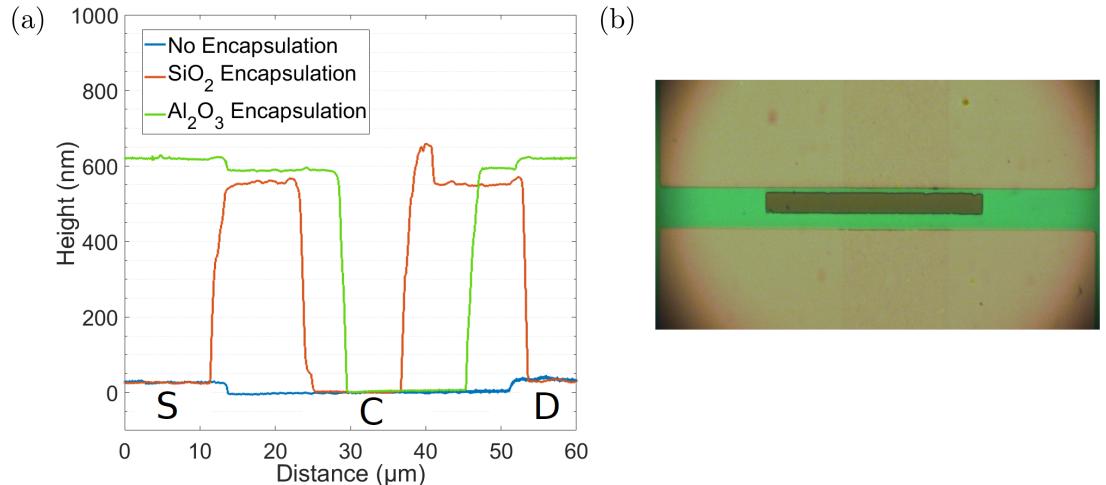


Figure 2.11.: A profile comparison of dielectric materials used for encapsulation is shown in (a), alongside a microscope image of a device encapsulated with aluminium oxide in (b). Note that the layer thicknesses in (a) were from initial tests of the process and are used for illustrative purposes. S is source electrode, D is drain electrode and C is the channel region.

The initial attempt at fabricating a dielectric encapsulation layer used silicon dioxide as the dielectric. However, silicon dioxide adheres poorly to gold without an metallic adhesive layer present, as shown in Figure 2.11 (a). Aluminium oxide was chosen

as an alternative as it sticks well to bulk electrode materials, is heat and chemical resistant, has a relatively high dielectric constant and is bio-compatible [15], [19], [22]. Figure 2.11 (b) shows the aluminium oxide successfully adhered to the electrodes and Figure 2.11 (a) shows the layer had a clean profile after lift-off. Unfortunately, when aluminium oxide layers which were thicker than ~ 100 nm were deposited, a significant drop in channel mobility occurred after encapsulation. This drop was significant enough to make devices unsuitable for sensing. Meanwhile, devices with encapsulation ~ 100 nm thick had significant gate current leakage through the encapsulation layer when liquid-gated. This leakage was present even when AZ® nLOF 2020 was used when patterning electrodes to avoid edge spikes (as discussed in Section 2.3.5). Furthermore, aluminium oxide should not be subsequently exposed to its etchant TMAH, meaning it was difficult to completely remove residual photoresist from device channels after encapsulation. Alternative approaches to high-dielectric ceramic encapsulation are discussed in [?@sec-future-work-fabrication](#).

2.4. Characterisation of Carbon Nanotube and Graphene Field-Effect Transistors

2.4.1. Atomic Force Microscopy

Atomic force microscopy in this thesis was taken using a Nanosurf NaioAFM in dynamic force mode (also known as tapping mode, oscillating mode, acoustic AC mode or intermittent-contact mode). An ACLA probe (AppNano) was used with a tip diameter of 12 nm, height of 14 – 16 μm and a nominal cantilever spring constant of 58 N/m. All atomic force microscopy was performed with the Nanosurf NaioAFM on a stabilising table under a Faraday cage to minimise mechanical and electromagnetic interference. A 256×256 pixel resolution was typically used. Imaging was performed in air at room temperature. Atomic force microscope (AFM) images could not be taken from the small exposed channel region on the encapsulated devices, so were instead taken on a representative carbon nanotube or graphene film sample fabricated on the same wafer as the device being tested. Moisture adversely affected the AFM imaging process. Therefore, films functionalised with biological materials were washed with DI water and gently dried with N_2 before atomic force microscope images were taken. The open source data analysis software Gwyddion (version 2.59) was used to analyse AFM images. This included levelling the background with the polynomial background removal function, removing scarring and zeroing the z-scale.

2.4.2. Fluorescence Microscopy

Fluorescence microscopy was performed using an Olympus BX63 fluorescence microscope controlled using cellSens imaging software. Microscope objectives used were all

Olympus UPLSAPO/UPlanSApo, apochromat objectives which compensate for spherical and chromatic aberrations. Objectives had infinite aperture and a field number of 26.5. Filter cubes used included the Olympus FITC filter (excitation wavelength range: 467 – 498 nm, emission wavelength range: 513 – 556 nm), Texas Red (excitation wavelength range: 542 – 582 nm, emission wavelength range: 604 – 644 nm) and GFP (excitation wavelength range: 604 – 644 nm, emission wavelength range: 502 – 538 nm). The ISO sensitivity was kept at the lowest available setting, ISO200. All microscopy was performed in darkness with the screen turned away from the microscope. To ensure photobleaching did not adversely affect imaging, images were taken soon after initial exposure to fluorescence and taking repeated photos of the same region was avoided. Various useful and thorough introductions to fluorescence microscopy can be found online [23], [24].

2.4.3. Raman Spectroscopy

Raman spectroscopy was performed with a HORIBA Jobin Yvon LabRAM HR800 Raman spectrometer. The wavelength and power used for laser excitation of samples were 514 nm and 1 mW respectively. Spectra were taken with a 1800 line holographic grating with a hole size of 300 μm . A accumulation time of 20 seconds was used when taking spectra. Each spectrum was recorded twice at ten positions within a $40 \mu\text{m} \times 100 \mu\text{m}$ rectangular region on a carbon nanotube film, with a vertical spacing of 10 μm and horizontal spacing of 20 μm between each position. Spectra were collected over two wavenumber ranges at each position, with the first range between 100 cm^{-1} and 650 cm^{-1} , and the second between 1300 cm^{-1} and 1650 cm^{-1} . Data collected at the final, tenth position was often much noisier than all other measurements taken due to an unclear experimental issue, and this data was therefore discarded.

2.4.4. Electrical Characterisation

Both liquid-gated and back-gated measurements were taken of carbon nanotube and graphene devices. All measurement setups used had the same basic configuration, with two source measure units (SMUs) attached to the source and gate. V_{ds} was applied between the source SMU (SMU 1) and the drain SMU (SMU 2), while V_g was applied between the gate SMU (SMU 3) and the drain SMU. The drain SMU was held at 0 V or connected to a ground plane. Drain current I_d was measured at the drain SMU, and gate leakage current I_g was measured at the gate SMU. Voltage from the source and gate SMUs was either kept constant or varied, with only one SMU voltage varied at a time. Three different measurement setups were used for taking these measurements, the Agilent (Keysight/HP) 4156C semiconductor parameter analyser, the Keysight B1500A semiconductor device analyser, and a National Instruments NI-PXIe modular measurement system with a 8 GB PXIe-8821 controller and two NI-4138 source measure units in the system chassis.

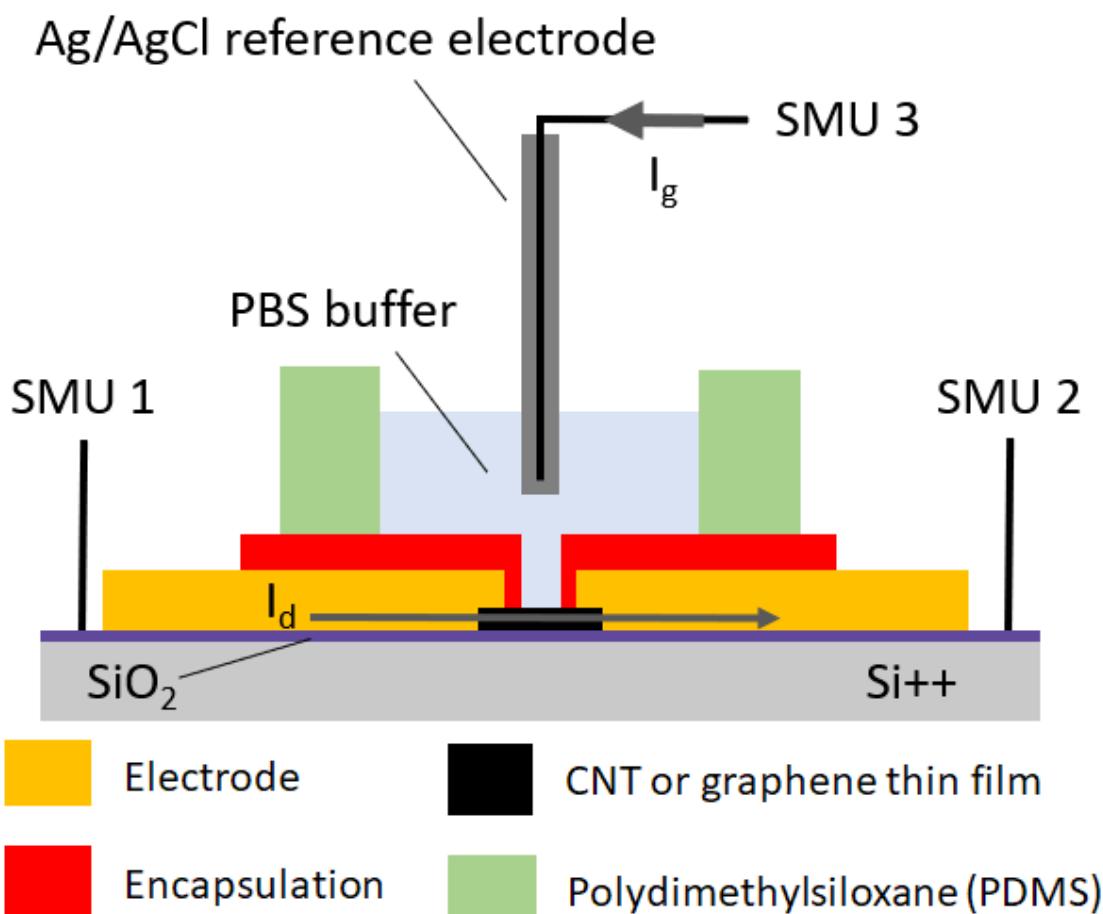


Figure 2.12.: A liquid-gated device schematic showing electrical connections to the three source measure units, SMU 1, SMU 2 and SMU 3.

Liquid-gated measurements were taken using the configuration shown in Figure 2.12. Ag/AgCl standard electrodes were used as the liquid-gate electrode. The electrode was submerged in 80 µL of PBS buffer in a polydimethylsiloxane (PDMS) ‘well’ – a flexible structure used to contain the electrolyte solution – with outer dimensions of 12 mm × 6 mm × 6 mm. This PDMS well was sonicated in isopropanol for 10 min and thoroughly N₂ dried before use. Microscope images of the PDMS surface before and after this cleaning step are shown in Figure 2.13 (a) and Figure 2.13 (b) respectively. The end of Ag/AgCl standard electrode to be submerged was rinsed in DI water and left to sit in DI water for 15 minutes before each characterisation. When using the Agilent 4156C semiconductor parameter analyser or Keysight B1500A semiconductor device analyser for liquid-gated measurements, a Faraday-caged Rucker and Kolls 666 probe station with micromanipulators was used to contact the devices. When using the National Instruments NI-PXIe system for liquid-gated measurements, a custom-made chip carrier with spring-loaded, pointed-tip, gold-coated pogo pins was used.

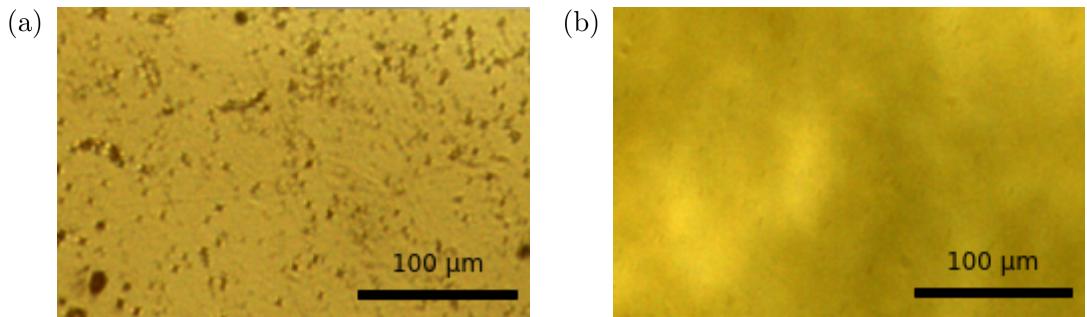


Figure 2.13.: Microscope images of the surface of a PDMS well before (a) and after (b) isopropanol (IPA) sonication for 10 minutes.

Back-gated measurements were taken with a copper plane placed underneath the Si/SiO₂ wafer and connected to SMU 3. The Agilent 4156C Semiconductor Parameter Analyser and Keysight B1500A Semiconductor Device Analyser were used for back-gated measurements of devices within the vapour delivery system device chamber. When the lid of this chamber was tightly sealed, it acted a Faraday cage for another custom-made chip carrier with spring-loaded gold-coated pogo pins, able to contact four channel electrode pairs at once. The silicon back of the device was pressed by the pins against a copper block, connected to the gate SMU. The design of the chamber chip carrier printed circuit board (PCB) is shown in Figure 2.14 (a). The 0.5 mm through holes connect the PTFE-coated wires, which then connect to the output cable, while the 1.75 mm through holes are for attaching the sleeves of gold pogo pins. These pogo pins contact the device within the chamber. 2 × 2.5 mm solder pads have been placed around the 1.75 mm throughholes for better contact with the pogo pin sleeves. The circuit board was placed within two layers of PTFE casing for mounting and protection from vapour within the chamber. The wired interface is shown in Figure 2.14 (b), where the PTFE block is protecting the encased circuit board. The Faraday-cage Rucker and Kolls probe station was used for all back-gated measurements taken outside the vapour sensing chamber.

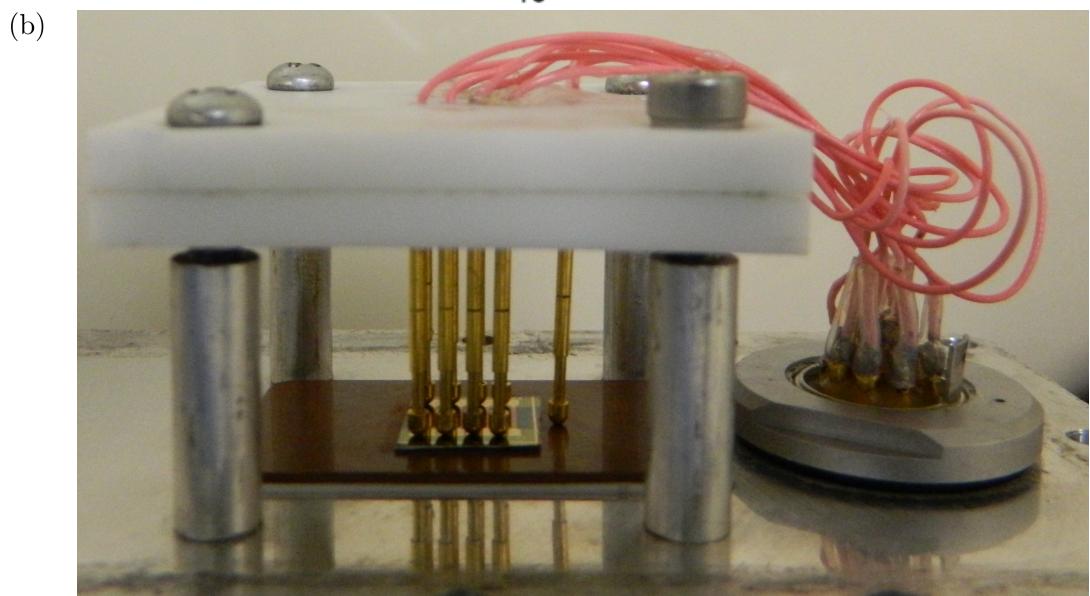
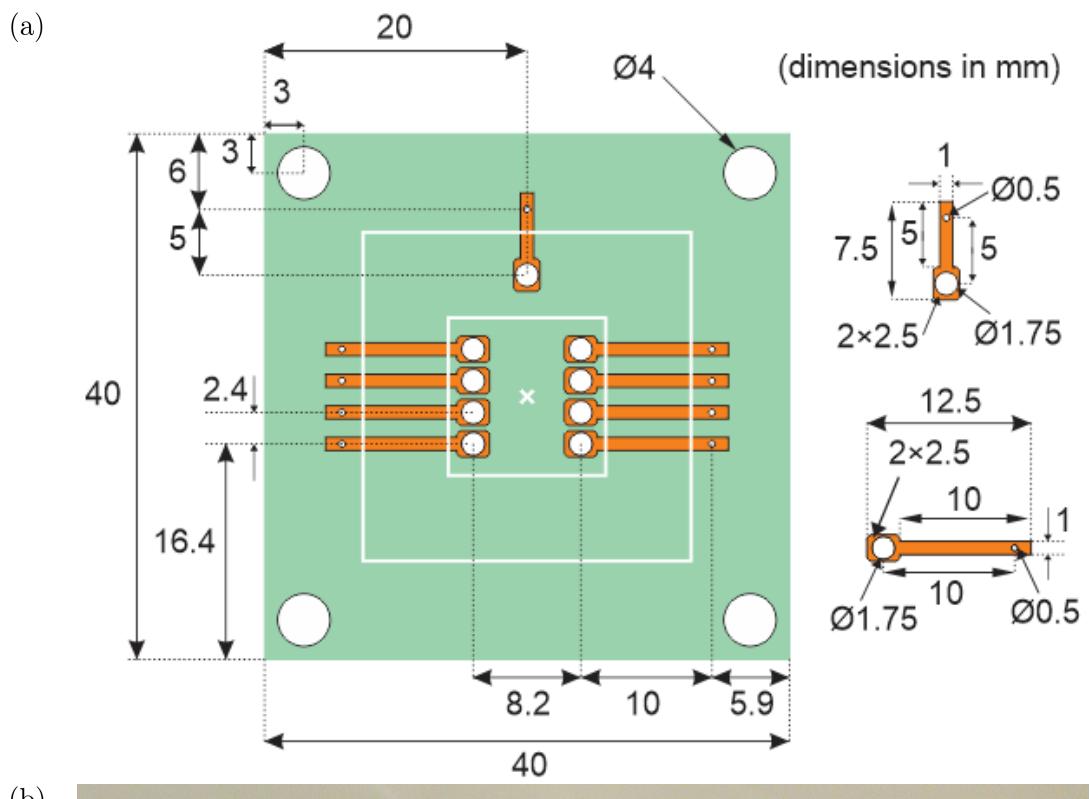


Figure 2.14.: The circuit board schematic for the interface between the sensor device and output signal cable leaving the delivery system chamber is shown in (a). The interface as constructed is shown in (b). This electronic interface was designed and put together by Rifat Ullah, School of Chemical and Physical Sciences, Te Herenga Waka - Victoria University of Wellington.

Custom programs for National Instruments LabView 2017 were used for measurements from the Agilent 4156C Semiconductor Parameter Analyser and the National Instruments NI-PXIe. Keysight EasyEXPERT software was used for characterisation with the Keysight B1500A Semiconductor Device Analyser. Liquid-gated transfer characteristics of carbon nanotube FETs were measured at $V_{ds} = 100$ mV and liquid-gated transfer characteristics of graphene FETs were measured at $V_{ds} = 1$ V, where V_{lg} was swept between -0.5 V and 1 V in both the forward and reverse direction with a step size of either 10 or 20 mV. Backgated transfer characteristics of carbon nanotube FETs were either measured at $V_{ds} = 100$ mV or $V_{ds} = 1$ V, where V_{bg} was swept between -5 V and 5 V or -10 V and 10 V in the forward and reverse directions with a step size of 50 mV or 100 mV.

A liquid-gated setup was used for aqueous-phase sensing and a back-gated setup in the vapour delivery system was used for vapour-phase sensing. Sensing measurements were performed with constant source-drain and gate voltages. The gate voltage used was chosen by locating the subthreshold region of the device transfer characteristics and choosing a voltage that fell within this region, usually $V_g = 0$ V. Using the NI-PXIe with the PXIe-2737 module, eight-channel multiplexed current measurements could be taken in rapid succession. An integration time of 200 or 400 ms was used for sampling with each channel, with the actual sampling rate set by the NI-PXIe. In practice this meant a sampling rate of 1.81 s (for 200 ms integration time) or 3.41 s (for 400 ms integration time) for any given channel. A 200 ms integration time meant the time between samples from successive channels varied between 220ms – 230 ms, while a 400 ms integration time meant the time between samples was consistently 426 ms. The Keysight equipment used a constant 1 s sampling interval.

Aqueous Sensing

Before the sensing process, 200 μ L of PBS was added to the PDMS well and 100-120 μ L of PBS was removed. This initial step was performed to wet the sides of the PDMS well, and check that the attachment of the PDMS well to the device would not unseal when larger volumes of PBS were added during sensing. Before any sensing measurement, a transfer characteristic curve was taken of the liquid-gated device. The initial amount of buffered electrolyte in the well was 100 μ L, unless specified otherwise.

From February 2022 onwards, the standard sensing addition series used comprised of a ‘control series’ and an ‘analyte sensing series’. The control series was performed as part of each sensing experiment to test for unwanted responses to electrolyte and to allow baseline drift to settle. The total control series interval was 1800 s. Electrolyte additions of 20 μ L were made at 100 s, 200 s and 300 s, while electrolyte subtractions of 20 μ L were made at 400 s, 500 s and 600 s. Immediately after the control series, a sensing sequence was performed as part of the same continuous measurement set. An initial electrolyte addition was performed at 2100s, to confirm no changes occurred during the control series that would interfere with sensing. Unless specified otherwise, five analyte

additions were then made with a time spacing of 300 s, at 2400 s, 2700 s, 3000 s, 3300 s and 3600 s. The experimental series was set to finish at 4000 s. The exact timings, analyte concentrations and gate voltage used in a given sensing sequence are discussed alongside the relevant experimental results.

Vapour Sensing

Various vapour exposure procedures were used during sensing measurements. These procedures were performed with the vapour delivery system, and are described in further detail in [?@sec-vapour-sensing-biosensors](#) and [?@sec-pristine-characteristics](#).

2.5. Summary

Several approaches were trialled when depositing a carbon nanotube network for the fabrication of transistor devices, which fall under the general categories of solvent-deposited, surfactant-deposited and surfactant-deposited with steam present. Standard photolithographic methods were used to successfully fabricate carbon nanotube and graphene field effect transistor devices. A range of photolithography types and electrode/encapsulation materials were trialled to find the optimal device composition for sensing. Atomic force microscopy, fluorescence microscopy and a variety of electrical measurement setups were used to characterise the devices. Pristine device characteristics can be found in [?@sec-pristine-characteristics](#), while functionalised device characteristics can be found in [?@sec-noncovalent-functionalisation](#) and [?@sec-biosensing-iORs](#).

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A. Vapour System Hardware

Table A.1.: Major components used in construction of the vapour delivery system described in this thesis.

Description	Part No.	Manufacturer
Mass flow controller, 20 sccm full scale	GE50A-013201SBV020	MKS Instruments
Mass flow controller, 200 sccm full scale	GE50A-013202SBV020	MKS Instruments
Mass flow controller, 500 sccm full scale	FC-2901V	Tylan
Analogue flowmeter, 240 sccm max. flow	116261-30	Dwyer
Micro diaphragm pump	P200-B3C5V-35000	Xavitech
Analogue flow controller, for micro diaphragm pump	X3000450	Xavitech
10 mL Schott bottle	218010802	Duran
PTFE connection cap system	Z742273	Duran
Baseline VOC-TRAQ flow cell, purple	043-950	Ametek Mocon
Baseline VOC-TRAQ flow cell, red	043-951	Ametek Mocon
Humidity and temperature sensor	T9602-5-A	Telaire
Enclosure, for humidity and temperature sensor	MC001189	Multicomp Pro

B. Python Code for Data Analysis

B.1. Code Repository

The code used for general analysis of field-effect transistor devices in this thesis was written with Python 3.8.8. Contributors to the code used include Erica Cassie, Erica Happe, Marissa Dierkes and Leo Browning. The code is located on GitHub and the research group OneDrive, and is available on request.

B.2. Atomic Force Microscope Histogram Analysis

The purpose of this code is to analyse atomic force microscope (AFM) images of carbon nanotube networks in .xyz format taken using an atomic force microscope and processed in Gwyddion (see Section 2.4.1). It was originally designed by Erica Happe in Matlab, and adapted by Marissa Dierkes and myself for use in Python. The code imports the .xyz data and sorts it into bins 0.15 nm in size for processing. To perform skew-normal distribution fits, both *scipy.optimize.curve_fit* and *scipy.stats.skewnorm* modules are used in this code.

B.3. Raman Spectroscopy Analysis

The purpose of this code is to analyse a series of Raman spectra taken at different points on a single film (see Section 2.4.3). Data is imported in a series of tab-delimited text files, with the low wavenumber spectrum ($100\text{ cm}^{-1} - 650\text{ cm}^{-1}$) and high wavenumber spectrum ($1300\text{ cm}^{-1} - 1650\text{ cm}^{-1}$) imported in separate datafiles for each scan location.

B.4. Field-Effect Transistor Analysis

The purpose of this code is to analyse electrical measurements taken of field-effect transistor (FET) devices. Electrical measurements were either taken from the Keysight 4156C Semiconductor Parameter Analyser, National Instruments NI-PXIe or Keysight B1500A Semiconductor Device Analyser as discussed in Section 2.4.4; the code is able to

analyse data in .csv format taken from all three measurement setups. The main Python file in the code base consists of three related but independent modules: the first analyses and plots sensing data from the FET devices, the second analyses and plots transfer characteristics from channels across a device, and the third compares individual channel characteristics before and after a modification or after each of several modifications. The code base also features a separate config file and style sheet which govern the behaviour of the main code. The code base was designed collaboratively by myself and Erica Cassie over GitHub using the Sourcetree Git GUI.

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