

Fabrication of Carbon Nanotube Network and Graphene Field-Effect Transistors

This chapter discusses the fabrication processes for both the carbon nanotube network and graphene transistors. Experimental optimisation of the transducer element is critical for biosensor work, and large numbers of transducers were required for testing various biosensor functionalisation processes. Therefore, these processes were developed to rapidly fabricate devices with reproducible device characteristics appropriate for biosensing work. Also outlined in this chapter are the characterisation techniques taken to test the quality and reproducibility of these fabrication processes.

The nitrogen ($\geq 99.99\%$) and oxygen (99.7%) used in fabrication work was supplied by BOC Limited New Zealand. All acetone and isopropanol used for wafer/device processing had a minimum 99.9% purity (HPLC grade). Deionised (DI) water was taken from a Synergy[®] UV Water Purification System. The DI water had a measured conductivity of $(1.4 \pm 0.1) \mu\text{S cm}^{-1}$, compared to tap water with a measured conductivity of $(7.8 \pm 0.2) \mu\text{S cm}^{-1}$.

Deposition of Carbon Nanotubes

4-inch *p*-type (B-doped) silicon wafers with either a 100 nm or 300 nm SiO₂ layer (WaferPro LLC) were used as the substrate for carbon nanotube network deposition. Devices intended for backgated measurements were fabricated with a 100 nm SiO₂ layer. Before deposition of carbon nanotubes, the wafers were spin-coated with AZ[®] 1518 photoresist, placed photoresist-side down onto a cleanroom wipe, fixed in place using vacuum suction, then cleaved into quarters using a diamond-tipped scribe tool.

For fabrication performed before June 2023, the protective photoresist layer was then removed by soaking the quarter-wafers in acetone for 15 minutes, then rinsed with isopropyl alcohol (IPA) and dried with N₂ gas. However, for complete removal of photoresist, we found it was necessary to flood expose the wafer with the Karl Suss Aligner for 1 min and then place it in AZ326 developer for 3 min, as discussed further in [?@sec-photoresist-contamination](#).

Carbon nanotubes were deposited before alignment markers photolithography on all wafers fabricated between Aug 2021–Feb 2023, while devices fabricated before Aug 2021 and after Feb 2023 had alignment markers photolithography performed before the deposition of carbon nanotubes. The process order was first switched in Aug 2021 as this order led to faster processing times. However, the order was switched back in Feb 2023 to minimise the exposure of carbon nanotubes to photolithographic chemical processes.

Solvent-Based

The solvent-based deposition process for the carbon nanotube network in the second fabrication protocol is as follows. 10 mg of 2-mercaptopurine (99%, Sigma-Aldrich) was dissolved in 1 ml ethanol by sonication until clear. Quarter wafers were sonicated in acetone for 3 min, then exposed to O₂ plasma at 100 W for at least 2 min in a small plasma cleaner (Plasma Etch, Inc., PE-50 Compact Benchtop Plasma Cleaning System) or reactive ion etcher (Oxford Instruments, Plasmalab® 80 Plus) under 300 mTorr pressure. The cleaned SiO₂/Si surface was then coated with 2-mercaptopurine for 10 minutes, rinsed with ethanol to remove residual 2-mercaptopurine, and then nitrogen dried.

Meanwhile, 5 μ g of 99% semiconducting carbon nanotube bucky paper (NanoIntegris, Iso-Nanotubes S-99) was dispersed in 10 mL of anhydrous 1,2-dichlorobenzene (Sigma Aldrich) by ultrasonication until no particles were visible to the naked eye. During this time, the ultrasonic bath temperature was kept between 20 – 30 °C or the buckypaper would not disperse successfully. The substrates were then placed into a dish with CNT-DCB suspension and left covered for 1 hour, dipped into ethanol for 10 min to remove residual solvent and any unattached carbon nanotube bundles, and then dried with nitrogen.

Surfactant-Based

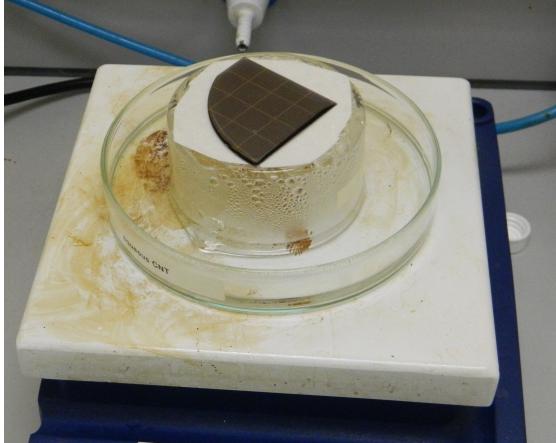
Two different approaches were used to attach the surfactant-dispersed CNTs. The composition of the surfactant used in the dispersion is proprietary to NanoIntegris. In both approaches, the quarter wafers were rinsed with ultrapure deionised water (DI water), acetone and IPA before being placed into a reactive ion etcher (Oxford Instruments, Plasmalab 80 Plus) and exposed to O₂ plasma at 100 W for at least 2 min in a small plasma cleaner (Plasma Etch, Inc, PE-50 Compact Benchtop Plasma Cleaning System) or reactive ion etcher (Oxford Instruments, Plasmalab 80 Plus) under 300 mTorr pressure to make the surface hydrophilic. 1 mL of poly-L-lysine (PLL) was immediately deposited onto each quarter wafer and left for 5 minutes. The quarter wafers were then rinsed for 30 s with DI water and dried with N₂ gas. This process allows for the surface adhesion of semiconducting single carbon nanotubes suspended in surfactant.

* Simple Dropcasting

2 mL of IsoNanotubes-S 90% or 99% solution (NanoIntegris) was decanted into a small bottle and sonicated for 5 s to break up bundles of CNTs. An even spread of 400 μL CNT solution was placed in the centre of the PLL-functionalised quarter wafer, covered and left for 10 minutes. The CNT solution was then rinsed off with DI water and IPA, and then the quarter wafer was dried with N₂ gas. Next, the quarter wafer was annealed in a vacuum oven at 150° C for 1 hour to remove residual surfactant. This method would often lead to an inhomogeneous spread of

CNTs across the quarter wafer surface, detailed further in section ?@sec-cnt-deposition-effects.

* Steam-Assisted Method



(a) Steam method setup without steam cover



(b) Steam method setup with steam cover

Figure 1: Photographs of steam-assisted method setup (top and side view).

2 mL of IsoNanotubes-S 90% or 99% solution (NanoIntegris) was decanted into a small bottle and burst-sonicated once (on then off again) to break up bundles of CNTs. 75 mL of 95° C water was then placed into a glass dish on a hotplate held at 95° C. After this, the PLL-functionalised quarter wafer was placed in the centre of an insulating surface on the same hotplate. The CNT dispersion was carefully spread across the surface of the wafer without spilling any over the wafer edges. The wafer on the insulating surface and glass dish were then left under the same cover for 2 minutes to expose the wafer to steam from the glass dish. The use of an insulating surface meant that the wafer and CNT dispersion were not heated from below while exposed to steam. The steam-assisted deposition setup is shown in Figure 1.

The CNT dispersion was then rinsed off the wafer with DI water, ethanol, acetone and IPA, and then the quarter wafer was dried with N₂ gas. As in the original method, the quarter wafer was then annealed in a vacuum oven at 150° C for 1 hour to remove residual surfactant. This method gave an even spread of CNTs across the quarter wafer surface, leading to a greater consistency in performance between devices. Further details can be found in ?@sec-cnt-deposition-effects.

Photolithography for Carbon Nanotube and Graphene Field-Effect Transistors

Photolithography was used to define eight channel regions on each device and subsequently to define metal contacts for each of these channels. A schematic demonstrating these pho-

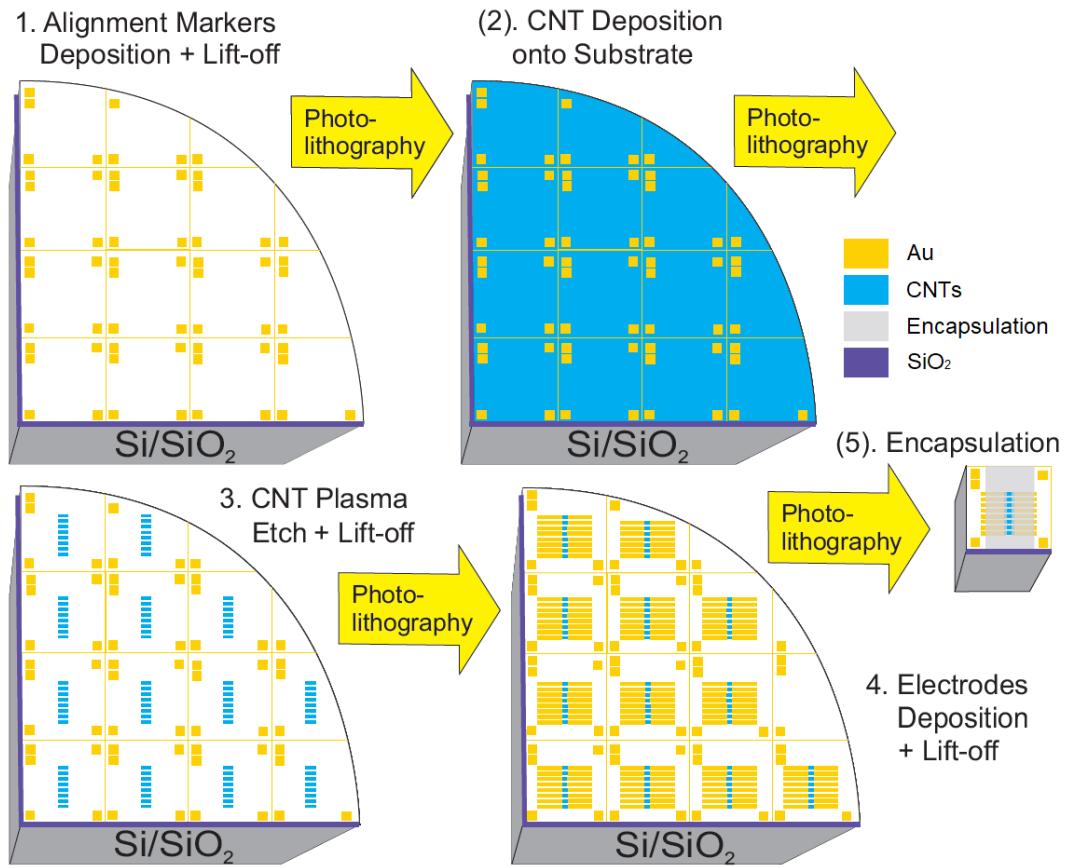


Figure 2: The photolithographic processes used for fabrication of both carbon nanotube and graphene devices (graphene devices were fabricated individually for every step, step #2 skipped for graphene devices)

tolithography processes on a quarter wafer is shown in Figure 2. Masks for photolithography were designed in-house using LayoutEditor CAD software and patterned externally with a UV laser writer.

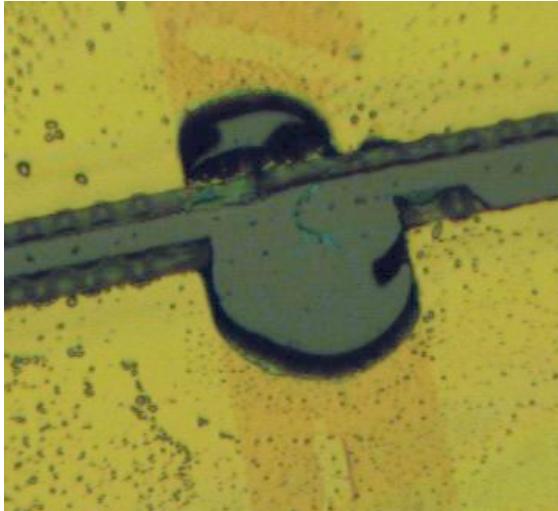
Thermal evaporation was used when depositing chromium (Cr-plated tungsten rods, Kurt J. Lesker) and gold (Au wire, 99.99%, Regal Castings Ltd.), while electron beam evaporation was used when depositing titanium (Ti pieces, 99.99%, Kurt J. Lesker) and metal oxides (*e.g.* Al₂O₃ pieces, 99.99%, Kurt J. Lesker). Metal and metal oxide deposition was performed using an Angstrom Engineering Nexdep 200 Vacuum Deposition System. Deposition thickness was controlled using an Inficon Deposition Controller and electron beam power was provided by a Telemark TT-6 power supply. For metals, the chamber was initially evacuated to a pressure 5×10^{-6} mTorr, while for metal oxides the chamber was initially evacuated to a pressure of 1×10^{-5} mTorr. After evaporation, the chamber was cooled and vented with nitrogen.

Carbon nanotube devices were fabricated using the quarter wafer substrates discussed in Section .

Graphene devices were fabricated using 300 nm SiO₂/p-type Si substrates covered with a monolayer of mechanically transferred CVD graphene (Advanced Chemical Supplier). This substrate was cleaved into equal-sized square chips before photolithography, with side length between 11.6–11.7 mm, subject to variability in wafer size. The same cleaving process outlined in Section was used for cleaving the chips, but the photoresist was not rinsed off after cleaving. Devices were exposed to a brief burst of N₂ gas to remove any dust from the cleaving process from the surface of devices. When not being used in photolithography, devices were stored in a vacuum desiccator to prevent the quality of the graphene deteriorating with exposure to air over time.

Dimethyl sulfoxide (DMSO) was sometimes used in lift-off processes instead of acetone between Jul 2021 and Feb 2023 because of its effectiveness as a photoresist stripping agent. However, it was abandoned due to some indications it was too aggressive for the devices being fabricated, as shown in Figure 3 and also as detailed in [?@sec-cnt-deposition-effects](#). It is possible that heat from the electrodes deposition sometimes crosslinked residual photoresist on the nanomaterial, and then during lift-off was removed aggressively together with any attached nanomaterial by the DMSO. However, it is also possible that prolonged exposure to DMSO alone was sufficient to detach nanomaterial from the substrate. Therefore, acetone was the preferred agent for lift-off despite being a less efficient stripping agent than DMSO.

From Jul 2023 onwards, after each photolithography step using negative resist, quarter wafers/chips placed in AZ326 or SU8 developer for 3 min to ensure complete removal of photoresist residue. For each step with positive resist, the same procedure was performed but with a flood exposure with UV light for 1 min before being placed in developer. The exception to this rule was for devices with an aluminium oxide layer present. Tetramethylammonium hydroxide (TMAH), the active ingredient of AZ® 326, etches through aluminium oxide and causes electrical shorts through the dielectric layer [[@Oh2011](#); [@Ali2021](#)]. A further discussion showing the results of this process is given in [?@sec-photoresist-contamination](#).



(a) Damage to gold electrode in channel region after DMSO lift-off



(b) Damage to graphene (blue region) after DMSO lift-off

Figure 3: Lift-off with dimethyl sulfoxide sometimes led to damage to regions where nanomaterials were present.

Alignment Markers

Metal alignment markers were deposited in order to accurately align the device channels with device electrodes in subsequent photolithography steps. These alignment markers were asymmetric to indicate the orientation of the device for subsequent photolithography steps and electrical characterisation. In later discussion, channel 1 is defined as the channel placed closest to the large, double square alignment marker.

For carbon nanotube quarter wafers, alignment markers were deposited either directly before or after carbon nanotube deposition (see Section for discussion). For graphene devices, alignment markers were deposited directly after cleaving using the protective photoresist layer spincoated prior to cleaving. AZ® 1518 was used for alignment marker photolithography.

For carbon nanotube devices made before Jun 2022, chromium was used as an adhesive layer for gold, while for all graphene devices and carbon nanotube devices made after Jun 2022, titanium was used as the adhesive layer. For chromium/gold depositions, a nominal 10 nm of chromium was deposited followed by a nominal 100 nm Au layer. For titanium/gold depositions, a nominal 10 – 20 nm of titanium was deposited followed by a nominal 50 nm Au layer (for independent measurements of metal layer thickness, see Section). Devices were then soaked in acetone for at least 2 hours for photoresist lift-off, washed in IPA and dried with nitrogen. The use of titanium gave rise to a cleaner lift-off and improved gold adhesion. Using a relatively thin gold layer (50 nm nominal instead of 100 nm) proved to still be clearly visible but to a cleaner lift-off.

Channel Etching

Eight channel features, each 1000 μm in length and 100 μm in width with a pitch of 1200 μm , were patterned using AZ® 1518 photolithography on each carbon nanotube or graphene-covered substrate. Unwanted nanomaterial not covered with photoresist was then etched away with 200 W oxygen plasma at 600 mTorr using a reactive ion etcher or RIE (Plasmalab® 80 Plus, Oxford Instruments). The etch time was 3 minutes for carbon nanotube quarter wafers, and 1 minute for graphene chips. The protective photoresist was then removed by soaking in acetone for at least 5 minutes.

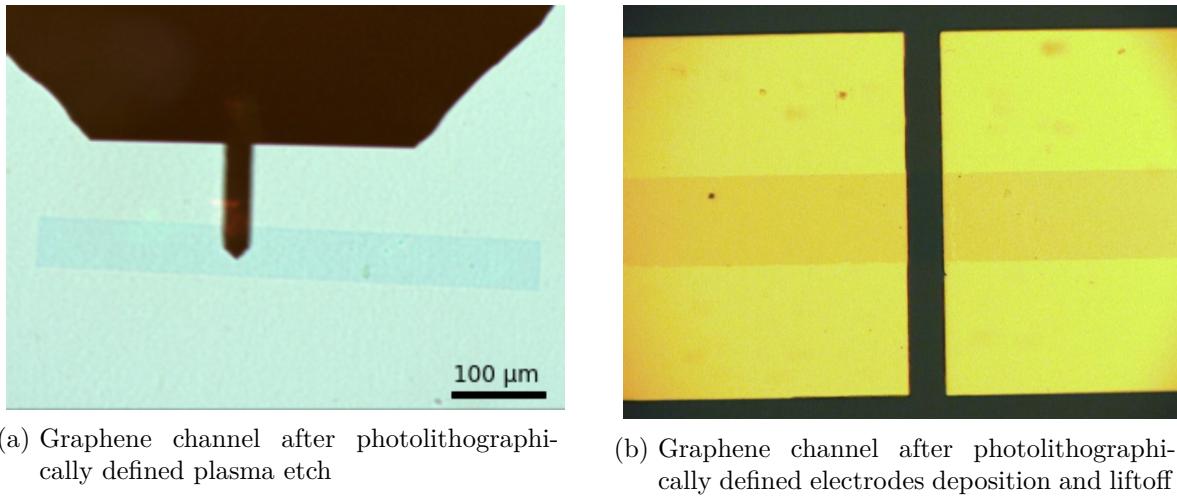
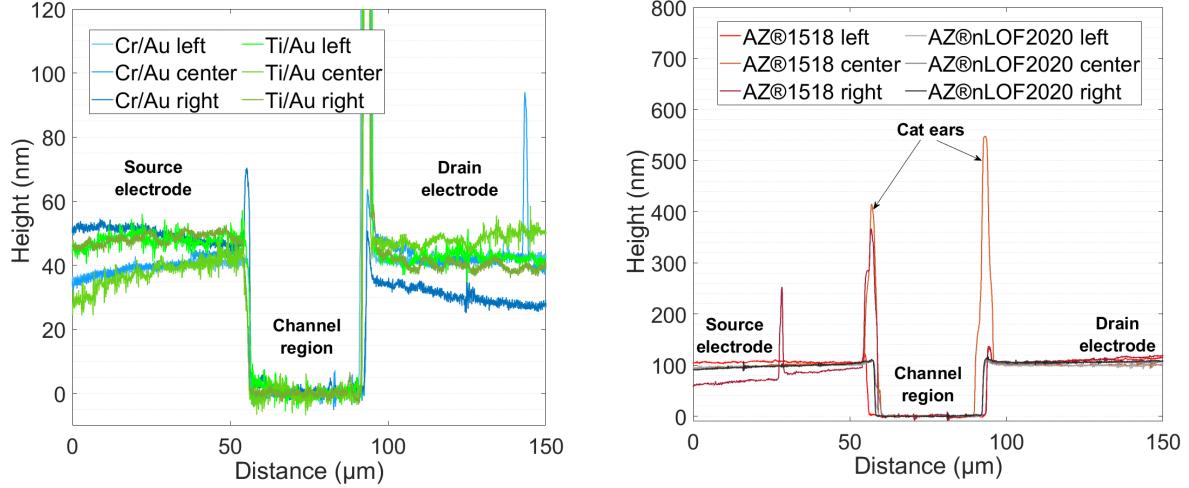


Figure 4: Microscope images of a graphene channel after plasma etch and electrodes photolithography steps.

Electrodes

The source and drain electrodes for each channel were patterned using photolithography with either AZ® 1518 photoresist (pre-Mar 2023) or AZ® nLOF 2020 photoresist (post-Mar 2023). Before metal deposition, the developed photoresist pattern was exposed to O₂ plasma at 50 W for up to 5 s or at 20 W for 20 – 25 s in a PE-50 plasma cleaner (Plasma Etch, Inc.) to remove residual photoresist on the developed regions and ensure a clean lift-off. After metal deposition, wafers/devices were soaked in acetone for at least 2 hours for photoresist lift-off, washed in IPA and dried with nitrogen.

As with the alignment markers deposition (see Section), before Jun 2022 chromium was used for the gold adhesion layer, and after Jun 2022 titanium was used. Adhesion layers are required to stick metals such as gold and platinum to silicon dioxide [Guarnieri2014]. A 20 nm nominal titanium layer instead of 10 nm nominal was found to give better electrode adhesion, and devices after Feb 2023 were made using this thicker adhesion layer. Good electronic contact



(a) Comparison of channel height profile for the different adhesion layers used (AZ® 1518 photolithography used for all profiles)

(b) Comparison of channel height profile for the different photoresist types used (titanium adhesion layer used for all profiles)

Figure 5: Dektat height profiles taken between the source and drain electrodes across a channel from various quarter wafers with electrodes deposited using different approaches. For each quarter wafer, the profiles of three different channels are shown, selected from different locations across the quarter wafer surface.

could be made with electrodes with a nominal gold layer thickness of 60 – 100 nm, and a Au layer nominally 100 nm thick was most commonly used.

Example height profiles of chromium layer channels and a titanium layer channels taken using a Veeco Dektat 150 profiler are shown in Figure 5a. AZ® 1518 photoresist was used here for photolithographic patterning. A 10 nm adhesion layer and 100 nm Au layer were used for both depositions to ensure a consistent comparison. From Figure 5a, we find an measured Cr/Au electrode height of 42 ± 1 nm and an measured Ti/Au electrode height of 48 ± 2 nm, slightly less than half the respective heights stated on the Inficon Deposition Controller.

Although using AZ® nLOF 2020 photolithography involves more processing steps, it gave rise to more cleanly-defined electrodes with a more consistent height profile. Often electrodes deposition using AZ® 1518 photoresist would lead to sharp vertical spikes along the edge of the electrode. These edge spikes or “cat ears” could partially or fully protrude through thin encapsulation materials such as SU8 and Al₂O₃, leading to significant leakage currents from the electrodes into the FET top gate. This effect is due to the profile of positive resists being suboptimal for lift-off processes, as discussed in ?@sec-photolithography.

The height profiles corresponding to a wafer with electrodes fabricated using AZ® 1518 and to a wafer with electrodes fabricated using AZ® nLOF 2020 are shown in Figure 5b. A 20 nm titanium adhesion layer and 100 nm Au layer were used for both depositions to ensure

a consistent comparison, resulting in a measured electrode height of 103 ± 2 nm for both wafers. The wafer which used AZ® nLOF 2020 photoresist clearly has a more consistent electrode height profile across the wafer surface than the wafer which used AZ® 1518 resist. The measured edge features for the AZ® 1518 resist electrodes vary in size from 20 nm to 450 nm above the bulk electrode surface, whereas the edge features for the AZ® nLOF 2020 resist do not exceed 14 nm in height.

Encapsulation

Several different approaches were used for the encapsulation, or contact protection, of devices. The encapsulation of graphene and carbon-nanotube transistors for biosensing is essential to improve transistor characteristics, passivate the electrodes and ensure only the nanomaterial region is active during biosensing, as discussed in [?@sec-biosensor-methods](#).

Before encapsulation photolithography the carbon-nanotube network quarter wafers were cleaved into individual 11 mm \times 11 mm chips, using the cleaving process outlined in Section . Cleaving the devices at this step simplified mask alignment and ensured consistent thickness across photoresist encapsulated devices.

Two different photolithography masks were used for encapsulation photolithography in this work, with different exposed areas of active nanomaterial. The first mask was used for devices made before Jan 2023, and was designed to leave a region of $500 \mu\text{m} \times 10 \mu\text{m}$ unencapsulated for each channel. The second mask was used exclusively after Jan 2023, and was designed to leave a region of $200 \mu\text{m} \times 20 \mu\text{m}$ unencapsulated for each channel. This change was made to double the area of carbon nanotubes exposed to electrolyte while halving the area of SiO₂ dielectric exposed to electrolyte during aqueous sensing.

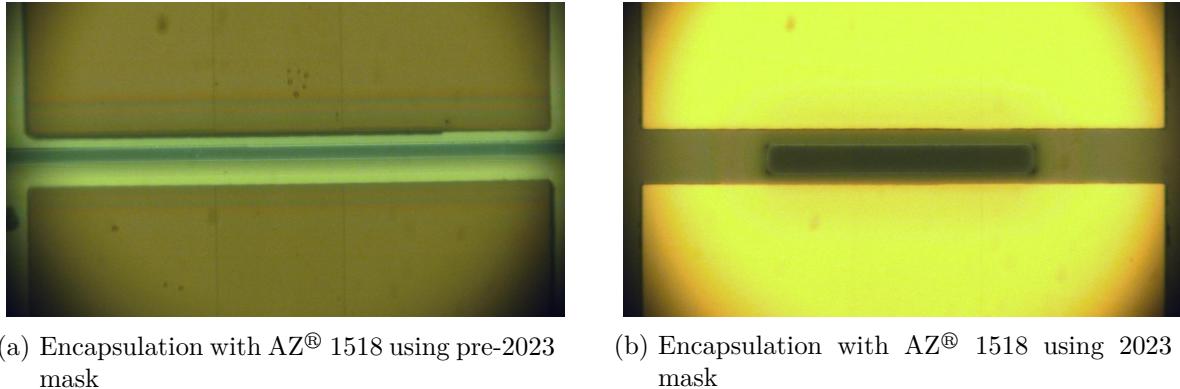


Figure 6: Microscope images of carbon nanotube devices after encapsulation photolithography with hardbaked AZ® 1518.

A side-by-side microscope comparison of hardbaked AZ® 1518 processed with each mask is given in Figure 6, while a Dektat profile comparison corresponding to Figure 6 is shown in

Figure 7a. The profiles corresponding to the mask used after Jan 2023 clearly exhibit greater device-to-device consistency, partly due to the mask requiring a greater level of accuracy when aligning the encapsulation pattern with the electrode channel. The larger feature size also means development time has less of an impact on the quality of the encapsulation opening.

* Photoresist encapsulation

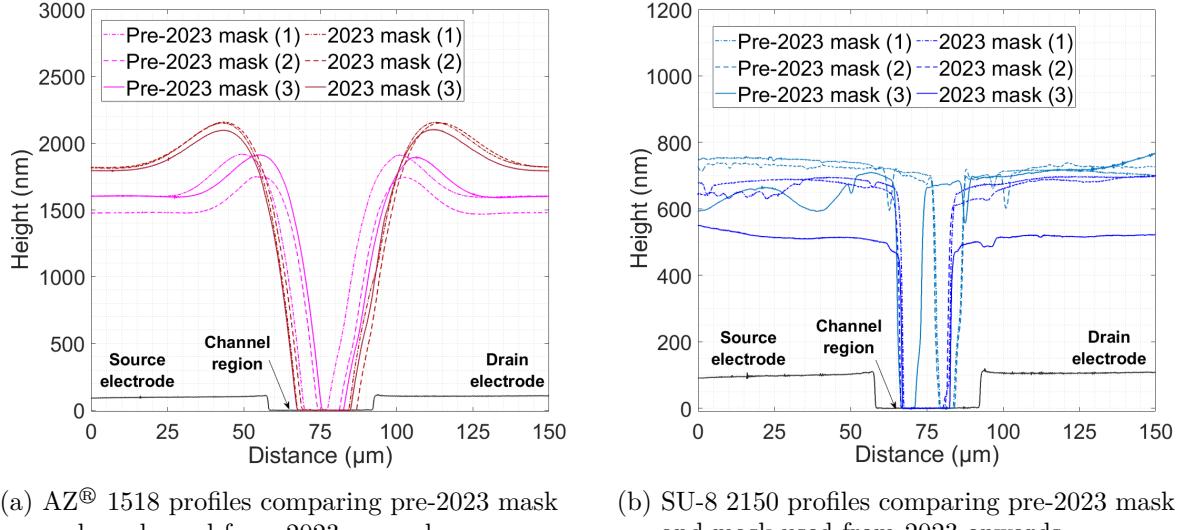


Figure 7: Dektat of carbon nanotube devices after encapsulation photolithography using hard-baked AZ® 1518 and SU-8 2150, taken from various devices.

Two types of photoresist were initially trialled for encapsulation, AZ® 1518 and SU8-2150. Both AZ® 1518 [@Thanihaichelvan2018; @Thanihaichelvan2019; @Shkodra2021] and SU-8 have been previously used for device encapsulation, with SU-8 noted for being particularly stable and biocompatible [@Lee2006; @Chen2021; @Albarghouthi2022]. Once developed, the photoresist pattern was exposed to O₂ plasma at 50 W for up to 5 s or at 20 W for 20 – 25 s to remove excess photoresist from the encapsulation opening. Devices were then hardbaked at 200°C for 1 hour to fully crosslink the encapsulation layer. This crosslinking ensured subsequent device exposure to solvent did not remove the photoresist encapsulation.

The exposed region clear of AZ® 1518 resist was $6.8 \pm 0.3 \mu\text{m}$ in width when using the old, pre-2023 mask, while the exposed region was $16.6 \pm 0.4 \mu\text{m}$ when using AZ® 1518 with the new mask from 2023, as seen in Figure 7a. However, the exposed region was reduced for the SU-8 encapsulation relative to the AZ® 1518, with an width of only $3.6 \pm 0.5 \mu\text{m}$ for the pre-2023 mask, as seen in Figure 7b. Photoresist development using SU-8 was significantly more time-sensitive than for the AZ® 1518. This meant when the development time was increased to create a wider encapsulation opening, it was difficult to avoid removing large areas of photoresist across the surface of the encapsulation. This meant using the new mask

from 2023 was especially important for maximising the exposed channel region of SU-8 devices. Using the new mask from 2023 with the SU-8 resist gave a significantly improved width of $13.8 \pm 1.0 \mu\text{m}$ for the exposed region.

A relatively thin SU-8 encapsulation layer could be deposited when compared to the AZ® 1518 encapsulation profile. The AZ® 1518 encapsulation layer had a average height of $1.7 \pm 0.2 \mu\text{m}$, while the SU-8 encapsulation layer had a average height of $680 \pm 20 \text{ nm}$. The SU-8 also had much less significant edge features than the AZ® 1518, regardless of the profiles of the source and drain electrodes.

As noted previously, for both resists the overall profile was more consistent for the new, 2023 mask from device to device than for the old pre-2023 mask.

* Dielectric encapsulation

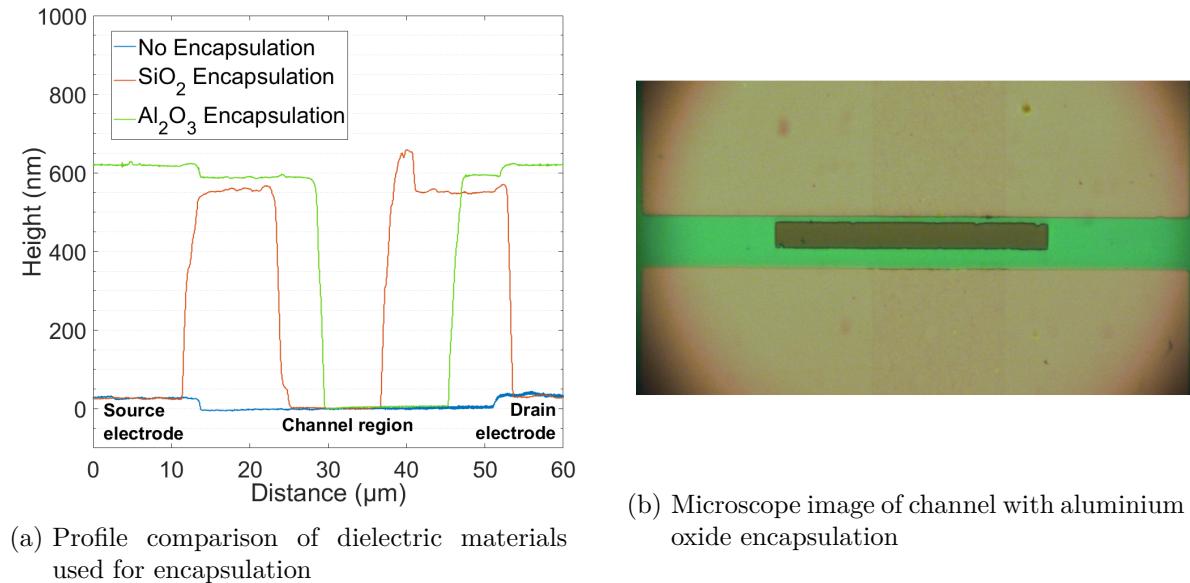


Figure 8: Dektat and microscope image of a device encapsulated with aluminium oxide.

Another approach taken was encapsulation of electrode channels with a dielectric metal oxide/ceramic layer. A electron beam deposition process was used to deposit a $100 - 150 \text{ nm}$ nominal metal oxide layer on devices patterned with the 2023 mask using AZ® nLOF 2020 photoresist. As in Section , the developed photoresist pattern was exposed to O_2 plasma at 50 W for up to 5 s or at 20 W for $20 - 25 \text{ s}$ in a PE-50 plasma cleaner (Plasma Etch, Inc.) before ceramic deposition. Before May 2023, devices were left in TechniStrip® MLO 07 (MicroChemicals) for $5 - 10 \text{ min}$ for lift-off. However, due to concerns over the impact of the constituent chemical DMSO on the nanomaterial region (see Figure 3), the lift-off process was altered from May 2023 onwards. After May 2023, devices were soaked in acetone for at least

4 hours and sonicated in clean acetone for 30 – 60 s to lift-off the photoresist, then washed in IPA and dried with nitrogen.

The initial attempt at fabricating a dielectric encapsulation layer used silicon dioxide as the dielectric. However, silicon dioxide adheres poorly to gold without an metallic adhesive layer present, as shown in Figure 8a. Aluminium oxide was chosen as an alternative as it sticks well to bulk electrode materials, is heat and chemical resistant, has a relatively high dielectric constant and is bio-compatible [Guarnieri2014; Albarghouthi2022; Kolodzey2000]. Figure 8 shows the aluminium oxide successfully adhered to the electrodes and had a clean profile comparable to that of the SU-8 encapsulation layer after lift-off. As noted earlier, aluminium oxide should not be subsequently exposed to its etchant TMAH.

Characterisation via Atomic Force Microscopy

Atomic force microscopy in this thesis was taken using a Nanosurf NaioAFM in dynamic force mode. Atomic force microscope (AFM) images could not be taken from the small exposed channel region on the encapsulated devices, so were instead taken on a representative carbon nanotube or graphene film sample fabricated on the same wafer as the device being tested. Moisture adversely affected the AFM imaging process. Therefore, films functionalised with biological materials were washed with DI water and gently dried with N₂ before atomic force microscope images were taken. The open source data analysis software Gwyddion (version 2.59) was used to analyse AFM images.

Characterisation via Fluorescence Microscopy

Fluorescence microscopy was taken using an Olympus BX63 fluorescence microscope controlled using cellSens imaging software. Microscope objectives used were all Olympus UPLSAPO/UPlanSApo, apochromat objectives which compensate for spherical and chromatic aberrations. Objectives had infinite aperture and a field number of 26.5. Filter cubes used included the Olympus FITC filter (excitation wavelength range: 467 – 498 nm, emission wavelength range: 513 – 556 nm), Texas Red (excitation wavelength range: 542 – 582 nm, emission wavelength range: 604 – 644 nm) and GFP (excitation wavelength range: 604 – 644 nm, emission wavelength range: 502 – 538 nm). The ISO was kept at the lowest available setting, ISO200. All microscopy was performed in darkness with the screen turned away from the microscope. To ensure photobleaching did not adversely affect imaging, images were taken soon after initial exposure to fluorescence and taking repeated photos of the same region was avoided. Various useful and thorough introductions to fluorescence microscopy can be found online [Nikon; Zeiss].

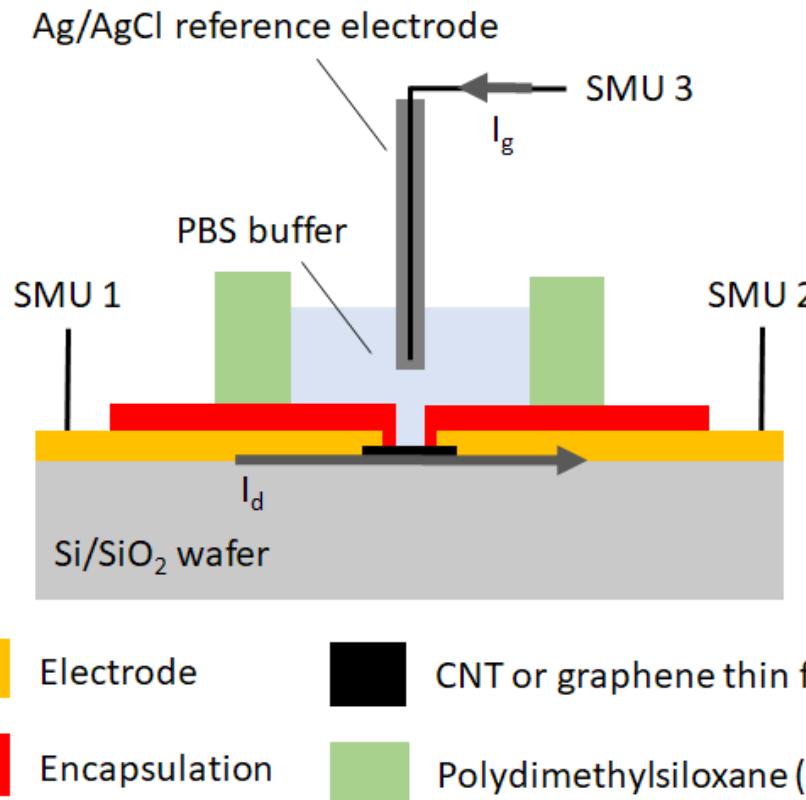
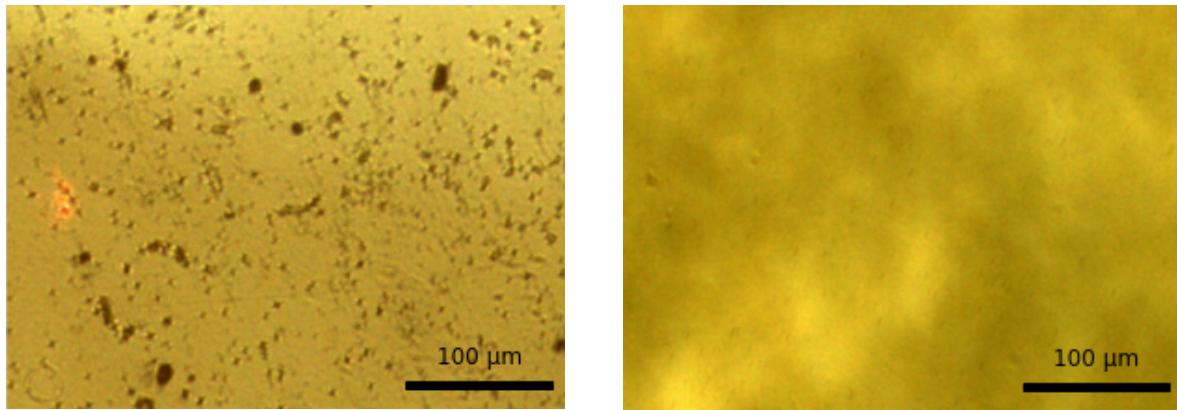


Figure 9: Liquid-gated device schematic showing electrical connections to the three source measure units. V_{ds} is applied between the source SMU (SMU 1) and the drain SMU (SMU 2), while V_{lg} is applied between the gate SMU (SMU 3) and the drain SMU. The drain SMU is held at 0 V or connected to a ground plane. Drain current I_d is measured at the drain SMU, and gate leakage current I_g is measured at the gate SMU.

Electrical Characterisation

Both back-gated and liquid-gated measurements were taken of carbon nanotube and graphene devices. Liquid-gated measurements were taken using the configuration shown in Figure 9. Back-gated measurements were taken with a copper plane placed underneath the Si/SiO₂ wafer and connected to SMU 3 instead of the reference electrode.

All measurement setups used had the same basic configuration, with two source measure units (SMUs) attached to the source and gate. Voltage from the source and gate SMUs was either kept constant or varied, with only one SMU varied at a time. Three different measurement setups were used for taking these measurements, the Keysight (Agilent/HP) 4156C Semiconductor Parameter Analyser, the Keysight B1500A Semiconductor Device Analyser, and a National Instruments NI-PXIe modular measurement system with a 8 GB PXIE-8821 controller and two NI-4138 source measure units. For measurements with the Keysight instruments, a third, drain SMU was attached and kept at a constant 0 V (as shown in Figure 9).



(a) PDMS surface before sonication in IPA for 10 min (b) PDMS surface after sonication in IPA for 10 min

Figure 10: Polydimethylsiloxane (PDMS) surface before and after isopropanol (IPA) sonication for 10 minutes.

When using the Keysight 4156C Semiconductor Parameter Analyser or Keysight B1500A Semiconductor Device Analyser for liquid-gated measurements, a Rucker and Kolls with micromanipulators was used to contact the devices; when using the National Instruments NI-PXIe for liquid-gated measurements, a custom-made chip carrier with spring-loaded, pointed-tip, gold-coated pogo pins was used. Ag/AgCl standard electrodes were used as the liquid-gate electrode. The electrode was submerged in 80 μ L of PBS buffer in a polydimethylsiloxane (PDMS) well with outer dimensions of 12 mm \times 6 mm \times 6 mm. This PDMS well was sonicated in isopropanol for 10 min and thoroughly N₂ dried before use. The microscope images seen in Figure 10 show the PDMS surface before and after this cleaning step. The end of

Ag/AgCl standard electrode to be submerged should be rinsed in DI water and left to sit in DI water for 15 minutes before sensing is performed.

The Keysight 4156C Semiconductor Parameter Analyser and Keysight B1500A Semiconductor Device Analyser were also used for back-gated measurements of devices within the vapour delivery system device chamber. This chamber acted as a Faraday cage for another custom-made chip carrier with spring-loaded gold-coated pogo pins, able to contact four channel electrode pairs at once.

Custom programs for National Instruments LabView 2017 were used for measurements from the Keysight 4156C Semiconductor Parameter Analyser and the National Instruments NI-PXIe. Keysight EasyEXPERT software was used for characterisation with the Keysight B1500A Semiconductor Device Analyser.

Liquid-gated transfer characteristics of carbon nanotube FETs were measured at $V_{ds} = 100$ mV and liquid-gated transfer characteristics of graphene FETs were measured at $V_{ds} = 1$ V, where V_{lg} was swept between -0.5 V and 1 V in both the forward and reverse direction with a step size of either 10 or 20 mV. Backgated transfer characteristics of carbon nanotube FETs were either measured at $V_{ds} = 100$ mV or $V_{ds} = 1$ V, where V_{bg} was swept between -5 V and 5 V in the forward and reverse directions with a step size of 50 mV.

Sensing measurements were performed with constant source-drain and gate voltages. The gate voltage used was chosen by locating the subthreshold region of the device transfer characteristics and choosing a voltage that fell within this region, usually $V_g = 0$ V. The choice of gate voltage for sensing measurements is discussed further in [?@sec-biosensing-transducers](#) and [?@sec-dummy-sensing](#). Using the NI-PXIe with the PXIe-2737 module, eight-channel multiplexed current measurements could be taken in rapid succession. An integration time of 200 or 400 ms was used for sampling with each channel, with the actual sampling rate set by the NI-PXIe. In practice this meant a sampling rate of 1.81 s (for 200 ms integration time) or 3.41 s (for 400 ms integration time) for any given channel. A 200 ms integration time meant the time between samples from successive channels varied between 220ms – 230 ms, while a 400 ms integration time meant the time between samples stayed at 426 ms. The other Keysight equipment used a 1 s sampling interval.

Summary

A variety of approaches were trialled when depositing a carbon nanotube network for the fabrication of transistor devices, and the resultant morphology of these networks are discussed in the next chapter. Standard photolithographic methods were used to successfully fabricate carbon nanotube and graphene field effect transistor devices. A range of photolithography types and electrode/encapsulation materials were trialled to find the optimal device composition for sensing, also discussed in the next chapter. Atomic force microscopy, fluorescence microscopy and a variety of electrical measurement setups were used to characterise the devices.