

**A**  
**PROJECT REPORT**  
**ON**  
**HARDWARE IMPLEMENTATION OF HOPFIELD**  
**NEURAL NETWORKS**

**SUBMITTED**  
**BY**  
**NAVYA SRI ASMATH (1601-14-737-017)**  
**&**  
**NEEHARIKA KOMPALA (1601-14-737-018)**

**UNDER THE GUIDANCE OF**  
**DR.SURESH PABBOJU**  
**PROFESSOR**  
**INFORMATION TECHNOLOGY**



**CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY(A)**  
**DEPARTMENT OF INFORMATION TECHNOLOGY**  
(Affiliated to Osmania University; Accredited by NBA-AICTE and NAAC-UGC,  
ISO 9001:2015 Certified Institution)  
Website: [www.cbit.ac.in](http://www.cbit.ac.in)  
**HYDERABAD-500 075**  
**2017-2018**



**Chaitanya Bharathi Institute of Technology<sup>TM</sup> (Autonomous)**

**(Regd. No. 855/2009)**

(Affiliated to O.U.; All U.G and 5 P.G. Programmes (Civil, CSE, ECE, Mech. & EEE) Accredited by NBA; Accredited by NAAC (UGC); ISO Certified 9001 : 2008)

**Chaitanya Bharathi P.O., CBIT Campus, Gandipet, Kokapet (V),  
Gandipet Mandal, Ranga Reddy District, Hyderabad - 500 075, Telangana**

**e-mail : principal@cbit.ac.in; Website: www.cbit.ac.in ☎ : 040 - 24193276, 277, 280, Fax: 040 - 24193278**

## **CERTIFICATE**

This is to certify that the project work entitled “**HARDWARE IMPLEMENTATION OF HOPFIELD NEURAL NETWORKS**” submitted to **CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY**, in partial fulfillment of the requirements for the award of degree of **B.E (Information Technology)** during the academic year 2017-2018 is a record of original work carried out by **Navya Sri Asmath (160114737017)** and **Neeharika Kompala (160114737018)** during the period of study in the Dept. of IT, CBIT, Hyderabad.

Project Guide  
**Dr.SureshPabboju**  
Professor, IT Dept.  
CBIT, Hyd.

Head of the Department  
**Dr.SureshPabboju**  
Professor , IT Dept.  
CBIT, Hyd.

## ACKNOWLEDGEMENT

We would like to express our gratitude to our guide **Dr.Suresh Pabboju**, Professor, Dept. of IT, C.B.I.T., for his kind co-operation and encouragement which help us in completion of this project.

We are highly indebted to **Dr. P Ravinder Reddy**, The Principal, C.B.I.T., Hyderabad and **Dr. Suresh Pabboju**, Head of Department, Information Technology for their guidance and constant supervision as well as for providing necessary information regarding the project & also for their support in completing the project.

We have taken efforts in this project. However, it would not have been possible without the kind support and help of Teaching Staff, Non-Teaching Staff and organizations. We would like to extend our sincere thanks to all of them.

We would like to express our special gratitude and thanks to industry persons for giving us such attention and time.

Our thanks and appreciations also go to our Parents in developing the project and people who have willingly helped us out with their abilities.

**NavyaSriAsmath**

**(1601-14-737-017)**

**&**

**NeeharikaKompala**

**(1601-14-737-018)**

## **DECLARATION**

We declare that the project work entitled “**HARDWARE IMPLEMENTATION OF HOPFIELD NEURAL NETWORK**” is being submitted by us to the Department of Information Technology, Chaitanya Bharathi Institute of Technology (A), affiliated to Osmania University, Hyderabad.

This is a record of bona-fide work carried out by us under the guidance and supervision of **Dr. Suresh Pabboju**, Professor ,Dept. of IT, CBIT.

No part of the thesis is copied from books/journals/internet and wherever a portion is taken, the same has been duly referred in the text. The report is based on the project work carried out entirely by us and not copied from any other source.

**Navya Sri Asmath**

**(1601-14-737-017)**

**&**

**NeeharikaKompala**

**(1601-14-737-018)**

## **ABSTRACT**

The purpose of this thesis is to study and simulate the behavior of a biological neuron, how nervous impulses, the so-called spikes, are transmitted through the body of the neuron, from the dendrites to the axon. And with this knowledge, to emulate this behavior with the target getting a system, in VHDL, that works exactly in the same way that a biologic neuron. For it, it is important to know how, why and in what circumstances a neuron is fired.

From an electronic point of view dendrites of a neuron are considered as inputs, and the axon as an output. Nervous impulses are interpreted as electrical signals. The artificial neuron will be used in other applications, so that, the codification of the program that emulates the neuron will have be extrapolated to other systems to get a complete neural network.

With the codification in VHDL of the artificial neuron a FPGA can be programmed for future applications of computational neuroscience as well as artificial intelligence

# Table of Contents

1 INTRODUCTION .....	1
1.1 Introduction to Neural Networks .....	1
1.2 Biological Background .....	2
1.3 Hopfield .....	3
1.4 Cognitive Science .....	5
1.5 Existing System .....	8
1.6 Proposed System.....	8
1.7 Applications.....	11
1.8 Report Organization .....	12
2 LITERATURE SURVEY.....	13
2.1 Comparison Between Analog And Digital Implementations Of ANN's .....	13
2.2 FPGA Vs Other Chips .....	13
2.2.1 ASIC's	
2.2.2 ASSP's	
2.2.3 SoC's	
2.2.4 FPGA's	
2.2.5 SoC-class FPGA	
2.3 Overview of VHDL .....	16
2.4 Hardware Implementations Using FPGA's .....	17
2.4.1 Prototyping and Simulation	
2.4.2 Density Enhancement	
2.4.3 Topology Adaption	
3 REQUIREMENTS, ANALYSIS AND SPECIFICATIONS .....	19
3.1 Introduction .....	19
3.2 Requirements .....	20
3.2.1 Device Support	
3.3 Analysis .....	21
3.3.1 System Performance	
3.3.2 Monitor Framework	
3.4 User Interface .....	22
3.4.1 Simulation	

3.4.2 Synthesis	
3.4.3 Editions	
4 DESIGN.....	25
4.1 A Brief Introduction to FPGA's .....	25
4.2 Implementation Issues .....	27
4.2.1 Learning Algorithm	
4.2.2 Signal representation	
4.2.3 Multiplier reduction schemes	
5 IMPLEMENTATION .....	30
5.1 Brief Introduction To ANN .....	30
5.2 Implementation Approaches.....	35
5.2.1 Non-RTR Approach	
5.2.2 RTR Approach	
5.3 Introduction to XOR Problem .....	37
5.4 Implementation Approach .....	38
6 TESTING AND RESULT .....	40
7 CONCLUSION AND FUTURE SCOPE.....	44
BIBILIOGRAPHY	

## List of Figures

Figure No.	Page No.
Figure 1.1 Parts of a Neuron.....	2
Figure 1.2 Indexed Memory .....	4
Figure 4.1 General Architecture of Xilinx FPGAs.....	26
Figure 4.2 Virtex-E Configurable Logic block .....	26
Figure 4.3 Signal Representation.....	28
Figure 5.1 The Perceptron Model.....	30
Figure 5.2 Multilayer Perceptron.....	31
Figure 5.3 The Sigmoid Function.....	33
Figure 5.4 RTR and NON- RTR approach.....	36
Figure 5.5 The exclusive OR.....	38
Figure 5.6 Neuron model for XOR Problem .....	39
Figure 6.1 IP MAC block execution.....	40
Figure 6.2 XOR state function block execution .....	40
Figure 6.3 Activation function execution .....	41
Figure 6.4 Initial Stage output .....	41
Figure 6.5 Training output.....	41
Figure 6.6 Final stage output .....	42



