

MAHL: Multi-Agent LLM-Guided Hierarchical Chiplet Design with Adaptive Debugging

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Abstract—As program workloads (e.g., AI) increase in size and algorithmic complexity, the primary challenge lies in their high dimensionality, encompassing computing cores, array sizes, and memory hierarchies. To overcome these obstacles, innovative approaches are required. Agile chip design has already benefited from machine learning integration at various stages, including logic synthesis, placement, and routing. With Large Language Models (LLMs) recently demonstrating impressive proficiency in Hardware Description Language (HDL) generation, it is promising to extend their abilities to 2.5D integration, an advanced technique that saves area overhead and development costs. However, LLM-driven chiplet design faces challenges such as flatten design, high validation cost and imprecise parameter optimization, which limit its chiplet design capability. To address this, we propose MAHL, a hierarchical LLM-based chiplet design generation framework that features six agents which collaboratively enable AI algorithm-hardware mapping, including hierarchical description generation, retrieval-augmented code generation, diverseflow-based validation, and multi-granularity design space exploration. These components together enhance the efficient generation of chiplet design with optimized Power, Performance and Area (PPA). Experiments show that MAHL not only significantly improves the generation accuracy of simple RTL design, but also increases the generation accuracy of real-world chiplet design, evaluated by Pass@5, from 0 to 0.72 compared to conventional LLMs under the best-case scenario. Compared to state-of-the-art CLARIE (expert-based), MAHL achieves comparable or even superior PPA results under certain optimization objectives.

Index Terms—Chiplet, Hierarchy, AI workloads, Compiler, Design Space Exploration, Multi-agent, LLM

I. INTRODUCTION

The slowing of Moore’s law and increasing demand for AI-specific Integrated Circuits (IC), have driven interest in developing new hardware solutions and computing paradigms that deliver high performance and energy efficiency [1], [2], [3]. 2.5D integration, an advanced packaging technique, has gained popularity due to its scalability and modularity to meet the growing computational demands of AI workloads [4], [5], [6], [7]. Typically, 2.5D IC interconnects multiple chiplets, either homogeneously or heterogeneously, within a single package via an interposer, thereby alleviating limitations for monolithic accelerators in area overhead and development costs.

To realize the 2.5D integration that accommodates different AI applications, the design of reusable and configurable chiplet IPs remains an indispensable and time-consuming venture. The inefficiency of the existing chiplet IP design methodology can

be mainly attributed to two reasons. First, manually designing, modifying, and verifying hierarchical and reusable hardware IPs demands substantial design time and expertise. Furthermore, the large-scale AI applications significantly expand design space, which poses major challenge to both design efficiency and quality in the chosen design. Therefore, to address these limitations, we need an efficient approach to optimize the generation flow of chiplets, not only enabling the rapid, cost-effective development of high-performance hardware designs, but also leveraging efficient DSE to identify the optimal configuration for specific AI applications.

Large Language Models (LLMs) have emerged as a promising solution in various hardware-related tasks. With a Multi-Agent design, LLM accuracy and stability are further enhanced. Prior works have demonstrated their potential in automatically generating HDL code from natural language descriptions or high-level specifications [8], [9], [10], [11]. Some studies [12], [13] have further explored the design space with the assistance of LLMs. Inspired by their potential, we aim to integrate LLMs into the traditional chiplet generation flow. However, through analyzing LLM-generated hardware designs, we observe three critical issues for integration: (1) *Flatten designs*: LLMs tend to generate all code within one single block, which fails to meet the modular requirements of chiplet design; (2) *High validation cost*: LLM-generated HDL code often lacks sufficient accuracy, while manual effort to develop and verify testbenches remains high; (3) *Imprecise parameter optimization*: LLMs still struggle with the precise optimization of configuration parameters [14], making it challenging to directly determine the most efficient configurations.

Based on these observations, we propose MAHL, an LLM-guided chiplet IP generation framework that decomposes chiplet generation tasks into LLM-manageable submodules and further reaps the hierarchical structures for DSE optimization. The contributions of our proposed MAHL can be summarized as follows:

- We propose a Hierarchical Parser and a Hierarchical Module Description Generator for AI-hardware co-design, incorporating two mechanisms. The AI-hardware mapping mechanism enables automated RTL generation by translating high-level AI models into hardware modules, while the hierarchical prompt splitting mechanism enhances module reuse, aligning with the modular and reusable nature of chiplet-based architectures.

- MAHL incorporates a Retrieval-Augmented Code Generator that leverages dynamic module selection to reuse correct and high-quality modules, thereby improving generation efficiency and promoting module reuse. In addition, our framework integrates a Diverseflow Validator that injects controlled noise into the debugging process to enhance output diversity, effectively preventing the validation and correction loop from getting stuck on a single error case.
- For the DSE in MAHL, we design a Multi-Granularity Design Space Explorer that integrates the strengths of both LLMs and analytical techniques. It employs LLMs to perform a coarse-grained, breadth-first exploration over the large design space, followed by analytical DSE for fine-grained, depth-oriented refinement to identify locally optimal configurations. This hybrid approach, together with a reinforcement-driven feedback loop guided by bottleneck analysis, leverages the domain knowledge of LLMs to efficiently navigate and optimize within an expansive design space.

The MAHL framework, leveraging LLM-generated hierarchical prompts, improves average Pass@1 success rates by 44.67% over conventional methods in simple RTL designs, achieving up to a 0.72 Pass@5 increase for complex AI designs. Compared to human-designed chiplets, MAHL-generated designs show an average latency reduction of 16.08% in high-performance mode and an 83.96% area reduction in compact-area mode, highlighting MAHL’s significant potential in chiplet generation.

II. BACKGROUND

A. AI Workload

AI algorithms have experienced an explosive growth over the past decades. The classical Convolutional Neural Networks (CNNs) have played a pivotal role in advancing computer vision, leading to significant model innovations [15], [16]. As research progresses, its focus further expands to Natural Language Processing (NLP), driving the evolution of LLMs with increased diversity and complexity. For instance, GPT [17] leverages data-driven pretraining and multitask learning to address a wide range of NLP tasks, while LLaMA [18], an open-source auto-regressive model, optimizes for performance with limited resources. BERT [19], on the other hand, specializes in bidirectional context understanding. Therefore, in this paper, we select three representative LLM models, BERT [19], GPT [17], and LLaMA [18], as our target algorithms.

B. Chiplet Design Flow

Prior research [20], [21] utilize custom frameworks to propose the chiplet-based design, leveraging its advantages in scalability and modular reuse. For example, the Chopin method utilizes reusable algorithmic chiplets, enabling flexible combination of matrix multiplication and other computational modules based on task requirements, thereby improving hardware resource utilization [20].

Inspired by prior work, we outline a four-phase chiplet design flow: (1) Design Specification, (2) Behavior Modeling, (3) Design Space Exploration and RTL Implementation, and (4)

Physical Layout. **Phase I** defines system-level specs tailored to target algorithms. **Phase II** builds behavioral models for early performance/resource estimation. **Phase III** conducts DSE to identify optimal architectures, followed by final RTL synthesis. Though both Phases II and III involve RTL, the former aids modeling, while the latter finalizes the design. **Phase IV** performs backend tasks like place-and-route and DRC/LVS checks.

To streamline the labor-intensive module design and DSE phases, we propose integrating LLMs to automate modular, configurable, and reusable chiplet generation.

C. LLM-aided Hardware Generation

Traditional hardware design utilizes Electronic Design Automation (EDA) tools to streamline the flow, thereby reducing the need for manual intervention [22], [23], [24]. However, with the evolution of LLMs, researchers have explored more automatic hardware generation and debugging flow [25], leveraging techniques like prompt engineering and fine-tuning [26], [27], [28].

Recent works such as Chip-Chat [29] and RTLCoder [30] demonstrate the potential of LLMs in RTL generation, while VGV [31] enhances Verilog synthesis. However, scaling to complex, hierarchical designs remains challenging.

To address this issue, [12] proposes the GPT4AIGChip framework, which utilizes a demo-augmented pipeline to automate template-based AI accelerator design with LLMs. ROME [32] introduces an automatic hierarchical generation pipeline without human feedback, but it lacks support for AI-chiplet design, prioritizing generation accuracy over key aspects like module reuse and parameterized PPA optimization.

III. FRAMEWORK

A. Overview

Figure 1 depicts a comprehensive overview of the workflow in our MAHL framework. Leveraging natural language user input specifying the AI algorithm, MAHL automatically extracts neural network layer information, searches and designs the best-fit hardware design structure, and finally implements a chiplet IP with optimized configuration and PPA, aiming to achieve the chiplet design tailored for the algorithm while satisfying user-defined objectives. The framework incorporates six agents, each playing a critical role in automating the hardware IP generation and reducing manual design burden in the typical chiplet design workflow:

(1) The **AI-Hardware Hierarchical Parser** decomposes user-defined algorithm into multiple computing and interconnection modules, and selects the most appropriate hardware module implementation descriptions by leveraging LLMs and a Compute & Interconnect library. For components absent from the library, it further incorporates a human-computer interaction (HCI) interface to facilitate real-time completion, enabling a seamless software-to-hardware mapping process;

(2) The **Hierarchical Module Description Generator** primarily retrieves hierarchical descriptions from the Module Description Library. In cases of retrieval failure, it leverages

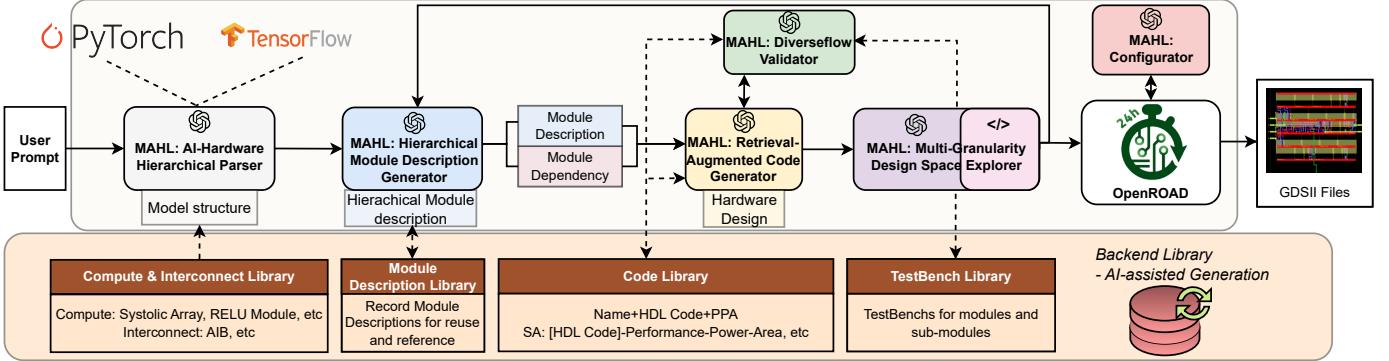


Fig. 1. The overview of the MAHL framework. MAHL framework consists of 6 agents, including an AI-Hardware Hierarchical Parser, a Hierarchical Description Generator, a Retrieval-Augmented Code Generator, an Adaptive Validator, a Multi-granularity Design Space Explorer and a Configurator.

the provided module placeholders to reconstruct the hierarchy from flattened descriptions. The duo-agent mechanism is also applied to ensure format compliance and content refinement of the generated hierarchical description;

(3) The **Retrieval-Augmented Code Generator** splits the hierarchical module description into multiple modules and generates corresponding HDL codes in a hierarchical order. To improve code reuse, a dynamically updated Code Library is maintained for high-quality code retrieval;

(4) The **Diverseflow Validator** integrates conventional simulation and synthesis tools with a multi-round debugging strategy. It generates testbenches using LLMs and retrieves existing ones from the Testbench Library. To enhance output diversity and avoid stagnation on individual failure cases, it introduces controlled noise into prompts, thereby improving validation efficiency;

(5) The **Multi-Granularity Design Space Explorer** receives the submodule PPAs and performs a multi-granularity DSE. It includes both coarse-grained LLM-driven DSE to expand design space and fine-grained analytical DSE for refinement, with the goal of obtaining optimized configurations. After that, the parameters will be fed back to Module Description Generator for full design generation;

(6) The Configurator leverages LLMs to automatically explore and determine the optimized layout-level configuration for physical design generated with OpenROAD [33].

B. Hierarchical Description Generation

As discussed in Section II, **Phase I** of the typical flow focuses on defining the design specification for the target algorithm. Leveraging the modular nature of chiplet-based architecture, this phase is hierarchically realized by two key agents: (1) the **AI-Hardware Hierarchical Parser** and (2) the **Hierarchical Module Description Generator** in Figure 1.

AI-Hardware Hierarchical Parser: As illustrated in the left part of Figure 2, the AI-Hardware Hierarchical Parser starts with a user prompt specifying the target algorithm and corresponding design requirements. This prompt may optionally include user-defined hardware preferences. Otherwise, the agent will automatically infer the most suitable hardware configuration based on the algorithm characteristics.

The parser first decomposes the algorithm into structured computational and interconnection layers sourced from Torchvi-

sion [34] or Huggingface [35] using `print(model)` command, which are then passed to LLMs. Leveraging its natural language understanding and domain knowledge, the LLMs evaluates the functional requirements of each layer and determines the most appropriate hardware modules by referencing a built-in library of computing and interconnection unit name with existing module description. The LLMs then produce a preliminary hardware module description after mapping. For any unmapped or ambiguous components that fails to find the corresponding hardware modules, the agent queries the user through an interactive interface to provide additional specifications. The mapping strategy can be abstracted as:

$$\mathcal{M} = \left\{ (l_i, h_i) \middle| \begin{cases} h_i = \text{LLM}(l_i, \mathcal{H}_{\text{lib}}), & \text{if matches} \\ h_i = h_i^{\text{user}}, & \text{otherwise} \end{cases} \right\}_{l_i \in \mathcal{L}} \quad (1)$$

where l_i denotes the extracted computing or interconnection layers, and \mathcal{H}_{lib} represents the compute and interconnect library. $\text{LLM}(\cdot)$ refers to a mapping function that infers hardware module h_i for each layer l_i through LLMs, and h_i^{user} refers to the user-provided specification. The resulting complete set of hardware modules serves as the foundation for hierarchical module description generation in subsequent stages.

Hierarchical Module Description Generator: For layers that are successfully mapped, the corresponding hardware modules directly retrieve hierarchical descriptions from a Module Description Library, as shown in the right part of Figure 2. For unmapped layer module h_i^{user} , a duo-agent system composed of two LLMs is employed to generate the corresponding hierarchical description. The first LLM, serving as a generator, fills in a module placeholder template with system prompt containing hierarchy hint, which then produces a structured description containing components including *Module*, *Description*, *Sub-modules*, *Port*, *Connections* and *Params*. The second LLM, serving as an evaluator, evaluates the generated hierarchical description for format correctness and semantic completeness. If the description is valid, a “template pass” token is issued and the description is stored in the Module Description Library. Otherwise, revision suggestions are provided for iterative refinement.

It is worth noting that this agent is invoked in both **Phase I** for initial specification and **Phase III** for final design optimization.

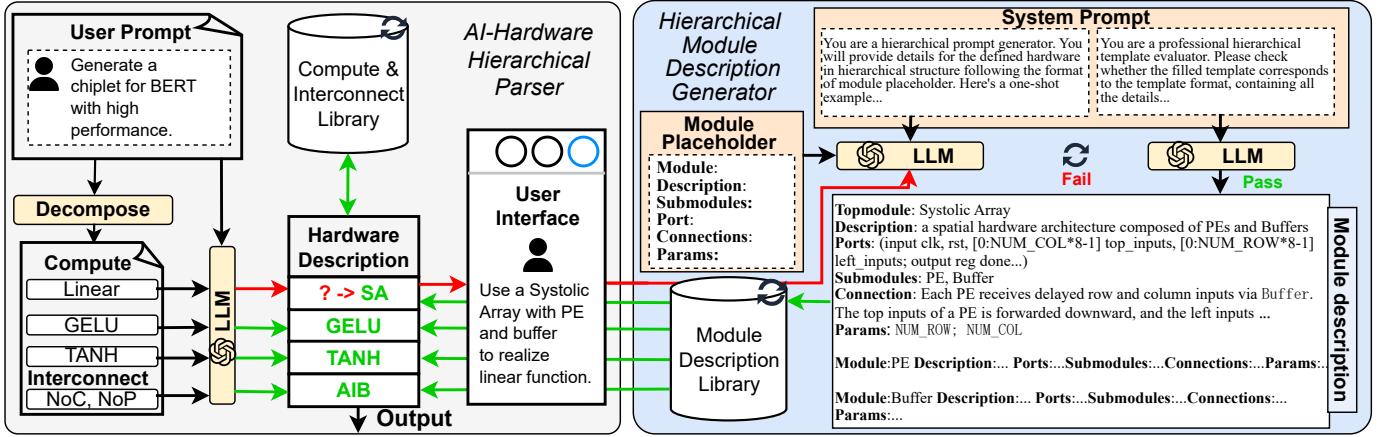


Fig. 2. Hierarchical description generation flow incorporates (1) AI-Hardware Hierarchical Parser and (2) Hierarchical Module Description Generator.

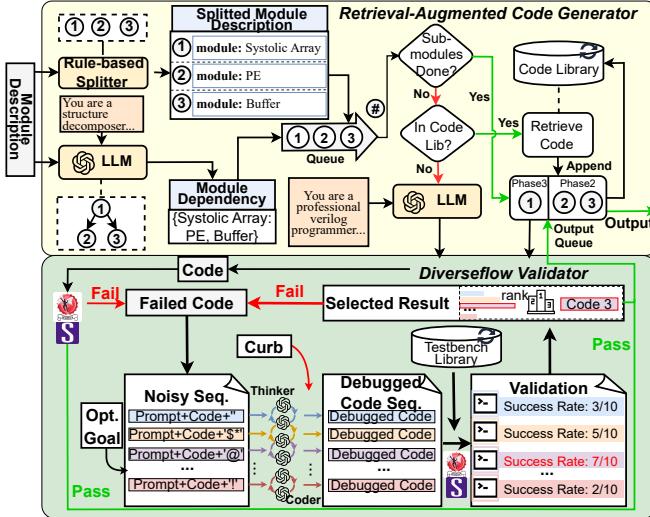


Fig. 3. RTL implementation and validation flow, including (1) Retrieval-Augmented Code Generator and (2) Diverseflow Validator.

In the latter case, the system prompt additionally encodes user-specified PPA targets, and the evaluator assesses whether the generated design can reach these goals through the additional optimization. If not, feedback of other potential techniques, such as clock gating for power or pipelining for performance, is returned to guide further refinement. The hierarchical module descriptions of all layers form a set, which constitutes the input to the subsequent design phase.

C. RTL Implementation and Validation

RTL implementation and validation are involved in both **Phase II** and **Phase III**, each focusing on different objectives, as discussed in Section II. As shown in Figure 1, this process is supported by two agents: (1) the **Retrieval-Augmented Code Generator**, and (2) the **Diverseflow Validator**.

Retrieval-Augmented Code Generator: The upper part of Figure 3 illustrates the workflow of Retrieval-Augmented Code Generator, which operates on inputs of hierarchical module descriptions produced by the preceding agents. For each hierarchical module description, the system performs two key steps: a rule-based structural decomposition that segments the design

into individual modules, and an LLM-assisted dependency analysis to identify inter-module relationships. The resulting individual module descriptions are then ordered bottom-up according to their dependency hierarchy and placed into a queue for sequential processing.

For designs that have not yet undergone **Phase III**, the agent first checks whether all submodules specified in the dependency graph have been generated. A complete set of submodules indicates that the RTL code required for behavioral modeling is available, allowing proceeding to the DSE phase. If some submodule codes are still missing, each module description is processed by first querying the dynamically updated Code Library, a repository of HDL code snippets where each entry includes:

- **Key:** A unique identifier (typically the module's name or function).
- **Weight w :** A numerical score reflecting the overall quality and reliability of the code.
- **PPA:** Power, performance and area of the code.
- **Code:** The corresponding HDL implementation.

For each module, the agent retrieves the most relevant entry by computing the cosine similarity between the query token T (derived from the description) and each stored key T_{db} :

$$S_{\max}(T) = \max_{T_{db} \in DB} (\cos(T, T_{db})). \quad (2)$$

while the decision is performed in a two-step check ensuring both the similarity and quality of the retrieved code:

- 1) **Similarity Check:** If $S_{\max} < t_{sim}$, where t_{sim} is a predefined similarity threshold, the retriever directly proceeds to the red fail path to further code generation, as shown in Figure 3;
- 2) **Weight Check:** If $S_{\max} \geq t_{sim}$, the candidate quality is further examined. Only if $w(T_{db}) \geq t_w$, where t_w is the weight threshold, the code will be retrieved and reused (green success path in Figure 3); otherwise, the retriever opts to the red fail path.

When the retriever opts to the red path for new code generation, it invokes the LLM. For any newly generated code, an initial weight $w_0 = \alpha$ is assigned. After undergoing the

Algorithm 1 Dynamic Weight Management for Code Library

Require: Each code block's initial weight w_n is initialized.
1: N : the number of submodules in simulated code
2: Set scaling factor $\beta > 1$
3: **for** $n = 1$ to N **do**
4: **if** code block n passes simulation test **then**
5: $w_n \leftarrow \beta \cdot w_n$
6: **else**
7: $w_n \leftarrow \frac{1}{\beta} \cdot w_n$
8: **end if**
9: **end for**
10: Remove all code blocks with $w_n < t_h$ (garbage collection)

Diverseflow Validator, the new entry including extracted *Key*, initial weight w_0 , *Power*, *Performance (Clock Frequency)* and *Area (PPA)* values derived from synthesis tools and the validated *Code*, is appended into the Code Library.

For designs that have entered **Phase III** and are undergoing final RTL code generation, the agent will further dynamically adjust the weights of code entries based on final code validation outcomes. Instead of an explicit equation, this dynamic update is performed via a weight management algorithm (detailed in Algorithm 1). In essence, for each code snippet that passes its tests, its weight is multiplied by a factor $\beta > 1$; if it fails, its weight is reduced by multiplying by $1/\beta$. Code entries with weights falling below a threshold t_h are removed from the Code Library through a garbage collection process.

Diverseflow Validator: The lower part of Figure 3 presents the validation workflow for newly generated code. Each code snippet is first verified for functional correctness using a simulator (e.g., ICARUS Verilog) and a Testbench Library containing validated testbenches. To ensure its reliability, the testbenches are generated manually with assistance from LLMs. Since each module's behavior and interfaces are explicitly defined by the hierarchical prompt, testbench generation can be performed in parallel with code generation, with system prompt such as: "You are a testbench generator. Please generate testbench for module description." Upon passing testbench validation through simulation, the code is synthesized using a standard synthesis tool (e.g., Design Compiler) to extract its PPA metrics and appended to the output queue (green path in Figure 3). The verified code and its corresponding PPA are then stored in the Code Library for future reuse.

For failed code, the agent creates a noisy prompt sequence containing K parallel threads. A subset of symbolically represented tokens (comprising $P\%$ of the total code length) is selected as noise. The introduction of noise during generation aims to reduce the likelihood of producing similar outputs repeatedly, thereby increasing the chances of generating correct code. Symbolic tokens are specifically chosen as noise to avoid the accidental formation of meaningful words, which could undesirably bias the model's generation. Each of the K threads is processed by a duo-agent system, consisting of:

- **Thinker:** Evaluates the buggy code, diagnosing issues and suggesting specific fixes.
- **Coder:** Applies the suggested modifications without access to the original prompt, ensuring unbiased corrections.

Algorithm 2 Code Selection Strategy

```
1: Input: debugged_list: list of debugged code sequences
2: Input: target_result: user-defined optimization metric (e.g.,
   1/clk_freq, power, or area)
3: Initialize: pass_list  $\leftarrow [ ]$ , fail_list  $\leftarrow [ ]$ 
4: for  $i$  in debugged_list do
5:   if codes[ $i$ ] passes simulation then
6:     Append ( $i$ , target_result(codes[ $i$ ])) to pass_list
7:   else
8:     Append ( $i$ , num_failed_cases(codes[ $i$ ])) to fail_list
9:   end if
10: end for
11: if pass_list is not empty then
12:   index  $\leftarrow$  index in pass_list with minimum target result
13: else
14:   index  $\leftarrow$  index in fail_list with minimum failed cases
15: end if
16: return codes[index]
```

The newly generated debugged code from all K threads is then re-executed for simulation and synthesis. The agent sorts and ranks these variants to identify the best-performing code, which refers to the functionally correct RTL implementation that best fits the user-defined optimization objectives in Algorithm 2, using their designed testbench. At the same time, the validator will record the errors reported from the simulator. If none of the variants fully pass the simulation, the agent will begin another iteration with the failed code with the fewest errors.

To avoid infinite loops, a *debugging curb* monitors the iteration count C . If the number of iterations exceeds C , the system halts and requests a human-written debugging manual for subsequent attempts. The human-written debugging manual should point out what's wrong in the code and that response will be attached to the prompt for the debugging code generation from this point on. Upon successful debugging, the best-performing code follows the green path in Figure 3 and is placed into the output queue. This RTL implementation and validation process iterates until all required submodules have been retrieved or generated in **Phase II**, or until all chiplet components with full RTL implementation have been completed in **Phase III**.

D. Design Space Exploration

Design Space Exploration is one of the major steps in **Phase III**, as illustrated in Section II. After collecting the necessary submodule PPAs, the flow will proceed to another agent, called Multi-Granularity Design Space Explorer (Figure 1), to derive the optimal hardware parameters for the input algorithm.

Multi-Granularity Design Space Explorer: In a typical chiplet design flow, DSE poses a significant challenge to the design flow, which is mainly attributed to the extensive design space. Given i parameters, even if each parameter is limited to only 10 possible values, the total number of configurations reaches 10^i , leading to long runtime. Therefore, designers often use heuristic baseline configurations to find suboptimal but feasible solutions. On the other hand, relying solely on LLMs can compromise precision. To address this challenge, this paper proposes a Multi-Granularity Design Space Explorer, where we

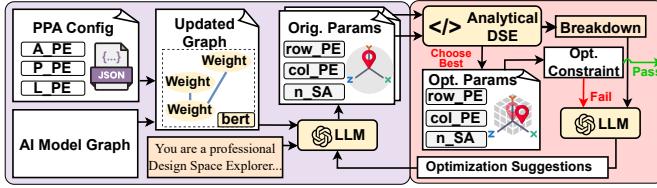


Fig. 4. Workflow of Multi-Granularity Design Space Explorer.

integrate the strengths of both LLM-based DSE and analytical DSE.

Provided in Figure 4, the PPA metrics of submodules are first used to update the node and edge weight in the extracted AI Model Graph, which represents the estimated computing and interconnection overhead of each layer. Given the AI-to-hardware simulation information, LLMs then function as a design space explorer and leverage its domain knowledge to derive M sets of coarse-grained configuration baseline from the whole design space. A precise analytical DSE then conducts refinement by iteratively adjusting the parameters within a limited range based on the coarse-grained configurations, which finally identifies one set of optimal configuration from M sets under the constrained design space.

After selecting the best configuration set, we first evaluate whether it satisfies the predefined constraints, including all PPA (Power, Performance, Area) targets. If the constraints are met, the configuration is accepted and output via the green path. Otherwise, we perform a breakdown of the analytical metrics into computing and interconnection components to identify the performance bottleneck. This bottleneck, along with its associated parameters, is then provided to the LLMs, which generates optimization suggestions for the next DSE iteration. Upon completion of the DSE process, the flow proceeds to the full chiplet RTL implementation, followed by **Phase IV**, which involves the final layout design. **Layout Configurator:** In **Phase IV**, the final layout is implemented using OpenROAD [33]. To generate GDSII files, an LLM-based agent, **Configurator**, automatically produces and iteratively revises configuration files by parsing the OpenROAD tutorial and error messages. It tunes parameters such as wire length, spacing, chip size, and congestion tolerance, ensuring successful execution of the layout flow.

IV. EVALUATION

A. Experimental Setup

Dataset. Dataset I is composed of simple designs, including the Multiplexer, the Adder, the Decoder, the Barrel Shifter, the Systolic Array, the AES Block Cipher and the UART. These designs are the same as the first dataset in ROME [32] and are used to test the generation and validation ability of the Retrieval-Augmented Code Generator and Diverseflow Validator. Given the focus of this study on chiplets, in Dataset II, we select and evaluate chiplet designs for different AI algorithms. Typically, their components involve a Systolic Array with PEs and buffers to implement ‘Conv1D’/‘Linear’/‘Conv2D’ layers and activation modules to implement other activation layers. For interconnection, we employ channels of the AIB 2.0 interface

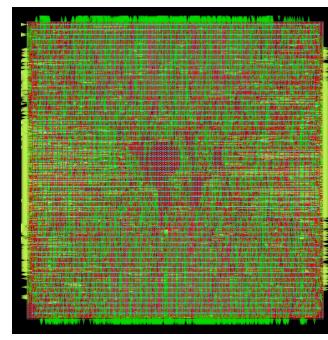


Fig. 5. Layout of one chiplet design for BERT algorithm.

[36] for the NoP while adopting multiple links per channel with 8 bits for NoC interface to ensure same bandwidth with NoP. We use AI model, including BERT, LLaMA and GPT for algorithm-hardware mapping.

Configuration and Platforms. Our MAHL employs three LLM models to perform RTL hierarchy-aware design generation and validation. We use one closed-source model, GPT-4o[37], and two open-source models, LLaMA 3.3-70B[38] and Gemma 3-27B[39]. For the GPT-4o model, we configure the temperature to 0.8 to approximate the behavior of its online version. For the local models, we use a temperature of 0.6, following the default setting in the Ollama library.

The Diverseflow Validator is configured with $K = 2$ threads, one with noise and one without noise. We define the curb count to be $C = 5$ and noise percentage to be $P = 30\%$. To ensure a fair comparison and save execution time, we only conduct 1 iteration of debugging for simple design, while for chiplet design, we set the debugging iterations to be 5. For the Multi-Granularity Design Space Explorer, we search $M = 80$ sets of coarse-grained configurations to enable comparable numbers of design points to CLARIE (expert-based) [40]. For Section IV-B, we conduct 10 trials to measure Pass Rate, while for Section IV-C, the number of trials is set to 20.

For the simulation EDA tools, we integrate the ICARUS Verilog [41] to automate the workflow. For hardware implementations that exist in the Compute & Interconnect Library, we use the same cycle-accurate chiplet simulator as CLARIE when conducting analytical DSE. The LLM-aided hardware design is synthesized based on a TSMC 28nm technology using Design Compiler to enable fair comparison with CLARIE for PPA comparison in Section IV-C. For the layout design, we resynthesize one chiplet and conduct complete layout procedure under SkyWater 130nm with OpenROAD [33], which is for the BERT model under compact area mode. The chiplet is composed of 32 32x32 Systolic Array, 16 Activation Units (GELU and TANH modules), connected through the 320 Gbps AIB channels, as shown in Figure 5. Most experiments are run on a Linux server with 4×A6000 graphics cards and a CPU of AMD EPYC 7763 64-Core Processor.

Experimental Metric. We evaluate the experimental results using multiple metrics. For generation accuracy, we apply

| | |
|------------------------------|--|
| Technology (nm) | SkyWater 130 |
| Chip Area (mm ²) | 15.0x15.0 |
| Supply (V) | 1.8 |
| Frequency | 1GHz |
| Number of Computing Unit | 32 32x32 Systolic Array 16 Activation Modules |
| Inter-connection | 320 Gbps AIB |

TABLE I
GENERATION ACCURACY COMPARISON ON LLM-GENERATED HIERARCHICAL PROMPT OVER 6 DESIGNS.

| | | GPT-4o | | | | | | Llama3.3:70b | | | | | | Gemma3.3:27b | | | | | |
|-----------------------------|---------------|--------|------|------|------|------|------|--------------|------|------|------|------|------|--------------|------|------|------|------|------|
| | | N | H | HR | ND | HD | HRD | N | H | HR | ND | HD | HRD | N | H | HR | ND | HD | HRD |
| Mux 64to1 | Pass@1 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 0.90 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 0.40 | 1.00 | 1.00 | 0.80 | 1.00 | 1.00 |
| | Pass@5 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 0.99 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 0.92 | 1.00 | 1.00 | 0.99 | 1.00 | 1.00 |
| Adder 64bit | Pass@1 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 0.60 | 1.00 | 1.00 | 0.80 | 1.00 | 1.00 | 0.40 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 |
| | Pass@5 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 0.98 | 1.00 | 1.00 | 0.99 | 1.00 | 1.00 | 0.92 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 |
| Decoder 5to32 | Pass@1 | 0.60 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 0.80 | 0.90 | 1.00 | 0.90 | 1.00 | 1.00 | 0.00 | 0.50 | 0.60 | 0.00 | 0.50 | 0.60 |
| | Pass@5 | 0.98 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 0.99 | 0.99 | 1.00 | 0.99 | 1.00 | 1.00 | 0.00 | 0.96 | 0.98 | 0.00 | 0.96 | 0.98 |
| Barrel Shifter 32bit | Pass@1 | 0.80 | 1.00 | 1.00 | 0.90 | 1.00 | 1.00 | 0.20 | 0.00 | 0.40 | 0.30 | 0.00 | 0.40 | 0.00 | 0.00 | 0.10 | 0.00 | 0.00 | 0.50 |
| | Pass@5 | 0.99 | 1.00 | 1.00 | 0.99 | 1.00 | 1.00 | 0.67 | 0.00 | 0.92 | 0.83 | 0.00 | 0.92 | 0.00 | 0.00 | 0.41 | 0.00 | 0.00 | 0.97 |
| Systolic Array 4x4 | Pass@1 | 0.00 | 0.30 | 0.60 | 0.30 | 0.50 | 0.70 | 0.40 | 0.50 | 0.80 | 0.70 | 0.60 | 0.80 | 0.00 | 0.00 | 0.20 | 0.00 | 0.00 | 0.20 |
| | Pass@5 | 0.00 | 0.83 | 0.98 | 0.83 | 0.96 | 0.99 | 0.92 | 0.96 | 0.99 | 0.97 | 0.98 | 0.99 | 0.00 | 0.00 | 0.67 | 0.00 | 0.00 | 0.67 |
| UART 8bit | Pass@1 | 0.00 | 1.00 | 1.00 | 0.20 | 1.00 | 1.00 | 0.60 | 0.70 | 1.00 | 0.70 | 1.00 | 1.00 | 0.50 | 0.40 | 0.80 | 0.60 | 0.50 | 0.80 |
| | Pass@5 | 0.00 | 1.00 | 1.00 | 0.67 | 1.00 | 1.00 | 0.98 | 0.99 | 1.00 | 0.99 | 1.00 | 1.00 | 0.97 | 0.92 | 0.99 | 0.98 | 0.97 | 0.99 |

TABLE II

COMPARISON OF OPTIMIZED DSE RESULT FROM MULTI-GRANULARITY DESIGN SPACE EXPLORER WITH GPT-4o WITH DSE FROM BASELINE CLARIE ([40]), A HUMAN EXPERT EXPERIENCE DEPENDENT FRAMEWORK. THE BANDWIDTH OF BOTH NoC AND NoP $BW_{NoC/NoP}$ IS MEASURED IN Gbps.

(a) High Performance Mode.

| | CLARIE ([40]) | | | MAHL | | |
|-----------------------|---------------|-------|-------|------------|-------|-------|
| | BERT | LLaMA | GPT | BERT | LLaMA | GPT |
| sizeSA | 32×64 | 32×64 | 32×64 | 32×64 | 32×64 | 32×64 |
| n _{SA} | 128 | 128 | 128 | 64 | 128 | 128 |
| type _{act} | GELU, TANH | SILU | GELU | GELU, TANH | SILU | GELU |
| n _{act} | 64 | 64 | 64 | 64 | 64 | 64 |
| BW _{NoC/NoP} | 320 | 320 | 320 | 320 | 320 | 320 |

(b) Compact Area Mode.

| | CLARIE ([40]) | | | MAHL | | |
|-----------------------|---------------|-------|-------|------------|-------|-------|
| | BERT | LLaMA | GPT | BERT | LLaMA | GPT |
| sizeSA | 32×32 | 32×32 | 32×32 | 32×32 | 16×16 | 32×32 |
| n _{SA} | 32 | 32 | 32 | 32 | 16 | 32 |
| type _{act} | GELU, TANH | SILU | GELU | GELU, TANH | SILU | GELU |
| n _{act} | 16 | 16 | 16 | 16 | 8 | 16 |
| BW _{NoC/NoP} | 320 | 320 | 320 | 320 | 320 | 320 |

Pass@k metrics [32] to assess the generation pass rate:

$$\text{pass}@k = \mathbb{E}_{\text{Problems}} \left[1 - \frac{\binom{n-c_p}{k}}{\binom{n}{k}} \right] \quad (3)$$

where n is the total number of generations, c_p is the number of successes, and k is the number of attempts considered. We apply *Pass@1* and *Pass@5* in our experiment. We also evaluate the generation quality, i.e., PPA optimization, based on metrics including power, latency and area.

B. Simple Design Generation with MAHL

As shown in Table I, the simple design generation with MAHL is composed of 6 different metrics as follows:

- **N** stands for conventional LLM generation with Non-hierarchical prompt;
- **H** stands for Hierarchical generation with Hierarchical Module Description Generator alone;
- **HR** stands for Hierarchical Generation with Retrieval-Augmented Code Generator alone;
- **ND** stands for Non-hierarchical generation with Diverseflow Validator alone;
- **HD** stands for Hierarchical Generation with Diverseflow Validator alone;
- **HRD** stands for Hierarchical Generation with Retrieval-Augmented Code Generator and Diverseflow Validator.

Note that when we measure the pass rate, we only count it as a success when it passes both the syntax and functional tests. Also, there is no combination of non-hierarchical generation with the Retrieval-Augmented Code Generator, since we do not store the non-hierarchical code for this evaluation.

Improvement with Hierarchical Generation: The hierarchical generation approach yields up to an improvement of 0.5 in *Pass@1*, and provides an average gain of approximately 20%–40% in *Pass@1* across most cases. Additionally, it enables the integration of the retrieval approach, further enhancing module reuse.

Improvement with Diverseflow Validation: The Diverseflow Validator, two parallel threads within a single validation iteration, demonstrates excellent performance. It achieves up to a 0.6 improvement in *Pass@1* and also provides consistent gains across other cases.

Improvement with Retrieval-Augmented Code Generation: The code retrieval component typically improves the pass rate by 10%–40%. It maintains a library of essential sub-modules for each generation, which are pre-verified as described in Section III.

Improvement with the Whole MAHL Framework: The overall framework consistently enhances generation performance across all cases, with a maximum improvement of 1.0 in *Pass@1*. Compared to the Non-Hierarchical Generation baseline, our full design (HRD) achieves an average *Pass@1* gain of 44.67%.

C. Chiplet IP Generation with MAHL

For chiplet IP design, Dataset II specializes its configuration for three AI models, which are BERT, GPT and LLaMA. Besides the same generation and validation function of MAHL as that used in the simple Verilog design generation, this experiment incorporates the AI-Hardware Hierarchical Parser and the Multi-Granularity Design Space Explorer to realize the whole flow of chiplet design. We apply the same mapping strategy as the one in CLARIE [40] for fair comparison, which is a chiplet design framework based on simulation and human expert experience. We allow a total of $n = 20$ generations and $M = 80$ coarse-grained configurations for each design. For the design objective, we choose *high_performance* and *compact_area* respectively. Other than the user-defined

TABLE III

PPA OPTIMIZATION RESULT INCLUDING PASS@5, ENERGY (UJ), LATENCY (NS), AREA (MM²) AND POWER DENSITY (MW/MM²) COMPARED WITH GENERAL LLMs AND THREE-YEAR HARDWARE DESIGN EXPERT (REPRESENTED BY [40]). ‘/’ REPRESENTS FAILURE IN LLM-BASED GENERATION OR UNAPPLICABLE FOR HUMAN EXPERT DESIGN. GREEN HIGHLIGHTS THE BEST RESULTS. WE USE GPT-4O AND LLAMA-3.3 AS THE GENERAL LLMs.

| | (a) High Performance Mode. | | | | | | | | | | | | | | |
|---------------|----------------------------|--------|--------------|--------|---------|--------|----------|---------------|--------|---------|--------|--------|-------------|--------|---------|
| | Pass@5 | Energy | BERT Latency | Area | P.D. | Pass@5 | Energy | LLaMA Latency | Area | P.D. | Pass@5 | Energy | GPT Latency | Area | P.D. |
| CLARIE | / | 647.11 | 2812.58 | 182.25 | 1262.43 | / | 34566.05 | 136219.25 | 182.25 | 1392.33 | / | 538.85 | 2220.71 | 182.25 | 1331.40 |
| GPT-4o | 0 | / | / | / | / | 0 | / | / | / | / | 0 | / | / | / | / |
| MAHL (ours) | 0.72 | 470.22 | 1806.54 | 236.81 | 1099.14 | 0.25 | 49848.65 | 123466.67 | 137.61 | 2933.96 | 0.60 | 595.78 | 2151.82 | 144.02 | 1922.46 |
| CLARIE | / | 647.11 | 2812.58 | 182.25 | 1262.43 | / | 34566.04 | 136219.25 | 182.25 | 1392.33 | / | 538.85 | 2220.71 | 182.25 | 1331.40 |
| Llama-3.3:70b | 0 | / | / | / | / | 0 | / | / | / | / | 0 | / | / | / | / |
| MAHL (ours) | 0.60 | 613.81 | 3132.10 | 132.45 | 1479.61 | 0 | / | / | / | / | 0.44 | 702.93 | 2194.76 | 172.16 | 1860.34 |

| | (b) Compact Area Mode. | | | | | | | | | | | | | | |
|---------------|------------------------|--------|--------------|-------|---------|--------|----------|---------------|------|---------|--------|--------|-------------|-------|---------|
| | Pass@5 | Energy | BERT Latency | Area | P.D. | Pass@5 | Energy | LLaMA Latency | Area | P.D. | Pass@5 | Energy | GPT Latency | Area | P.D. |
| CLARIE | / | 647.11 | 12223.84 | 25 | 2117.53 | / | 34566.05 | 682904.83 | 25 | 2024.65 | / | 538.85 | 8956.54 | 25 | 2406.51 |
| GPT-4o | 0 | / | / | / | / | 0 | / | / | / | / | 0 | / | / | / | / |
| MAHL (ours) | 0.60 | 503.78 | 12228.47 | 21.69 | 1899.37 | 0.25 | 27562.16 | 2660426.90 | 1.61 | 6434.81 | 0.60 | 399.50 | 11059.74 | 3.62 | 9978.45 |
| CLARIE | / | 647.11 | 12223.84 | 25 | 2117.53 | / | 34566.04 | 682904.83 | 25 | 2024.65 | / | 538.85 | 8956.54 | 25 | 2406.51 |
| Llama-3.3:70b | 0 | / | / | / | / | 0 | / | / | / | / | 0 | / | / | / | / |
| MAHL (ours) | 0.44 | 501.54 | 41956.70 | 6.23 | 1918.74 | 0.44 | 22869.55 | 816798.56 | 4.26 | 6572.54 | 0.25 | 453.62 | 9471.36 | 13.14 | 3644.90 |

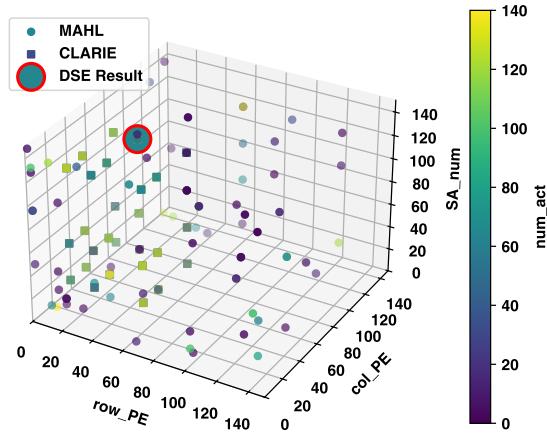


Fig. 6. Design space comparison of the computing parameters between CLARIE (human) and MAHL (ours) on BERT algorithm.

optimization objective mentioned in Section III-C, we also extend the decision making of best results by adding two soft constraints, abstracted as follows:

$$x^* = \arg \max_{x \in S} O(x), \quad S = X' \text{ if } X' \neq \emptyset \text{ else } X \quad (4)$$

$$X' = \{x \in X \mid P_1(x) \geq T_1, P_2(x) \geq T_2\} \quad (5)$$

Here, $P_1(x)$ and $P_2(x)$ represents two soft constraints other than the optimization objective in PPA. T_1 and T_2 are the thresholds for area and power density. In our experiment, we set T_1 to be 250 mm² and T_2 to be 2500 mW/mm².

As shown in Table II, the configuration is evaluated and found to be close to the golden configurations identified by CLARIE, which is attributed to the integration of LLM-based DSE and analytical DSE without manually identify the baseline. The design space of MAHL is largely extended compared to CLARIE, as shown in Figure 6.

As shown in Table III, our experiments display that utilizing MAHL enhances the generation accuracy compared to conventional LLMs. Specifically, $\text{Pass}@5$ rises from 0 to 0.72 for BERT with GPT-4o and 0 to 0.44 for GPT with Llama-3.3 under high performance mode. Even though few of the LLM-generated

chiplet designs, such as that for LLaMA under compact area mode, still struggle to reach the level of better trade-off from human experts, the PPA performance of most chiplet designs are already on the same order of magnitude as human expert, demonstrating its great potential for automatic generation and exploration of chiplet design. Insightfully, we observe that LLM-based generation tends to perform better on the primary design objective while underperforming compared to human experts on softer metrics, such as the power density represented by $P_2(x)$. This indicates that the LLM-based framework has yet to achieve the comprehensive trade-off among all design factors that should be taken into account for chiplet design.

When looking into general LLMs integrated in our MAHL framework, the results reflect that GPT-4o would bring more correct generations and better results on the design objective than Llama-3.3 in most cases, while Llama-3.3 tends to have a better trade-off of all hardware design factors considering $P_1(x)$ and $P_2(x)$. However, compared to using conventional general-purpose LLMs for generation, they both exhibit a significant improvement in success rate, which fails in all cases when generating complex chiplet design.

V. CONCLUSION

In this paper, we propose MAHL, a LLM-driven chiplet generation framework. With integrating promising techniques with LLM generation, MAHL exhibits its potential to be an effective solution to flattened generation, high validation cost and imprecise parameter optimization presented by directly using conventional LLMs. Extensive experiments show that MAHL can reach an improved hardware generation accuracy. Our framework also supports chiplet IP generation with comparable PPA performance with human expert under certain optimization objectives for specific AI models.

VI. ACKNOWLEDGMENT

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