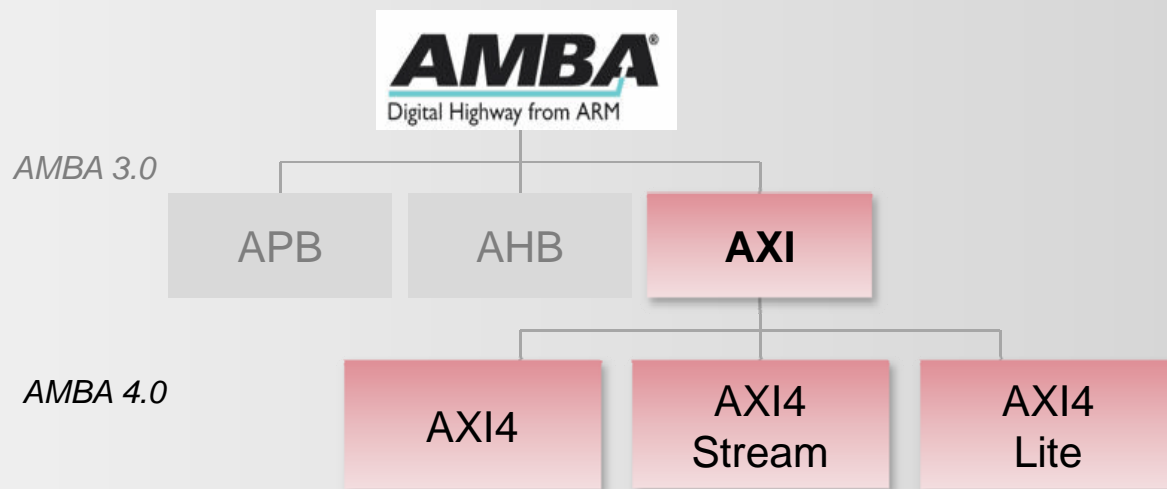# AXI4 Overview
- Benefits of Adopting AXI4
- Protocol Overview

AMBA® AXI4™ - Advanced Extensible Interface

- **Latest version of AMBA - Industry standard on-chip communication**
- **Enables higher performance vs. existing bus architectures**
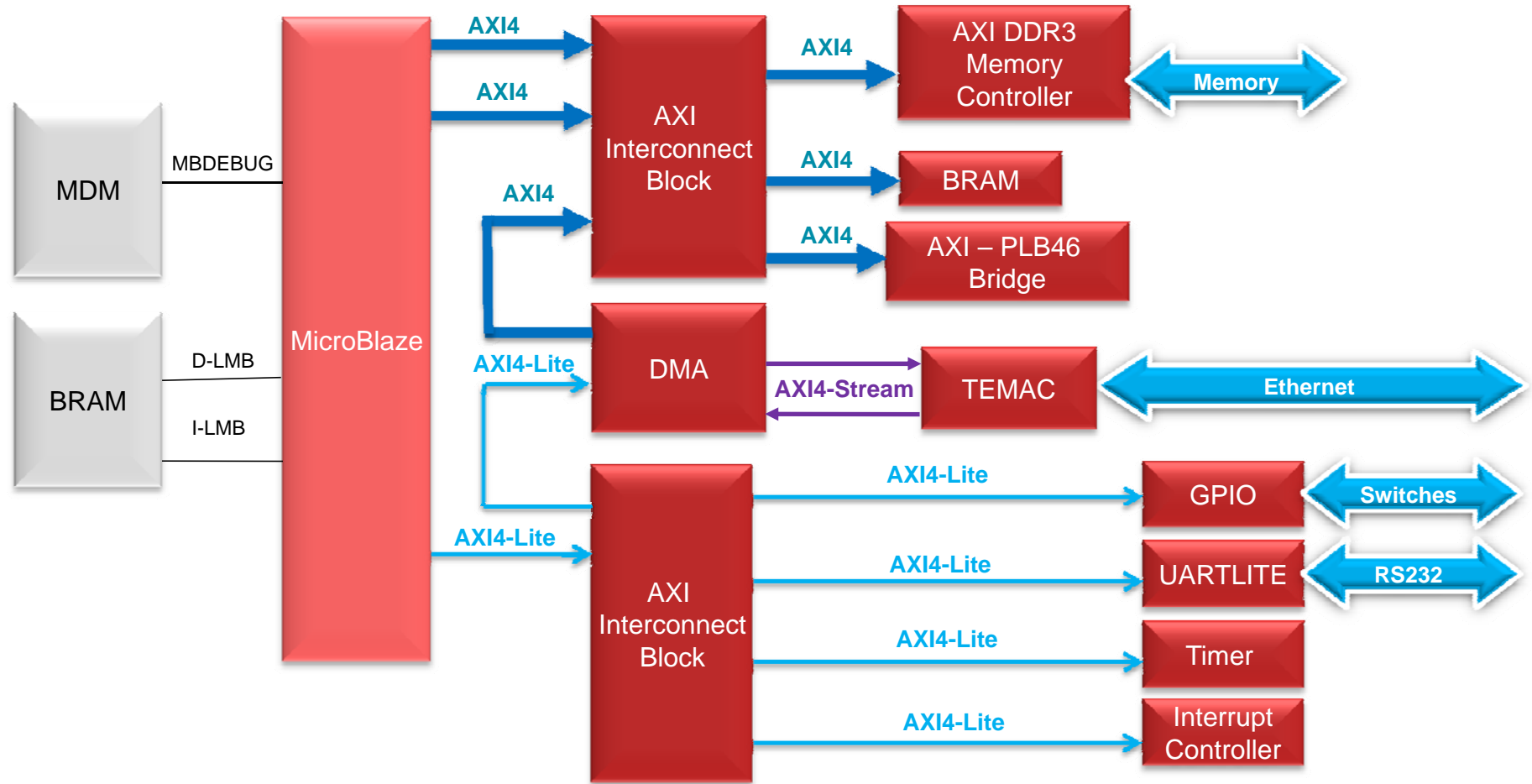- **Supports FPGA designs**

ARM and Xilinx partnered to develop AXI4 standard
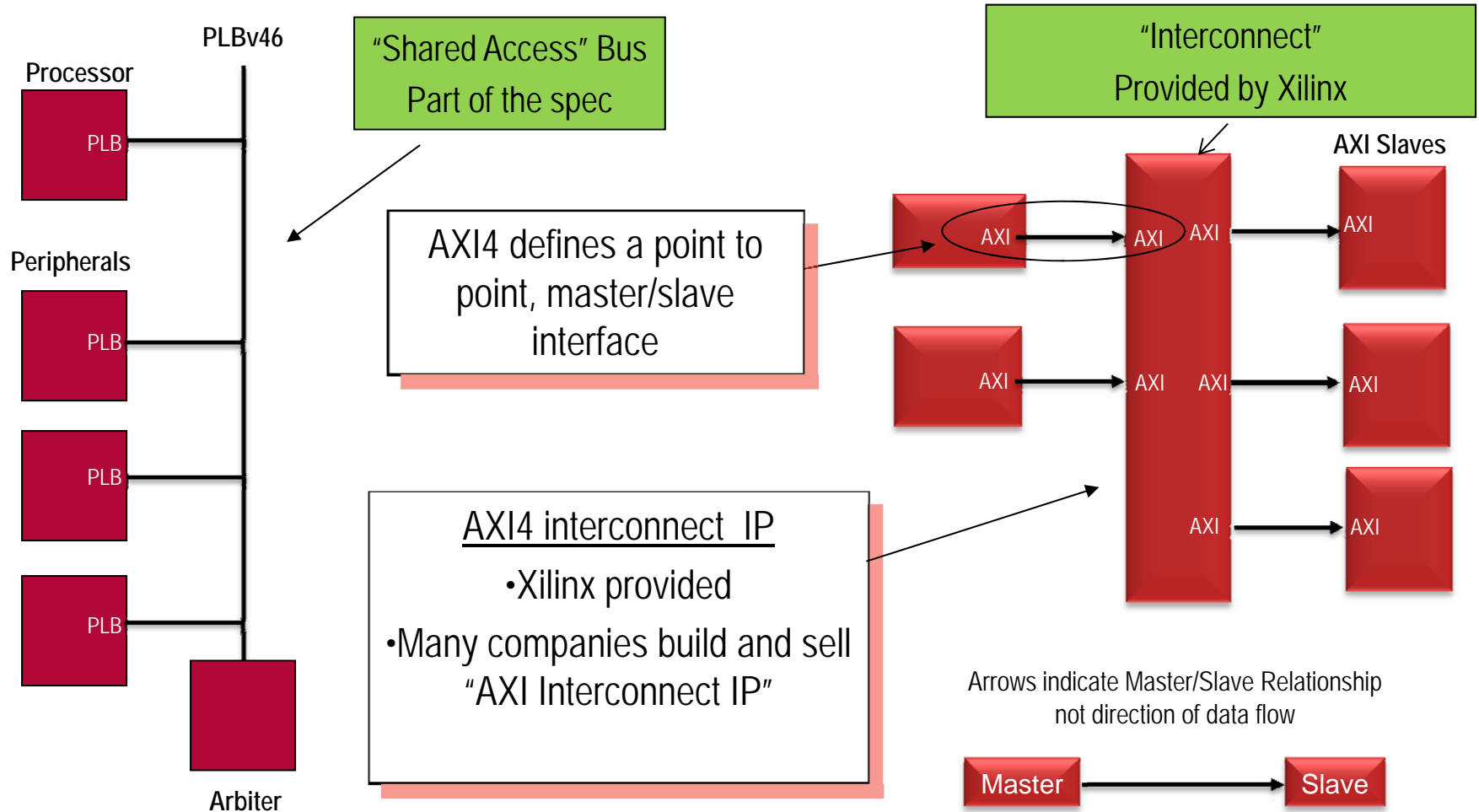
Broader IP Availability- ARM Connected Community

Over 400 ARM partners for IPs and Tools on the market

Increased Productivity – AXI4 supports Memory Mapped, Control and Streaming Applications
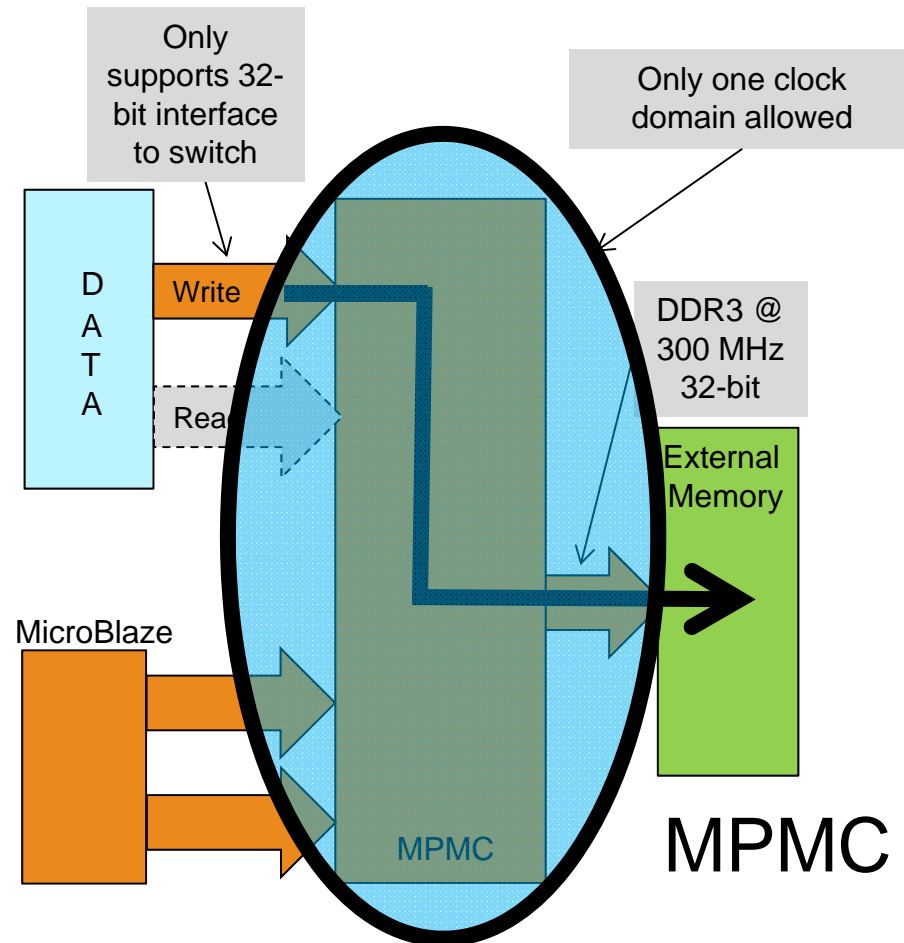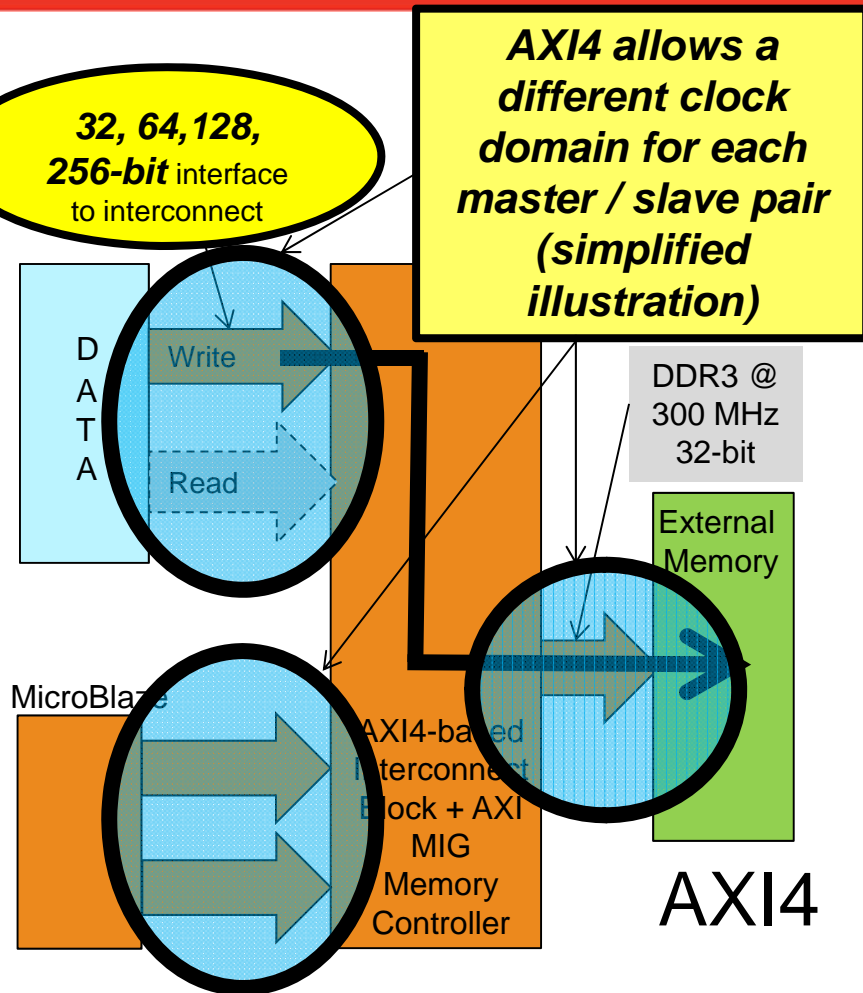

Single Interconnect Standard for IP across All Domains

AXI4 is an Interface Specification

PLBv46

Processor

PLB

Peripherals

PLB

PLB

PLB

Arbiter

"Shared Access" Bus
Part of the spec

"Interconnect"
Provided by Xilinx

AXI4 defines a point to point, master/slave interface

AXI Slaves

AXI → AXI AXI → AXI

AXI → AXI AXI → AXI

AXI → AXI

AXI4 interconnect_IP
•Xilinx provided
•Many companies build and sell "AXI Interconnect IP"

Arrows indicate Master/Slave Relationship not direction of data flow

Master → Slave

PLBv46 is a Bus Spec / AXI is an Interface Spec

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AXI4 Memory Interface vs. Multi Port Memory Controller with Local Link

32, 64,128, 256-bit interface to interconnect

AXI4 allows a different clock domain for each master / slave pair (simplified illustration)

DATA

Write

Read

DDR3 @ 300 MHz 32-bit

External Memory

MicroBlaze

AXI4-based Interconnect Block + AXI MIG Memory Controller

AXI4

Only supports 32-bit interface to switch

Only one clock domain allowed

DATA

Write

Read

DDR3 @ 300 MHz 32-bit

External Memory

MicroBlaze

MPMC

MPMC

AXI4 provides more flexibility in interface widths and clocking

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AXI4 Benefits

Availability

- Over 400 ARM partners for IPs and Tools on the market
- Xilinx and ARM connected communities developing IPs for FPGAs
- Helps You to invest with confidence

Productivity

- Single interconnect standard for
    - ALL domains
    - ALL Xilinx and Partner IPs
- Only one standard to learn
- Reduces time spent to integrate IPs within the design
- Provides higher performance (bandwidth) over PLBv46

Flexibility

- Configure the interconnect to meet system goals: Performance, Area, Power
- Enables ASIC verification methodology

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AXI4 Overview
 - **Benefits of Adopting AXI4**
 - **Protocol Overview**
 - ISE Design Suite AXI4 Support
 - Design Migration

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AXI4 - Advanced Extensible Interface
Standard Overview

- **AXI4**

  - Three flavors: AXI4, AXI4-Lite, AXI4-Stream

  - All three <u>share same</u> handshake rules and signal naming

	AXI4	AXI4-Lite	AXI4-Stream
Dedicated for	high-performance and memory mapped systems	register-style interfaces (area efficient implementation)	non-address based IP (PCIe, Filters, etc.)
Burst (data beta)	up to 256	1	Unlimited
Data width	32 to 1024 bits	32 or 64 bits	any number of bytes
Applications (examples)	Embedded, memory	Small footprint control logic	DSP, video, communication

AXI Fundamental Vocabulary

- **Channel**
  - Independent collection of AXI signals associated to a VALID signal

- **Interface**
  - Collection of one or more **channels** that expose an IP core's function, connecting a **master** to a **slave**
  - Each IP core may have multiple interfaces.
  - Also: AXI4, AXI4-Lite, AXI4-Stream

- **Bus**
  - Multiple-bit signal (not an **interface** or **channel**)

- **Transfer**
  - Single clock cycle where information is communicated, qualified by a VALID handshake. Data beat.

- **Transaction**
  - Complete communication operation across a **channel**, composed of a one or more **transfers**

- **Burst**
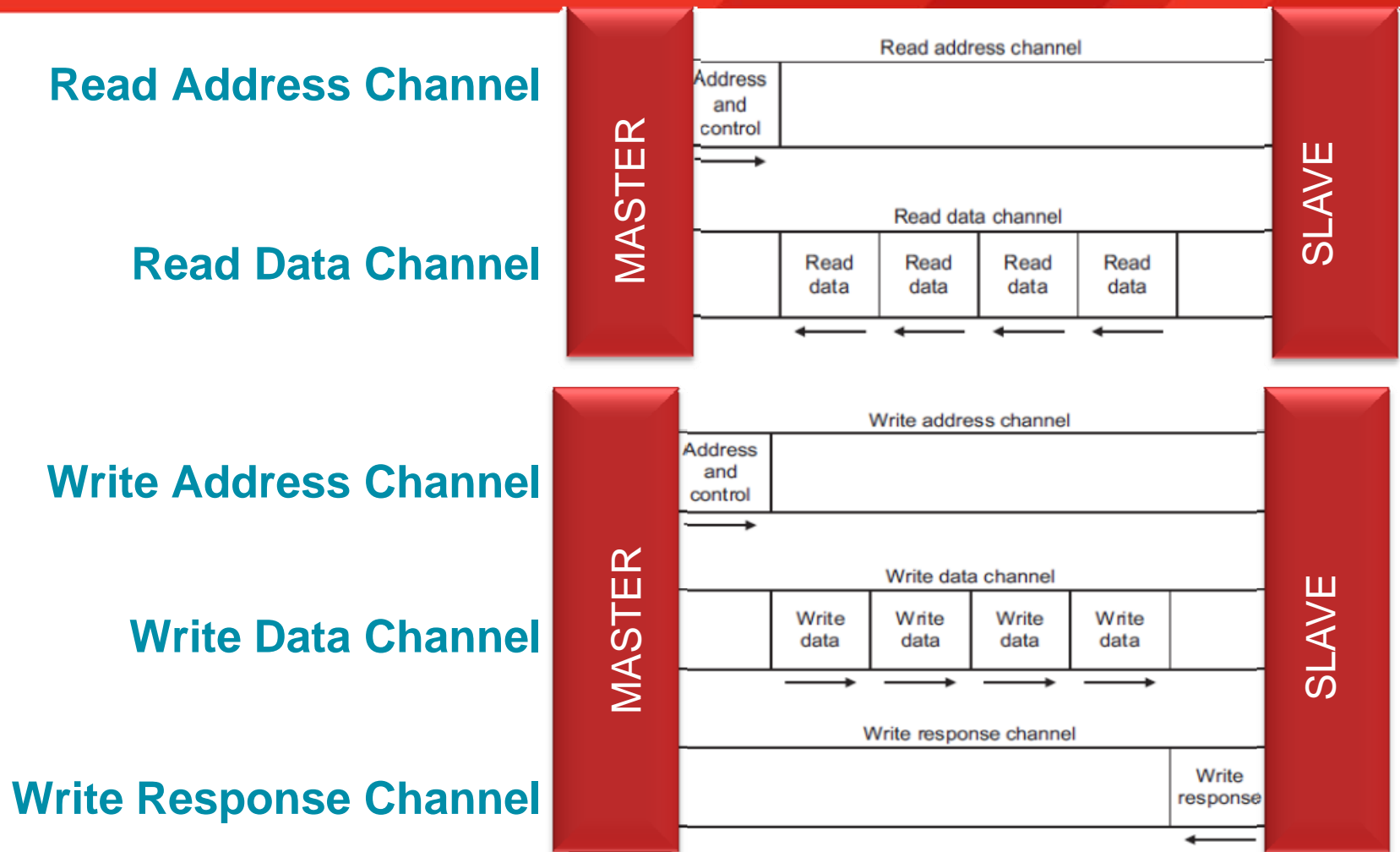 - **Transaction** that consists of more than one **transfer**

Basic AXI4 Handshaking

- *Master* asserts and holds VALID when data is available
- *Slave* asserts READY if able to accept data

- DATA and other signals transferred when VALID and READY = 1

- *Master* sends next DATA/other signals or deasserts VALID
- *Slave* deasserts READY if no longer able to accept data

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XILINX.
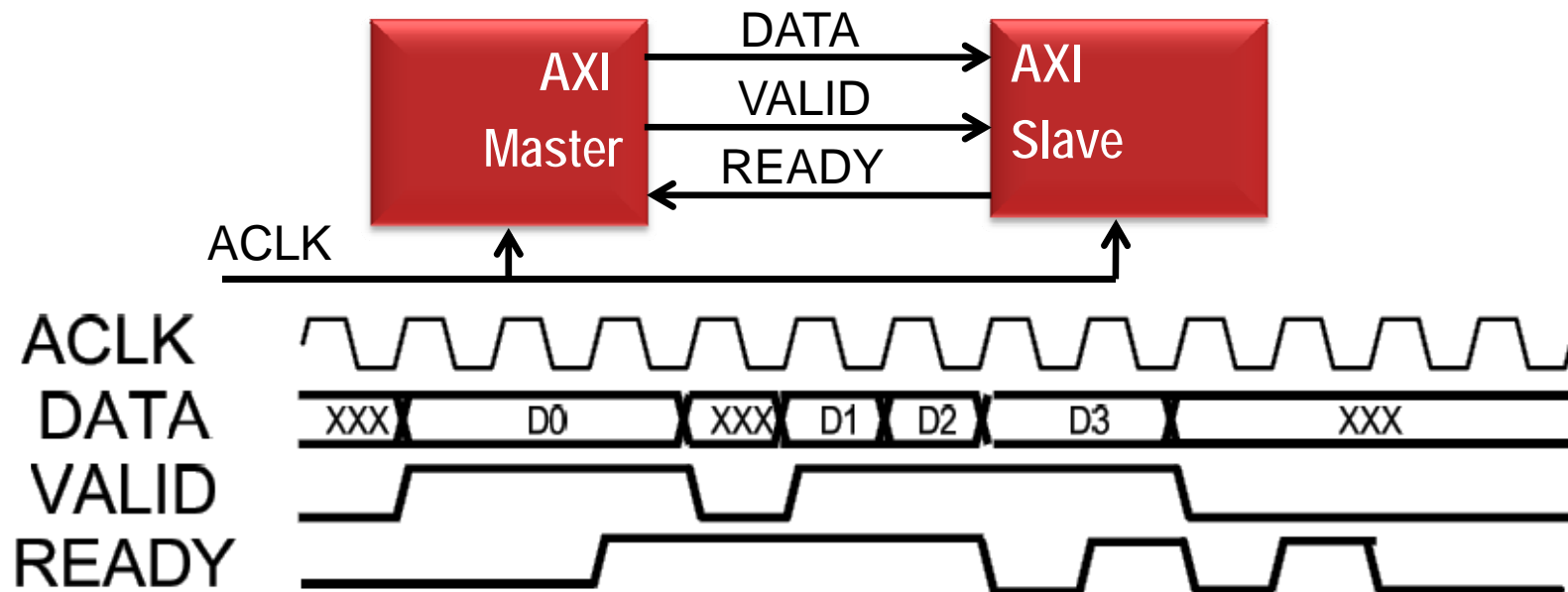
Basic AXI4 Signaling
5 Channels, Point to Point

Read Address Channel

Read Data Channel

Write Address Channel

Write Data Channel

Write Response Channel

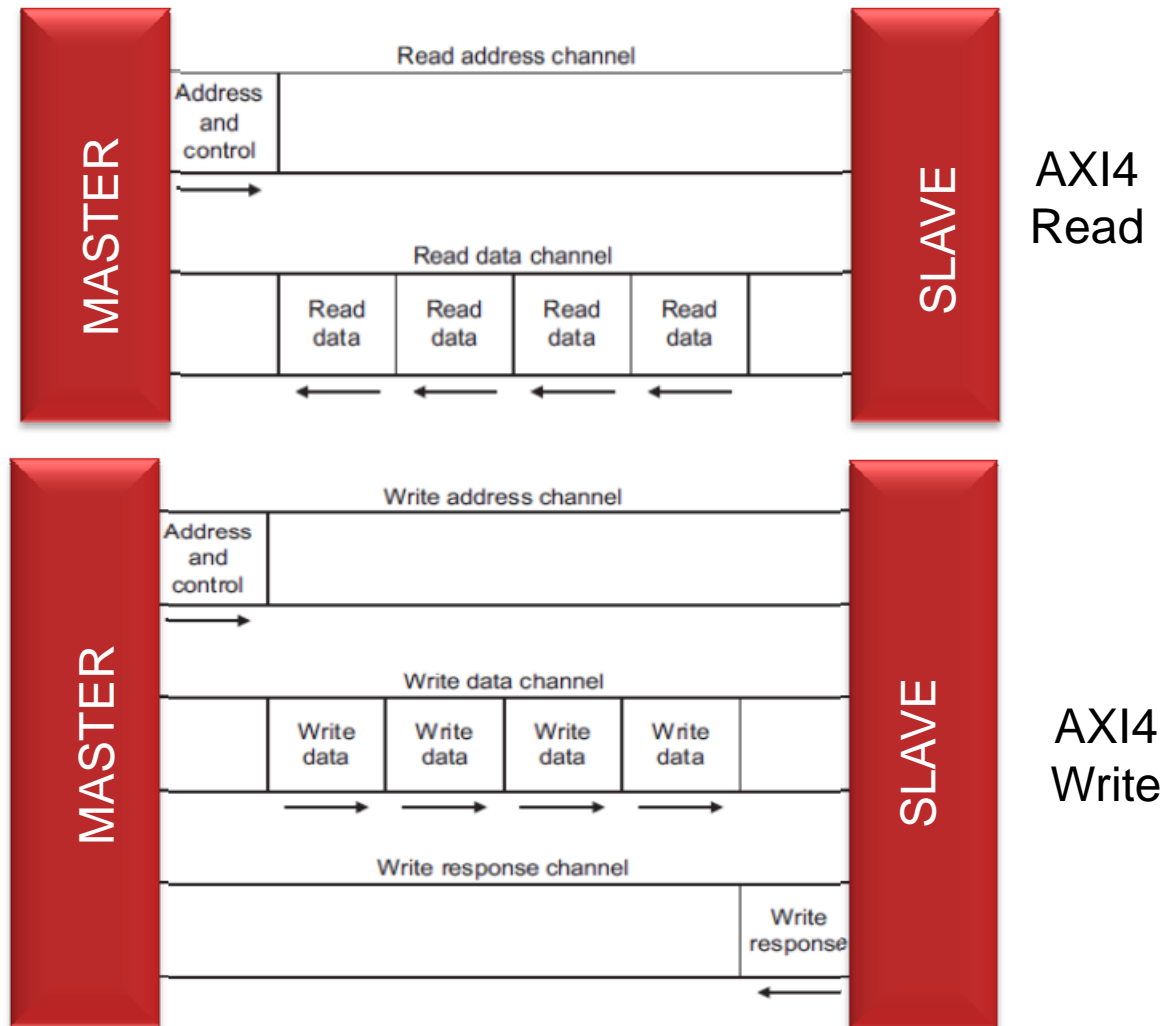AXI4, AXI4-Lite, AXI4-Stream are all simple variants of these 5 channels

The AXI Interface—AXI4

- **Single address multiple data**
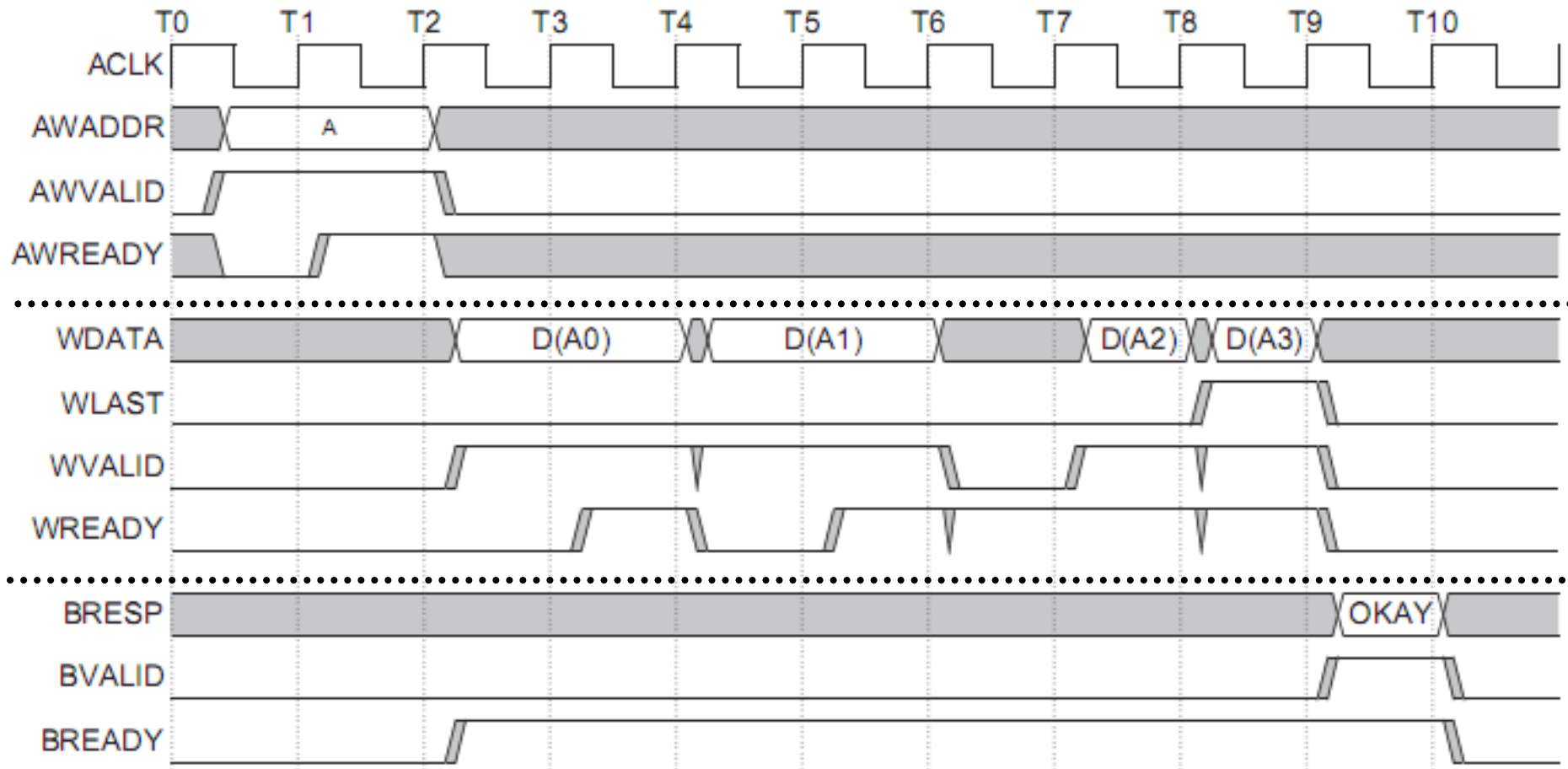 - Burst up to 256 data beats

- **Data Width parameterizable**
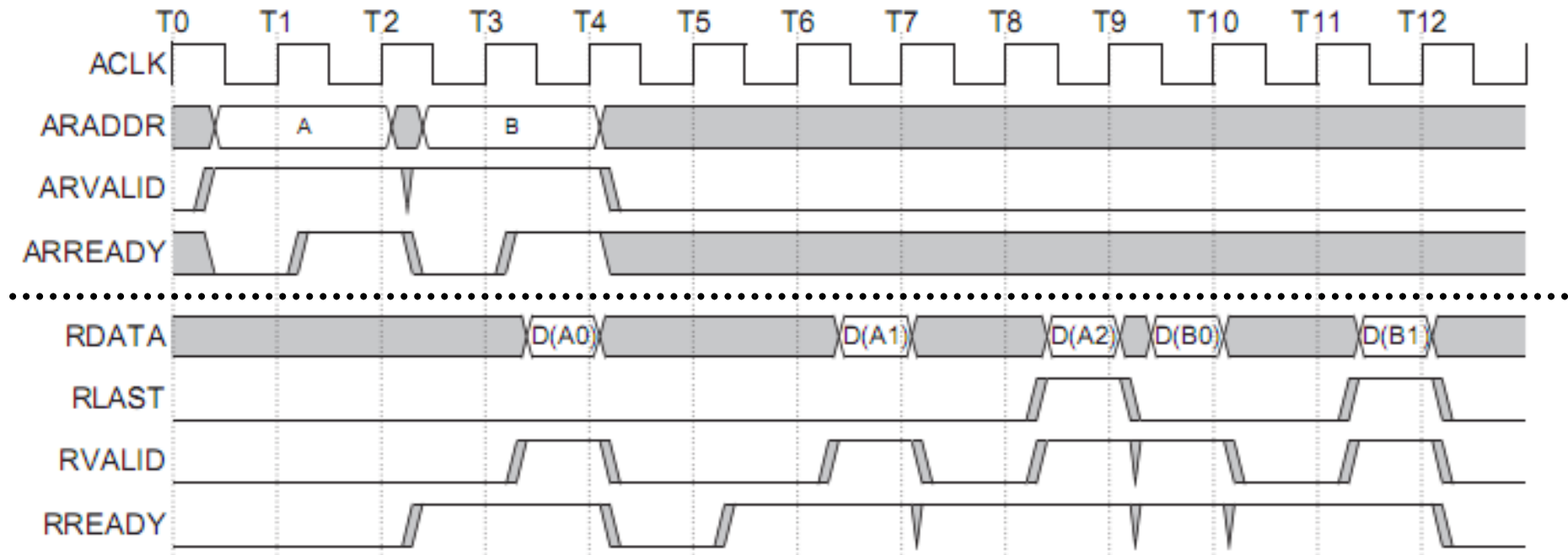 - 32, 64, 128, 256, 512, 1024 bits

AXI4 Read

AXI4 Write

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Example Transaction: AXI4 Write Burst

- **Four data writes**
- **Length and size of data write specified by Write Address Channel**
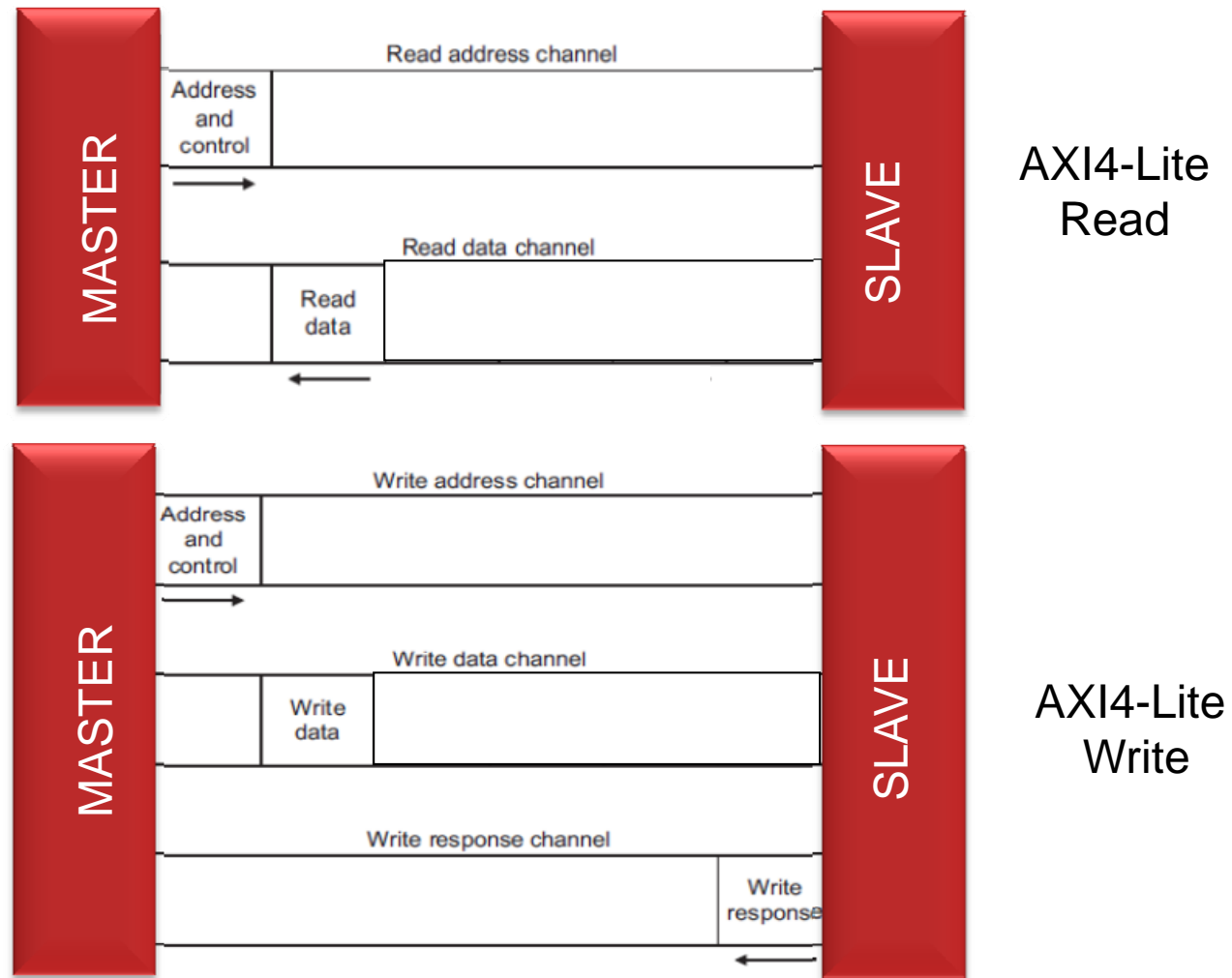
Example Transaction: AXI4 Read Burst (Pipelined address)

- **Pipelined read address A and B**
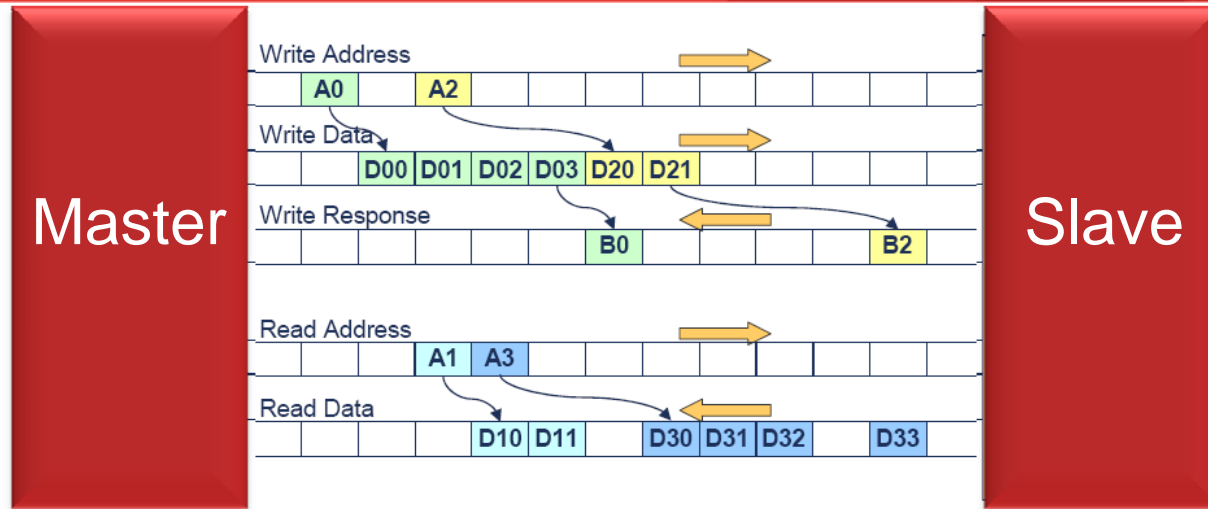- **Length and size of data read specified by Read Address Channel**

The AXI Interface—AX4-Lite

- **No burst**

- **Data width 32**

- **Very small footprint**

- **Bridging to AXI4 handled automatically by AXI_Interconnect (if needed)**

AXI4-Lite Read

AXI4-Lite Write

AXI4/AXI4-Lite
5 Channels

Write Address Channel
- AWID[m:0]
- **AWVALID**
- **AWREADY**
- **AWADDR[31:0]**
- AWLEN[7:0]
- AWSIZE[2:0]
- **AWPROT[2:0]**
- AWBURST[1:0]
- AWLOCK
- AWCACHE[3:0]
- AWREGION[3:0]
- AWQOS[3:0]

Write Data Channel
- **WVALID**
- **WREADY**
- **WDATA[n-1:0]**
- **WSTRB[n/8-1:0]**
- WLAST

Write Response Channel
- BID[m:0]
- **BVALID**
- **BREADY**
- **BRESP[1:0]**

Read Address Channel
- ARID[m:0]
- **ARVALID**
- **ARREADY**
- **ARADDR[31:0]**
- ARLEN[7:0]
- ARSIZE[2:0]
- ARBURST[1:0]
- **ARPROT[2:0]**
- ARLOCK
- ARCACHE[3:0]
- ARREGION[3:0]
- ARQOS[3:0]

Read Data Channel
- RID[m:0]
- **RVALID**
- **RREADY**
- **RDATA[n-1:0]**
- **RRESP[1:0]**
- RLAST

ACLK
ARESETn

AXI4-Lite signals bolded

The AXI Interface—AXI4-Stream

- **No address channel, no read and write, always just master to slave**
  - Effectively an AXI4 "write data" channel

- **Unlimited burst length**
  - AXI4 max 256
  - AXI4-Lite does not burst

- **Virtually same signaling as AXI4 Data Channels**
  - Protocol allows merging, packing, width conversion
  - Supports sparse, continuous, aligned, unaligned streams

AXI4-Stream Transfer