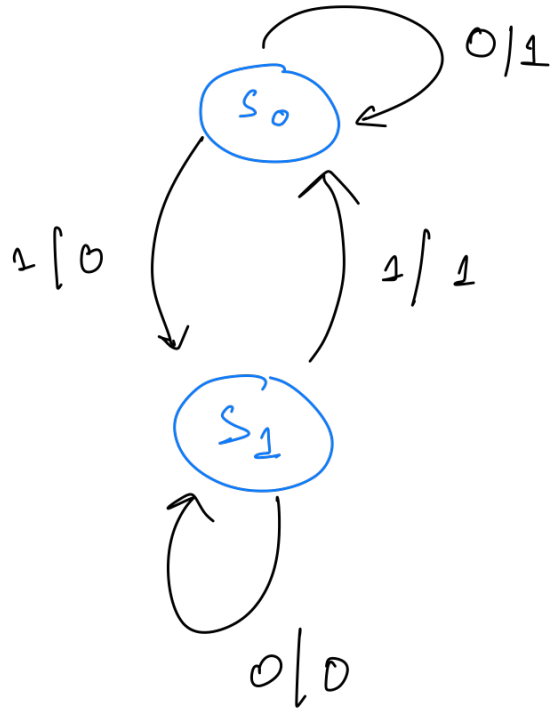
Q 2) odd parity generator

state diagram:




$S_0$ → initial state because no one has been encountred

$S_0$ : no. of 1s encounter after blank input are even

$S_1$ : no. of 1s encountered after blank input are odd

n-bit odd parity generator ⇒ generate parity of last n bits at $(n+1)^{th}$ output bit.

reset signal sent after 4 time units.

State Table:

| P.S | Next state, output | |
|---|---|---|
| | In | |
| | 0 | 1 |
| 0 | (0, 1) | (1, 0) |
| 1 | (1, 0) | (0, 1) |

Transition and Output table:

| PS | Next state In 0 | Next state In 1 | Output In 0 | Output In 1 |
|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |

2 states, we can use a D-flip flop

Excitation Table:

| PS $a$ | Input $i$ | NS $a'$ | FF input $D$ | O/p $O$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |

# K Maps

D

| a \ i | 0 | 1 |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 1 | 0 |

$D = \bar{a} \cdot i + a \cdot \bar{i}$

$D = a \oplus i$

O

| a \ i | 0 | 1 |
|---|---|---|
| 0 | 1 | 0 |
| 1 | 0 | 1 |

$O = \bar{a} \cdot \bar{i} + a \cdot i$

$O = y \cdot i$

## circuit diagram