**EMBEDDED SYSTEMS DESIGN (UCS** **704)**

**Assignments 1 to 12**

**Submitted by:**

**(102103186) GUNAAYAT KAUR**

**BE Fourth Year- COE**

**Submitted to:**

**Dr. Manisha**



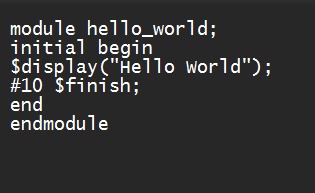
**Computer Science and Engineering Department**

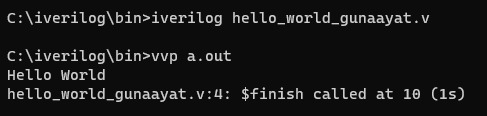
**Thapar Institute of Engineering and Technology, Patiala**

**NOVEMBER 2024**

**EXPERIMENT 1**

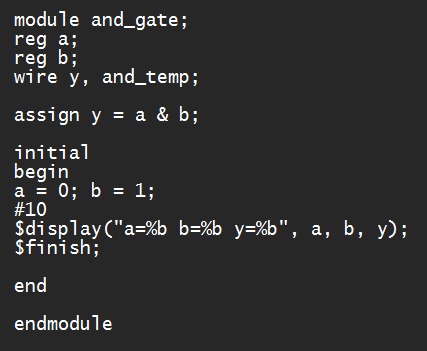
**HELLO WORLD**

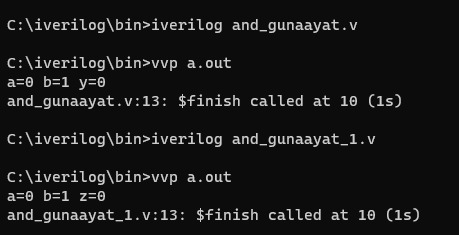




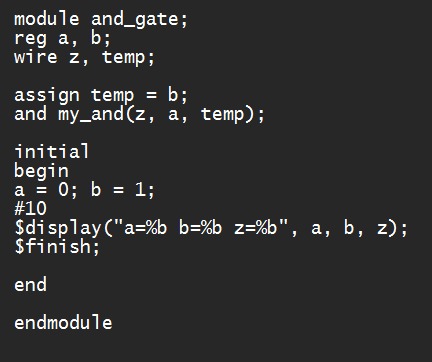
**AND GATE**

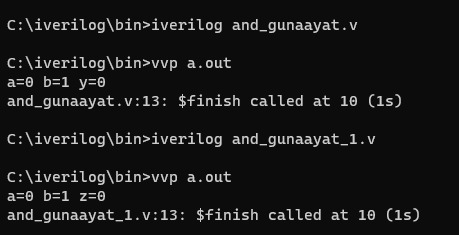
**Program 1**



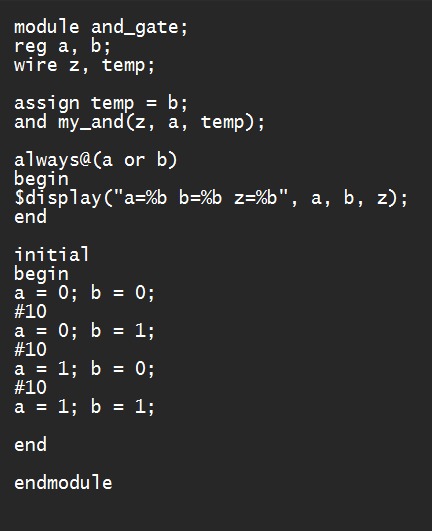


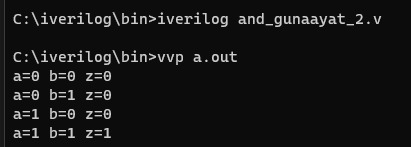
**Program 2**



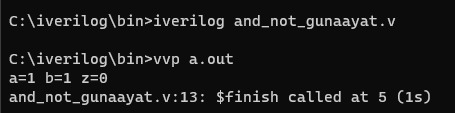
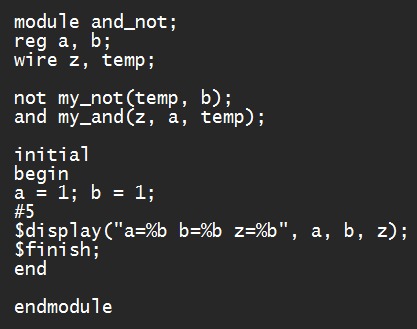


**Program 3**

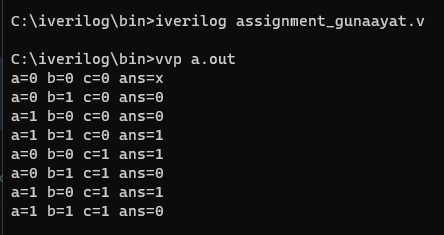
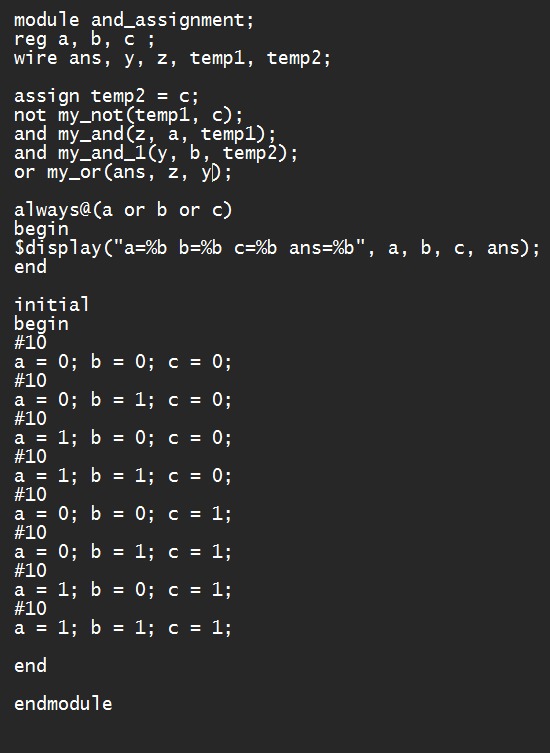




**AND and NOT**

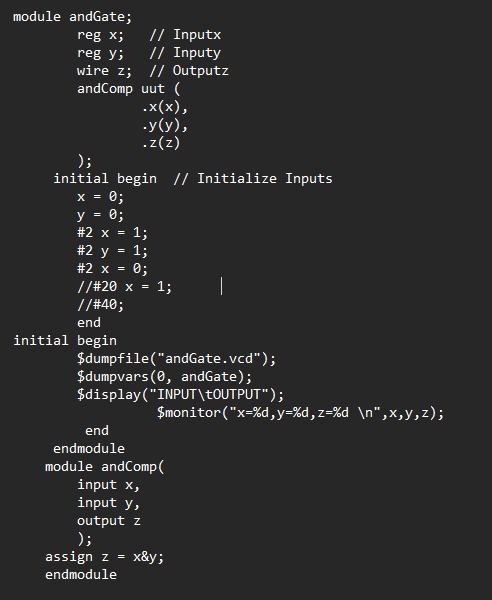


**Assignment Question**



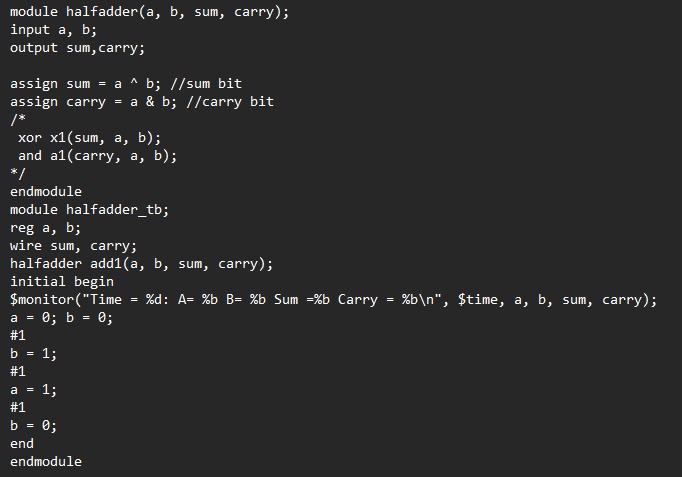
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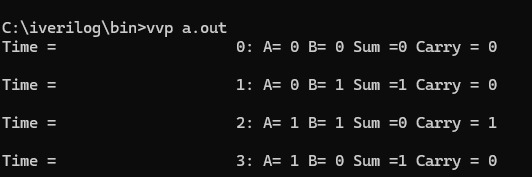
**AND GATE**





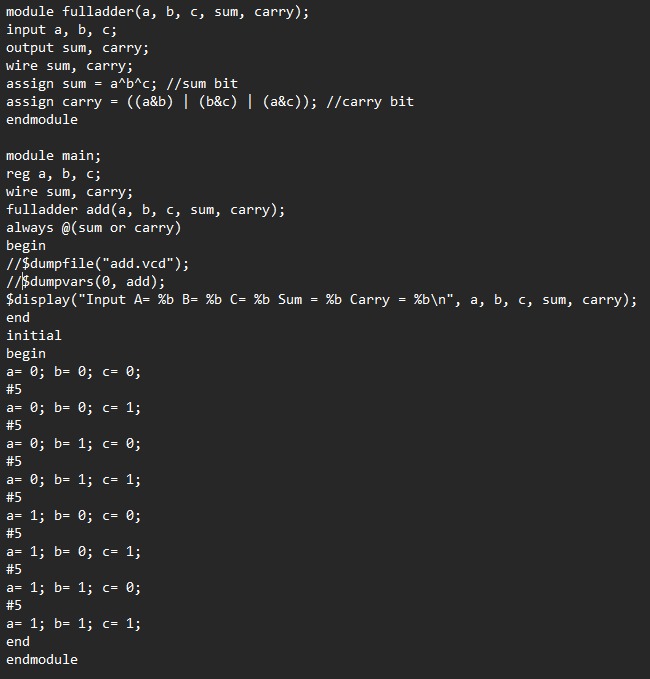
**HALF ADDER**

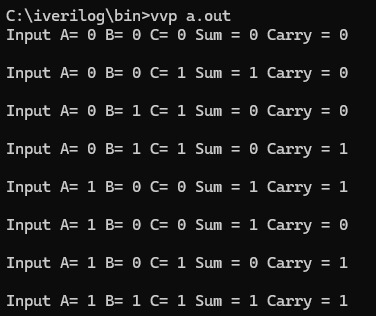




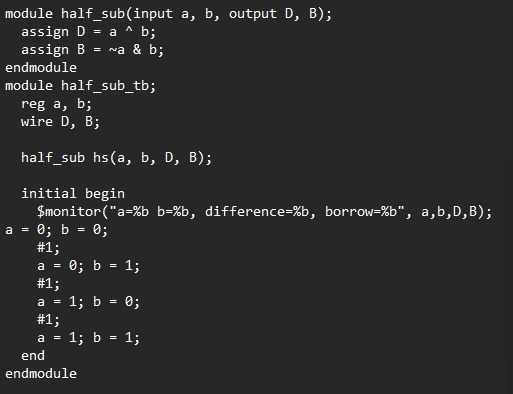
**EXPERIMENT 3**

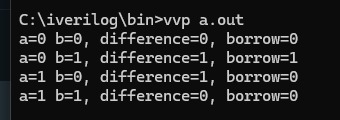
**FULL ADDER**





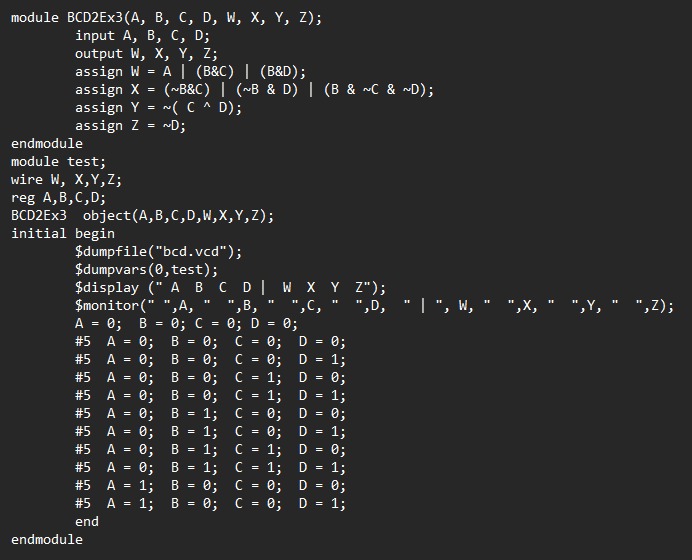
**EXPERIMENT 4**

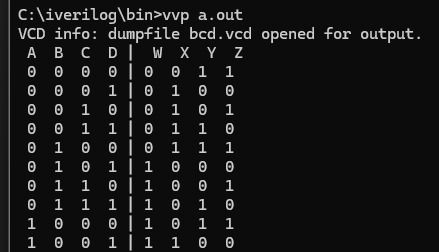
**HALF SUBTRACTOR**



**EXPERIMENT 5**

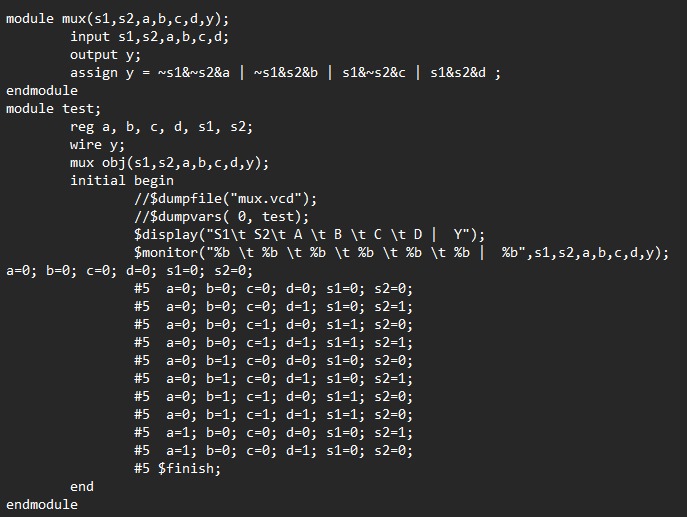
**NUMBER CONVERTER**

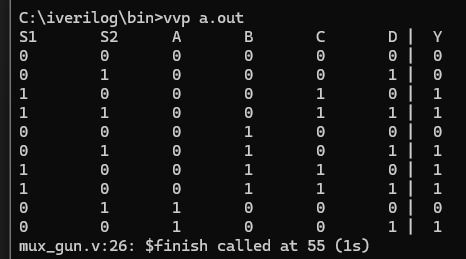




**EXPERIMENT 6**

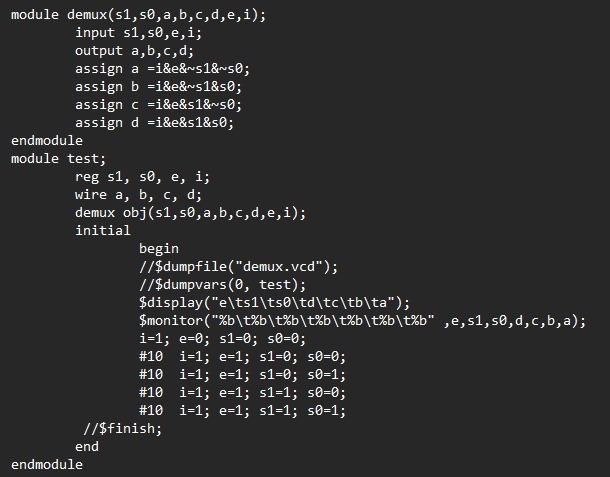
**MULTIPLEXER**

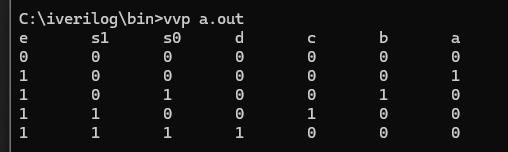




**EXPERIMENT 7**

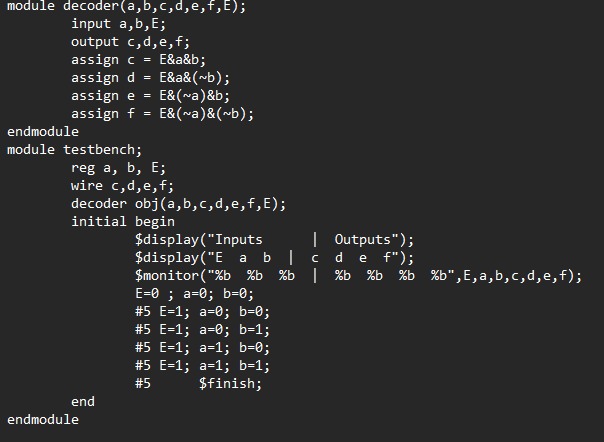
**DEMULTIPLEXER**

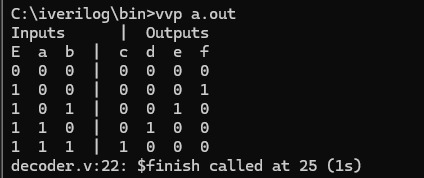




**EXPERIMENT 8**

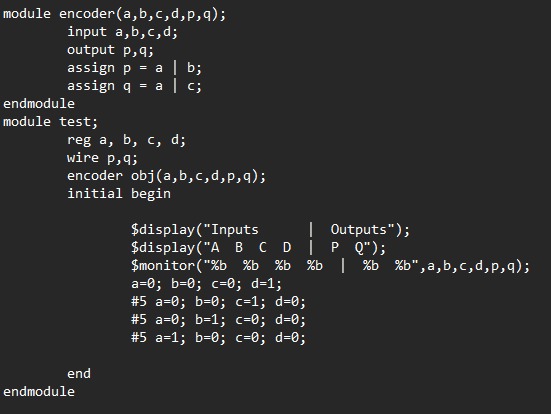
**DECODER**

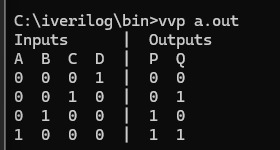




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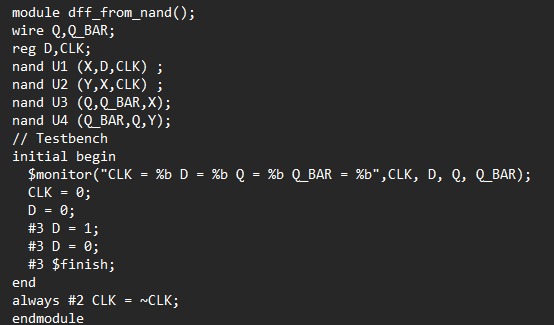
**ENCODER**

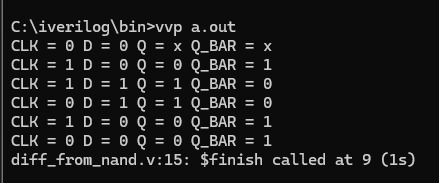




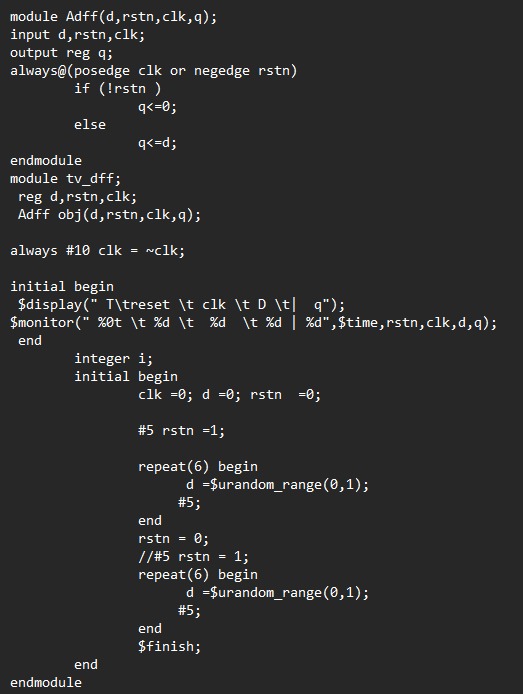
**EXPERIMENT 10**

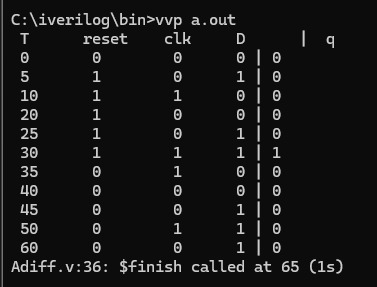
**D FLIP FLOP USING NAND GATE**



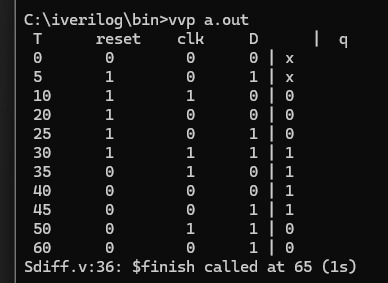
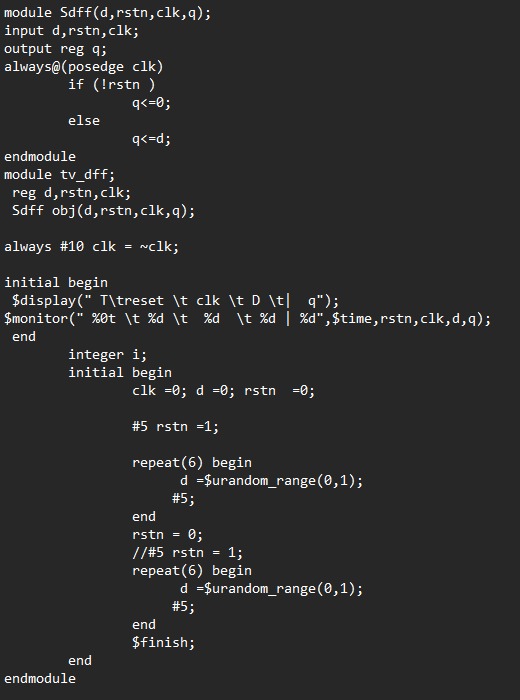


**ASYNCHRONOUS D FLIP FLOP**



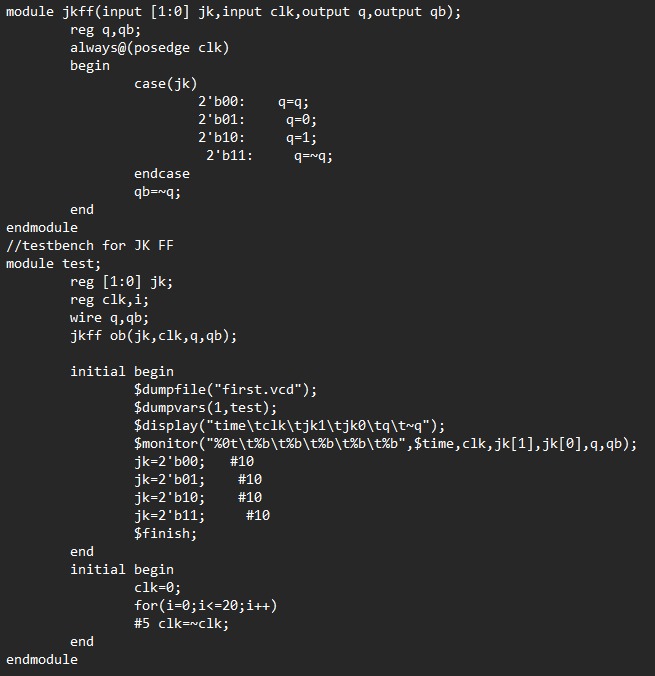


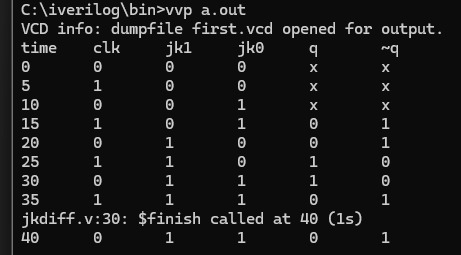
**SYNCHRONOUS D FLIP FLOP**



**EXPERIMENT 11**

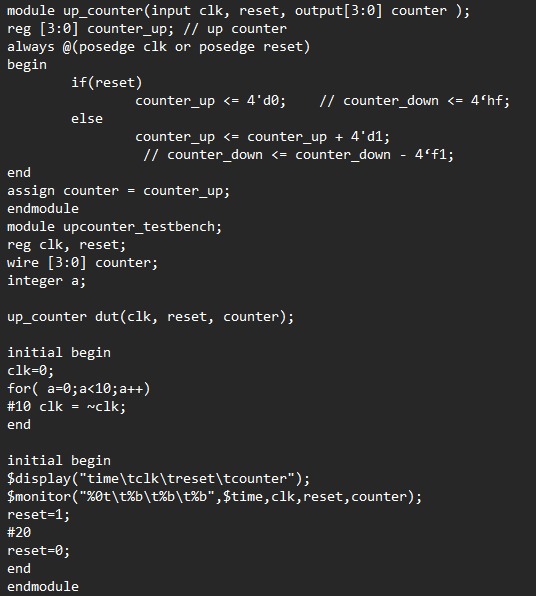
**JK FLIP FLOP**

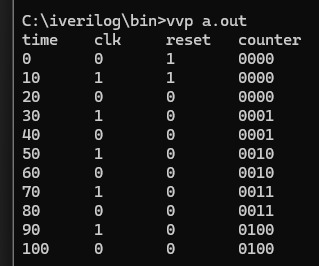




**EXPERIMENT 12**

**UP COUNTER/ DOWN COUNTER**





**UP - DOWN COUNTER**

