INDEX

Exp. No.	Title	Date	Grade	Sign.
1	To plot the forward and reverse characteristics of PN Junction Diode for the given Parameters. Also extract the following parameters : 1) Forward Resistance and Cut-in Voltage from forward characteristics. 2) Reverse resistance from reverse characteristics. 3) Reverse Recovery Time of the Diode (trr).	21/01/2022		
2	Implement RTL inverter using NPN BJT having Bf=20, Rb=10k, Rc=1K. 1. Verify its functionality by performing transient analysis. 2. Plot VTC and calculate noise margin. 3. Find theoretical and practical fan-out and compare them.	28/01/2022		
3	Implement DTL NAND Gate using parameters Bf=50, R1=10k, Rc=1K, R2=20k 1. Perform the static analysis and calculate the Noise Margin. 2. Verify its functionality by performing transient analysis. 3. Find practical fan-out	04/02/2022		
4	Implement Modified diode transister logic (MDTL) using NPN BJT. Bf = 20, R1 = 1.75k, R2 = 2k, R3 = 5k and Rc = 2k 1. Verify its functionality as NAND gate and calculate propagation delay. 2. Plot VTC and Calculate Noise Margin. 3. Compare DTL with MDTL with respect to noise margin, fan-out and propagation delay comment about it.	11/02/2022		
5	Implement TTL inverter using NPN BJT having Bf = 50, Rb = 4kΩ and Rc = 1.6kΩ. 1. Verify its functionality by performing transient analysis.	18/02/2022		

	2. Plot the VTC & Calculate the Noise margin. 3. Find out theoretical and practical fan-out & compare them.			
6	To design and verify the performance of given Resistively Loaded NMOS inverter circuitto obtain VOL = 0.147V for the given specifications: Kn' = 20uA/V, Vt0 = 0.8V, VDD = 5V, W/L = 2um/um. Find the noise margin of the circuit. Also see the effect of change in RL on noise margin andcomment on it.	04/03/2022		
7	Design and verify the performance of given saturated loaded NMOS inverter circuit to obtain Vih-2.9, for the given design parameter VDD=5V, Kn'=20ua/v^2, Vtl-0.8V, Vtl=0.8V, (W/L)driver=2um/1um. a) Compare the theoretical and practical values of the critical voltages on VTC& find noise margins of the circuit. b) observe the effect of change in (W/L) loaded on noise margin &comment on it. c) Also compare the results of noise with resistive loaded NMOS inverter for RL=200k	25/03/2022		
8	Design and verify the performance of given CMOS inverter circuit to obtain switching threshold voltage of 2.2V. Given specifications for the CMOS inverter are: V_{TN} = 0.8V, V_{TP} = -1V, V_{DD} = 5V, K_n' = 20µA/V^2, K_p' = 50µA/V^2, L_n = L_p = 1µm. Compare the theoretical and practical values of critical voltages on VTC and find the noise margin of the circuit. Observe the following parameters and comment on it. 1) Variation of VDD from 5V to 3.3V on the switching threshold voltage of CMOS inverter. 2) Variation of Kr at 0.25, 1 and 4 on the switching characteristics.	01/04/2022		
9	Write a winspice code to verify the functionality of given bicmos inverter circuit using default model parameters for the transistor.	04/04/2022		

10	Design the schematic and verify the functionality of Invertor circuit for CMOS Technology using Microwind Tool. Also Generate the automatic Layout	08/04/2022		
11	Design the schematic and verify the functionality of NAND circuit for CMOS Technology using Microwind Tool. Also Generate the automatic Layout	08/04/2022		
12	Design the schematic and verify the functionality of NOR circuit for CMOS Technology using Microwind Tool. Also Generate the automatic Layout	08/04/2022		

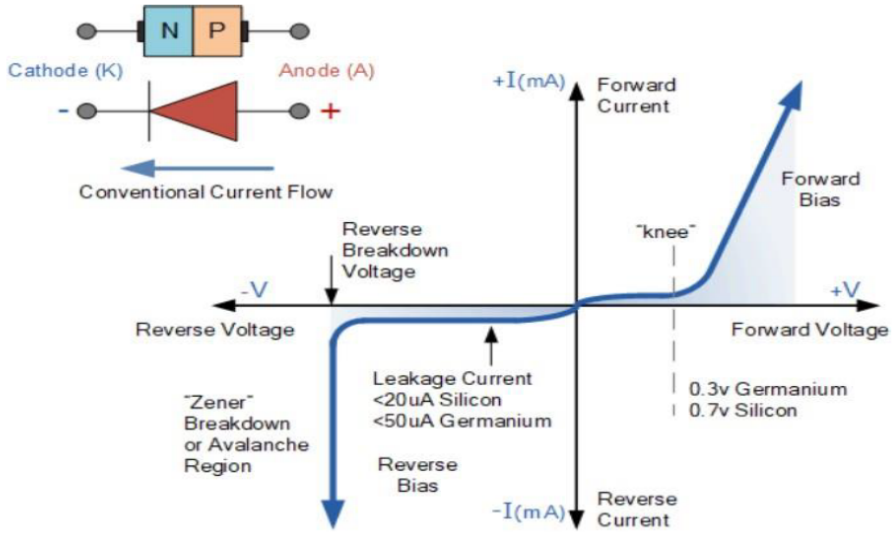
PRACTICAL 1

AIM: To plot the forward and reverse characteristics of PN Junction Diode for the given Parameters. Also extract the following parameters :

1. Forward Resistance and Cut-in Voltage from forward characteristics.
2. Reverse resistance from reverse characteristics.
3. Reverse Recovery Time of the Diode (trr).

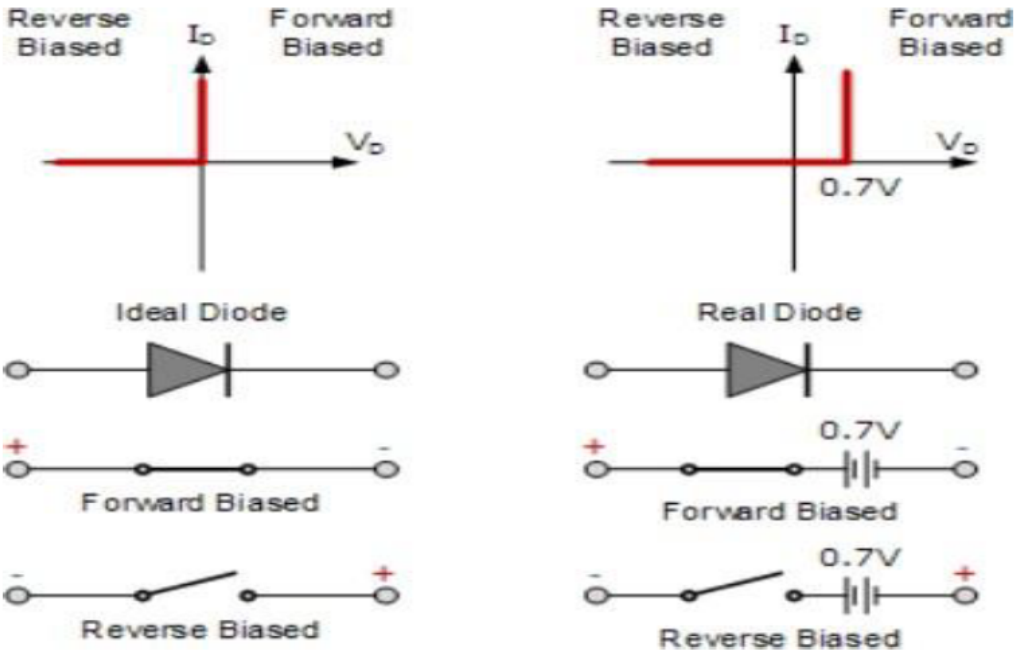
SOFTWARE USED: WinSpice Software

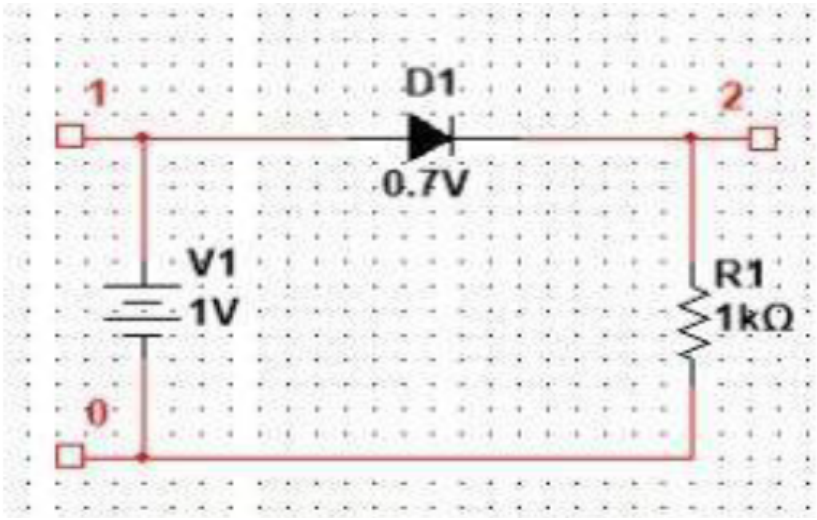
THEORY: A **PN Junction Diode** is one of the simplest semiconductor devices around, and which has the electrical characteristic of passing current through itself in one direction only. However, unlike a resistor, a diode does not behave linearly with respect to the applied voltage. Instead it has an exponential current-voltage (I-V) relationship and therefore we can not describe its operation by simply using an equation such as Ohm's law. If a suitable positive voltage (forward bias) is applied between the two ends of the PN junction, it can supply free electrons and holes with the extra energy they require to cross the junction as the width of the depletion layer around the PN junction is decreased. By applying a negative voltage (reverse bias) results in the free charges being pulled away from the junction resulting in the depletion layer width being increased. This has the effect of increasing or decreasing the effective resistance of the junction itself allowing or blocking the flow of current through the diodes pn-junction. Then the depletion layer widens with an increase in the application of a reverse voltage and narrows with an increase in the application of a forward voltage. This is due to the differences in the electrical properties on the two sides of the PN junction resulting in physical changes taking place. One of the results produces rectification as seen in the PN junction diodes static I-V (current-voltage) characteristics.



There are two operating regions and three possible “biasing” conditions for the standard Junction Diode and these are:

1. **Zero Bias –** No external voltage potential is applied to the PN junction diode.
2. **Reverse Bias –** The voltage potential is connected negative, (-ve) to the P-type material and positive, (+ve) to the N-type material across the diode which has the effect of Increasing the PN junction diode’s width.
3. **Forward Bias –** The voltage potential is connected positive, (+ve) to the P-type material and negative, (-ve) to the N-type material across the diode which has the effect of Decreasing the PN junction diodes width.





WINSPICE CODES:

1. Forward Characteristics

```
*Diode Forward Characteristics

.model mod1 D (IS=1E-12 RS=10 CJ0=5p TT=10N BV=10)

D1 2 0 mod1
R1 1 2 1k
V1 1 0 dc 1

.dc V1 0 5 0.05

.control
run
plot -I(V1)
.endc
.end
```

2. Reverse Characteristics

```
*Diode Reverse Characteristics

.model mod1 D (IS=1E-12 RS=10 CJ0=5p TT=10N BV=10)

D1 2 0 mod1
R1 1 2 1k
V1 1 0 dc 1
```

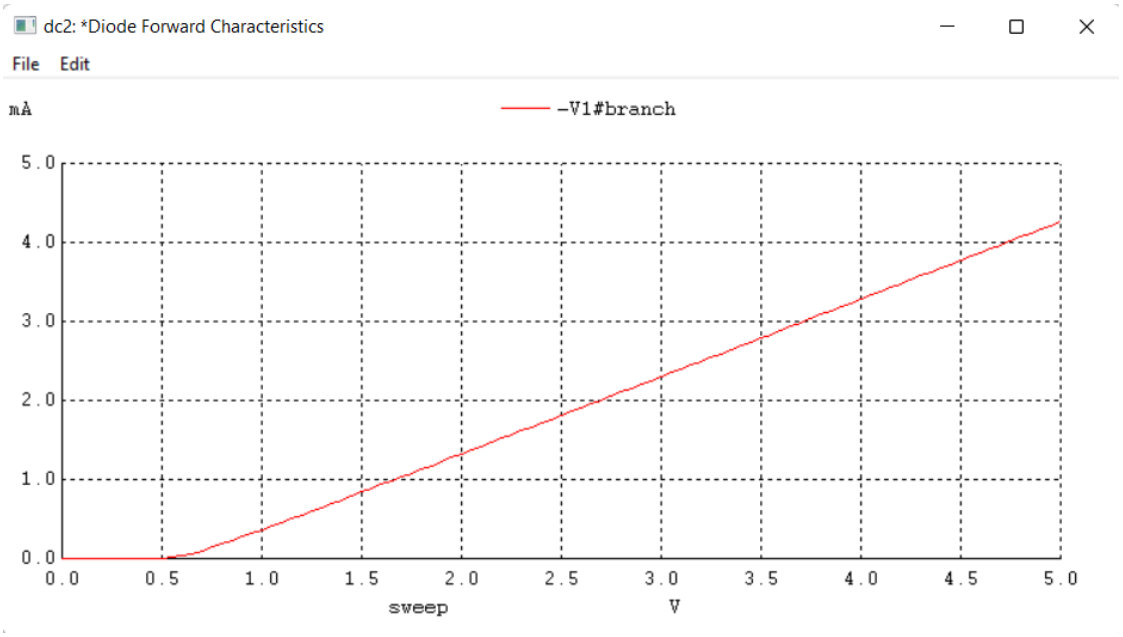
```
.dc V1 -15 0 0.05

.control
run
plot -I(V1)
.endc
.end
```

3. Reverse Recovery Time

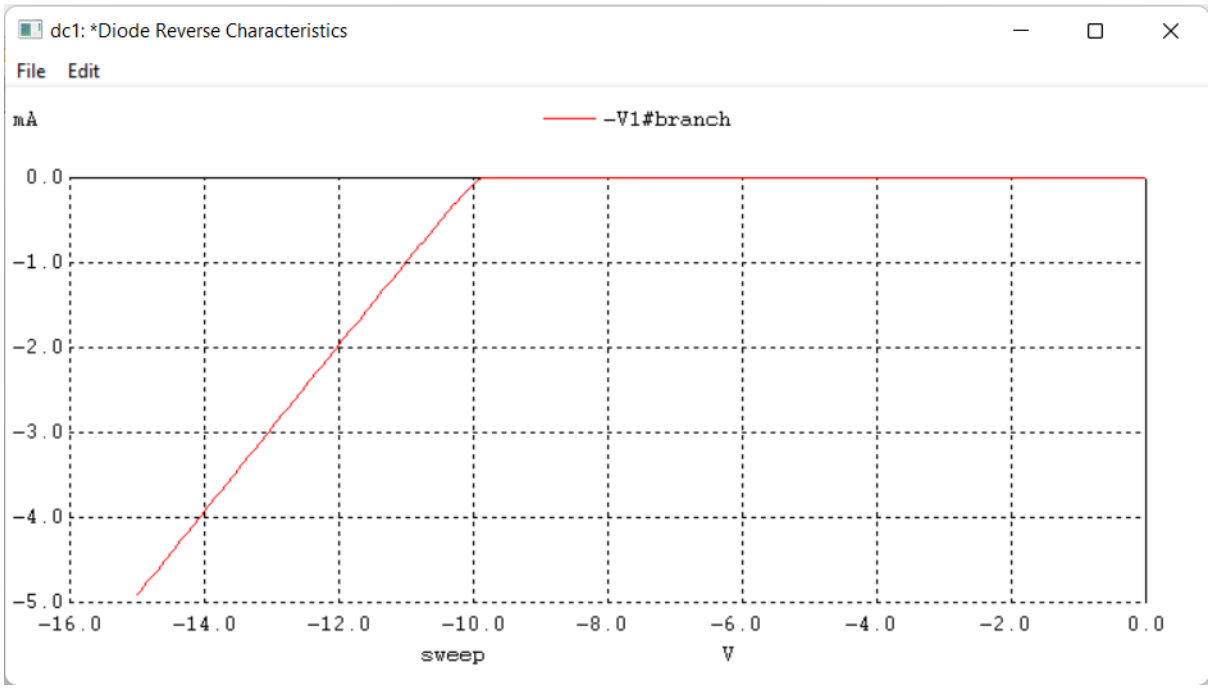
```
* Reverse Recovery Time of Diode

.model mod1 D(IS=1E-12 RS=10 CJO=5p TT=10N BV=10)

V1 1 0 pulse (5 -3 10n 0.05n 0.05n 30n 50n)
RS 1 2 1k
D1 2 3 mod1
Vo 3 0 0

.tran 1n 50n

.control
run
plot v(1) v(2)
plot i(Vo)
.endc
.end
```

OUTPUT:

1. Forward Characteristics

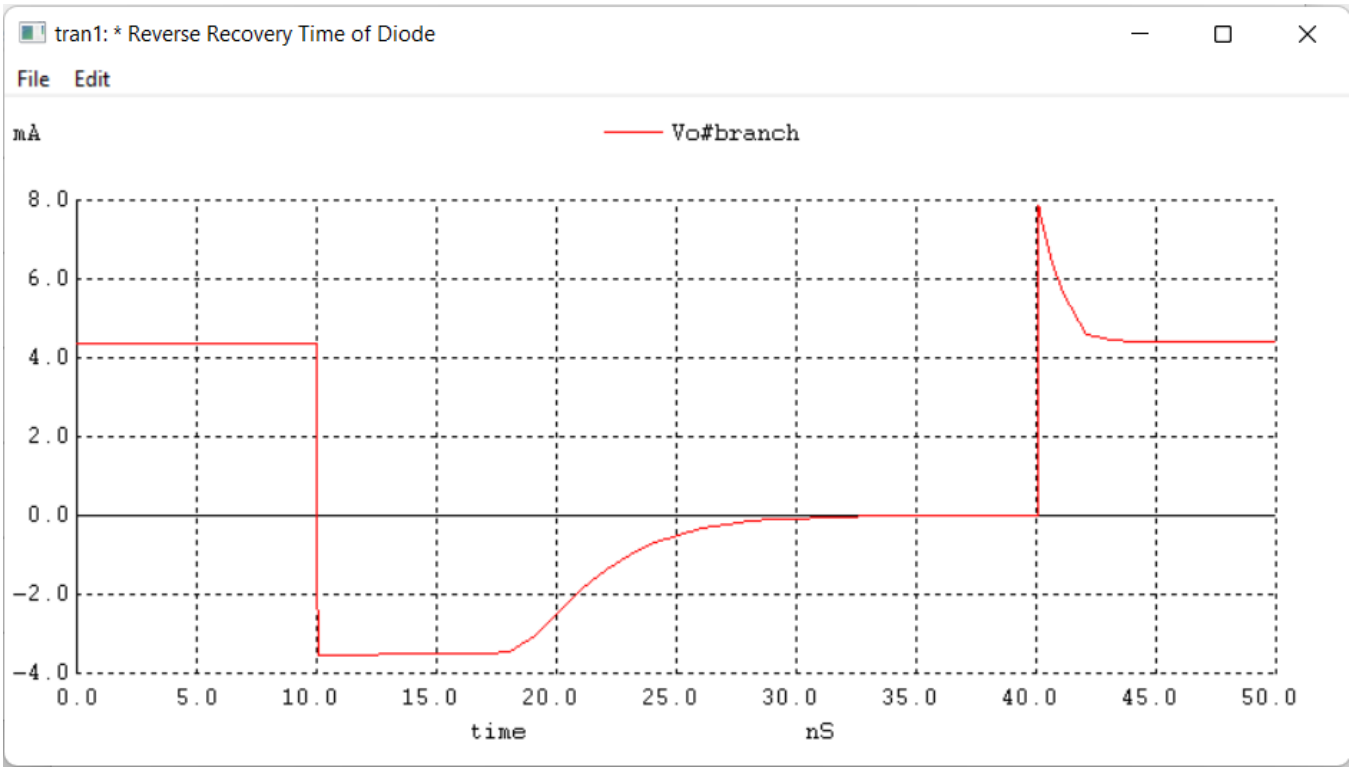


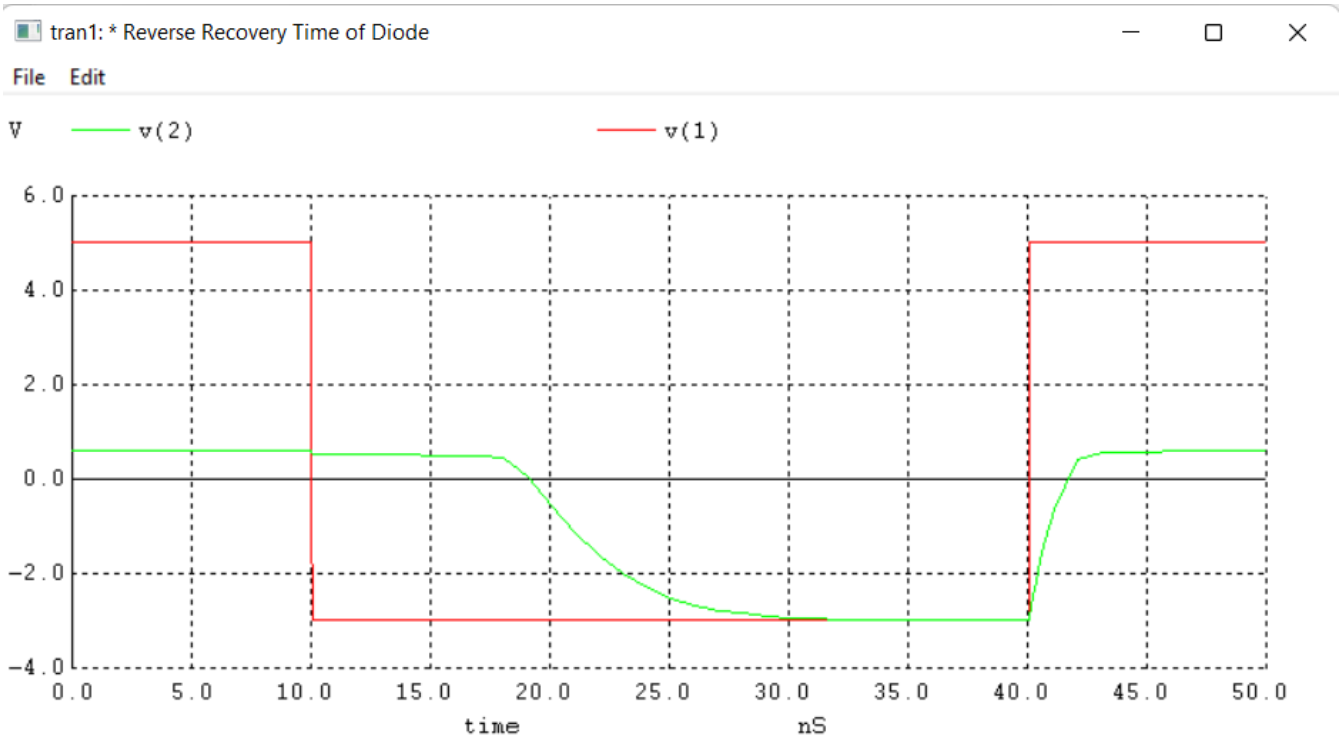
2. Reverse Characteristics



Reverse Resistance = 2V/2mA = 1kΩ

3. Reverse Recovery Time





Trr = 8 ns

CONCLUSION: From the experiment we implemented and observed the transfer characteristics of a Diode in Forward and Reverse mode and calculated their forward resistance and reverse resistance and cut-off voltage in forward mode. We also calculated trr from the Reverse Recovery Time plot.

PRACTICAL 2

AIM: Implement RTL inverter using NPN BJT having Bf = 20, Rb = 10k and Rc = 1k.

1. Verify its functionality by performing transient analysis.
2. Plot the VTC & Calculate the Noise margin.
3. Find out theoretical and practical fan-out & compare them.

SOFTWARE USED: WinSpice Software

THEORY:

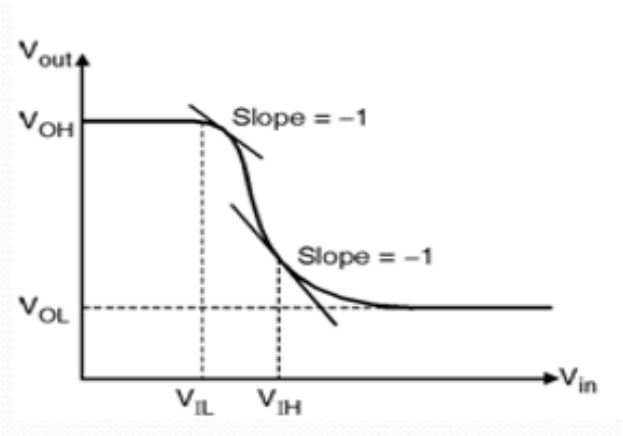
Introduction:

RTL Inverter is a circuit used to invert the input signal. It consists of one BJT transistor, Base connected with resistor (Rb), Collector connected with resistor (Rc) and Emitter is grounded. Input Signal is given to Base of transistor through Rb, Vcc is connected to Rc and Output is taken at collector terminal.

VOLTAGE TRANSFER CHARACTERISTICS (VTC):

To study the noise margins and the fan-out capability of the RTL inverter, we should know the static behaviour of the circuit output Vout when input Vin is increased from 0 to Vcc. When Vin is below the base-emitter cut-in voltage(V_{IL}), collector current is zero and transistor is in the cutoff mode, Vout is almost equal to Vcc (V_{OH}) (assuming no load is connected at output) and VTC will be constant output for 0<Vin<V_{IL}.

As Vin is increased beyond V_{IL}, the transistor enters active mode. The collector current (Ic = βIb) causes a voltage drop in the collector resistor and the collector voltage Vc = Vout = Vcc - IcRc falls. This fall continues until output saturation voltage (Vce=V_{OL}) BJT mode changes to saturation and corresponding input voltage is V_{IH}.



NOISE MARGINS:

Noise margin is the ratio by which the signal exceeds the minimum acceptable amount. It is normally measured in decibels. In a digital circuit, the noise margin is the amount by which the signal exceeds the threshold for a proper '0' or '1'.

$$NM_L = V_{IL} - V_{OL}$$

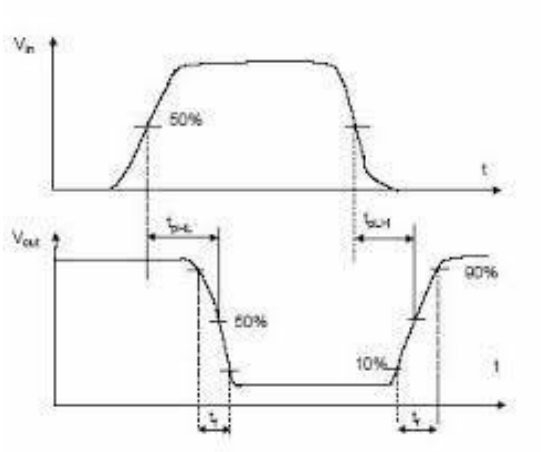
$$NM_H = V_{OH} - V_{IH}$$

In practice, noise margins are the amount of noise, that a logic circuit can withstand. Noise margins are generally defined so that positive values ensure proper operation, and negative margins result in compromised operation, or outright failure.

TRANSIENT RESPONSE:

Transient analysis means analyzing a system in unsteady state. If the variables involved in defining the state of a system does not vary with respect to time, then the system is said to be in steady state.

In Transient Analysis, also called time-domain transient analysis, computes the circuit's response a function of time. This analysis divides the time into segments and calculates the voltage and current levels for each interval.



PROPAGATION DELAY:

Propagation delay is a measure of how long it takes for a gate to change state. Ideally, should be as short as possible.

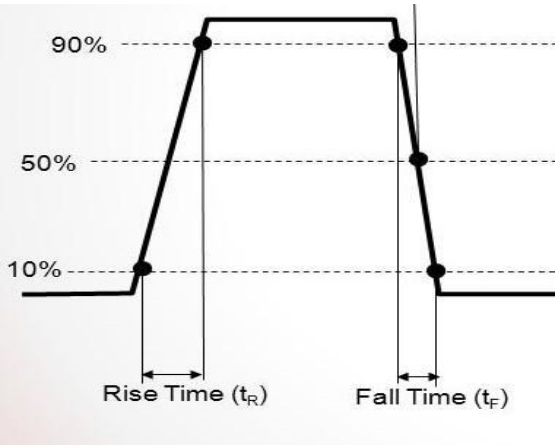
t_{PHL} – the time it takes the output to go from a high to low

t_{PLH} – the time it takes the output to go from a low to high

$$\text{Average Propagation Delay Time } (t_P) = \frac{t_{PHL} + t_{PLH}}{2}$$

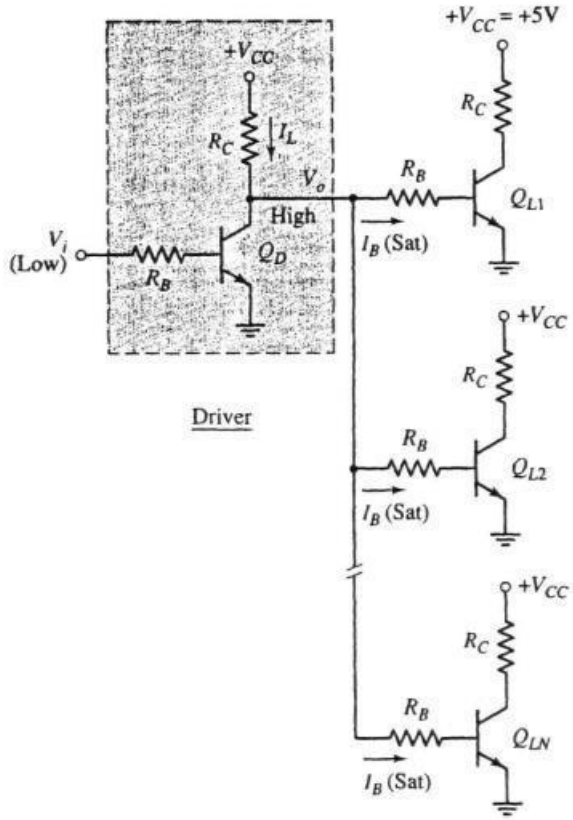
⇨ Rise Time (t_r) = Time from 10% to 90%

⇨ Fall Time (t_f) = Time from 90% to 10%



FAN-OUT:

Fan-out of the inverter is the number of identical circuits that the inverter can drive before Vo enters the transition region. When output of RTL inverter (the driver) is at logic low, it can drive practically any number of identical inverters (loads). Since, each load transistor is operating in the cutoff mode, no current is drawn via the collector resistor of the driver, and the output voltage remains at logic low.



For logic high output of the driver as shown in above figure there are N identical inverters connected to output of driver circuit. Since, the saturation base current of each load inverter is supplied by the driver, output voltage Vo drops from its open circuit voltage of Vcc. The gate fan-out therefore it is limited by the number of load inverters that can be driven into saturation while maintain satisfactory logic high Vo ≥ V_{IH}. The number depends on the current gain β of the driver transistor

From above figure, the sum of the base currents of the load gates, which is the current through the collector resistor of the driver, is given by

$$I_L = N*Ib(sat) = N*k*Ib(EOS)$$

Where overdrive factor k is defined by

$$k=Ib(sat)/Ib(EOS)$$

$$Ib(EOS) = Ic(EOS)/\beta = (Vcc - V_{CE(sat)})/\beta R_C$$

$$Vo = Vcc – (N*k*Ib(EOS)* R_C)$$

$$= Vcc – (N*k*(Vcc - V_{CE(sat)})/\beta)$$

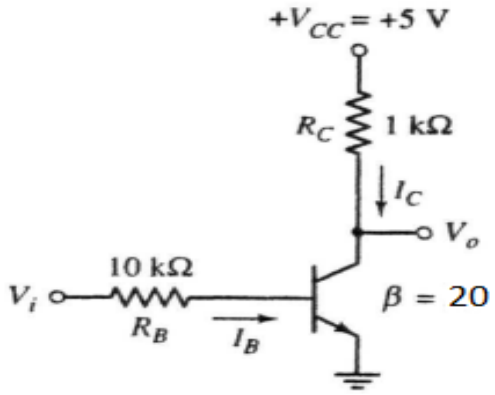
For regeneration of logic levels at the load gates, this voltage Vo must satisfy the input logic high level. Hence

$$Vcc – (N*k*(Vcc - V_{CE(sat)})/\beta) \geq V_{IH}$$

$$N \leq \frac{\beta\left[V_{cc} - V_{IH}\right]}{k\left[V_{cc} - V_{CE(sat)}\right]}$$

Circuit Diagram:

RTL inverter using NPN BJT



Working principle:

Bipolar transistor switch is the simplest RTL gate. The resistor R1 in the circuit is used across the base and input terminals. This resistor increases the voltage drop from 0.7 V to 1 V by converting the input voltage into current. The resistance Rb is chosen in such a way that it saturates the transistor and obtains high input resistance. The collector resistor Rc converts collector current into voltage. The resistance of R2 is high to saturate the transistor and low to obtain output resistance.

Application:

The RTL circuit consists of resistors at inputs and transistors at the output side. Transistors are used as the switching device.

WINSPICE CODES:

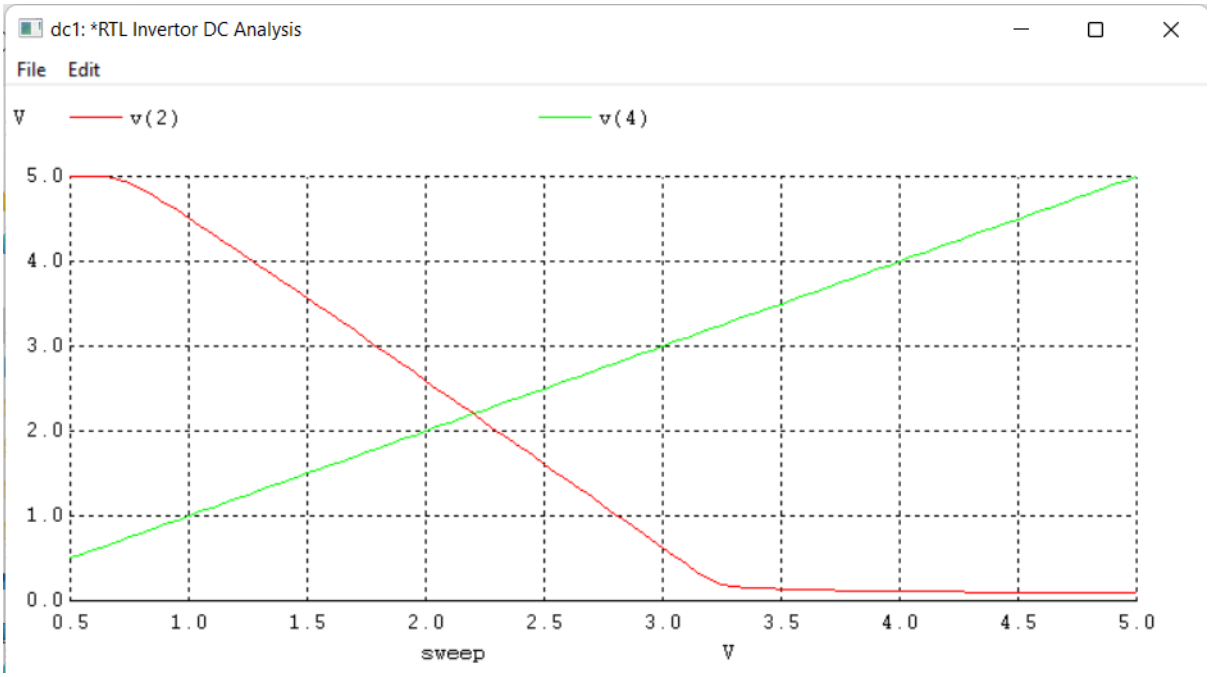
```
*RTL Invertor DC Analysis


.model myBJT NPN (BF = 20)


Q 2 1 0 myBJT

Rc 2 3 1k

Rb 4 1 10k

Vcc 3 0 5

Vin 4 0 5
```

```
.dc Vin 0.5 5 0.05

.control
run
plot v(2) v(4)
.endc
.end

*RTL Invertor Transient Analysis

.model myBJT NPN (BF = 20)

Q 2 1 0 myBJT
Rc 2 3 1k
Rb 4 1 10k
Vcc 3 0 5
Vin 4 0 pulse (0 5 1ns 1ns 1ns 100ns 200ns)
c 2 0 1p

.tran 1ns 400ns

.control
run
plot v(4) v(2)
.endc
.end

*RTL Invertor Fanout

.model myBJT NPN (BF = 20)
```

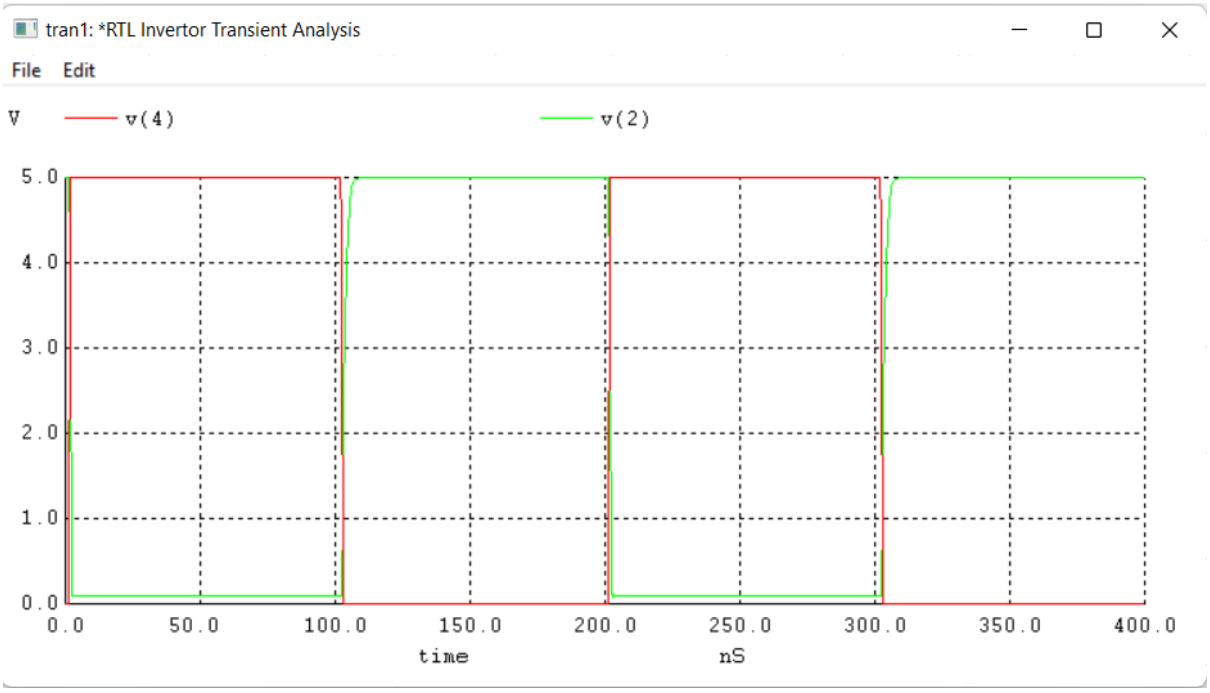
```
Q 2 1 0 myBJT
Rc 2 3 1k
Rb 4 1 10k
Vcc 3 0 5
Vin 4 0 5

.subckt RTL in c out 0
Q y z 0 myBJT
Rc y c 1k
Rb in z 10k
.ends RTL

x1 2 3 out1 0 RTL
x2 2 3 out2 0 RTL
x3 2 3 out3 0 RTL
x4 2 3 out4 0 RTL
x5 2 3 out5 0 RTL
x6 2 3 out6 0 RTL
x7 2 3 out7 0 RTL

.dc Vin 0.5 5 0.05

.control
run
plot v(2) v(4)
.endc
.end
```

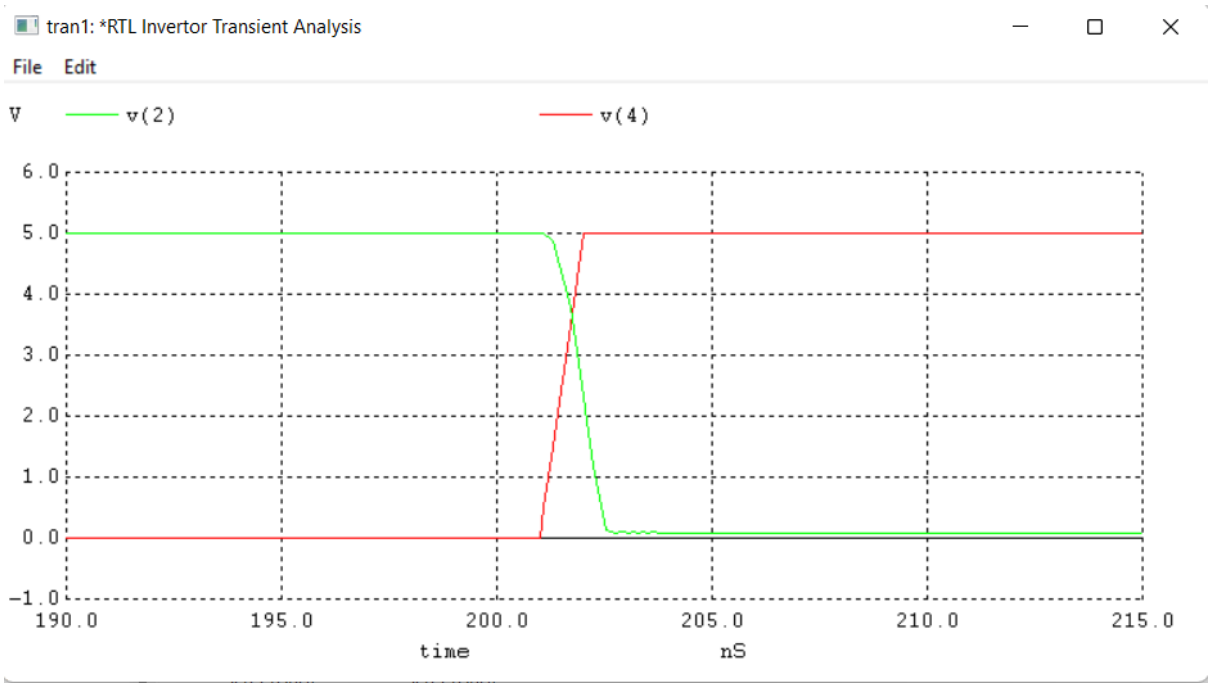
OUTPUT:

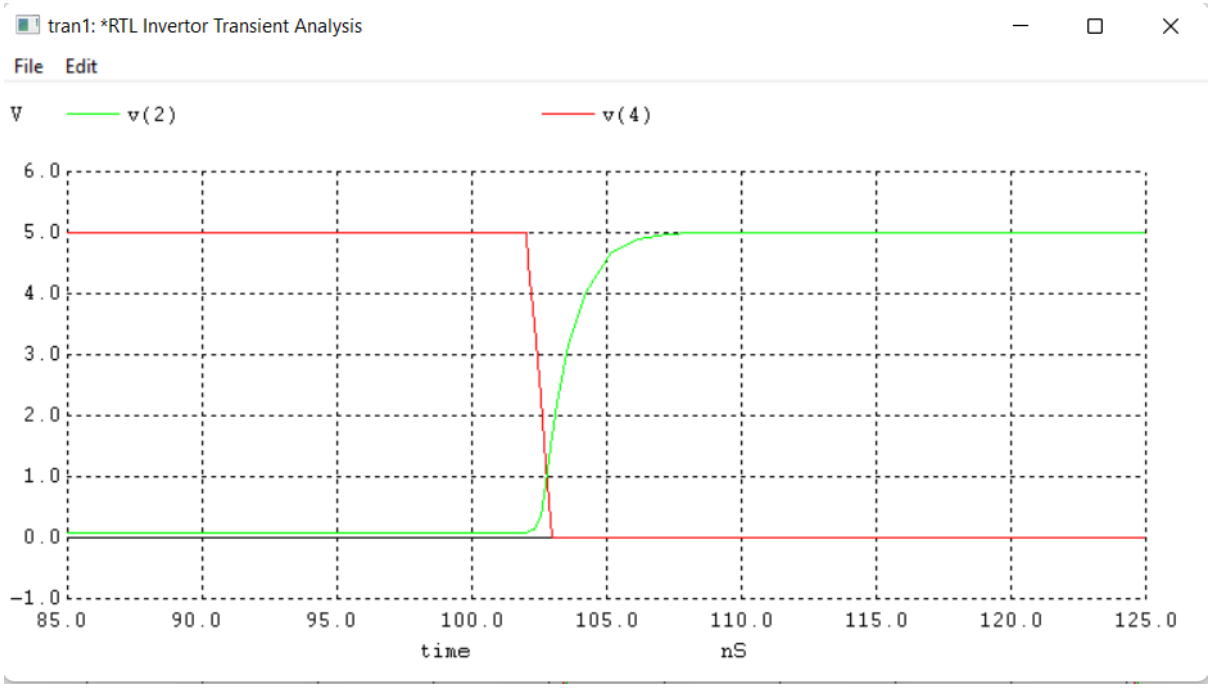
1. RTL Invertor DC Analysis



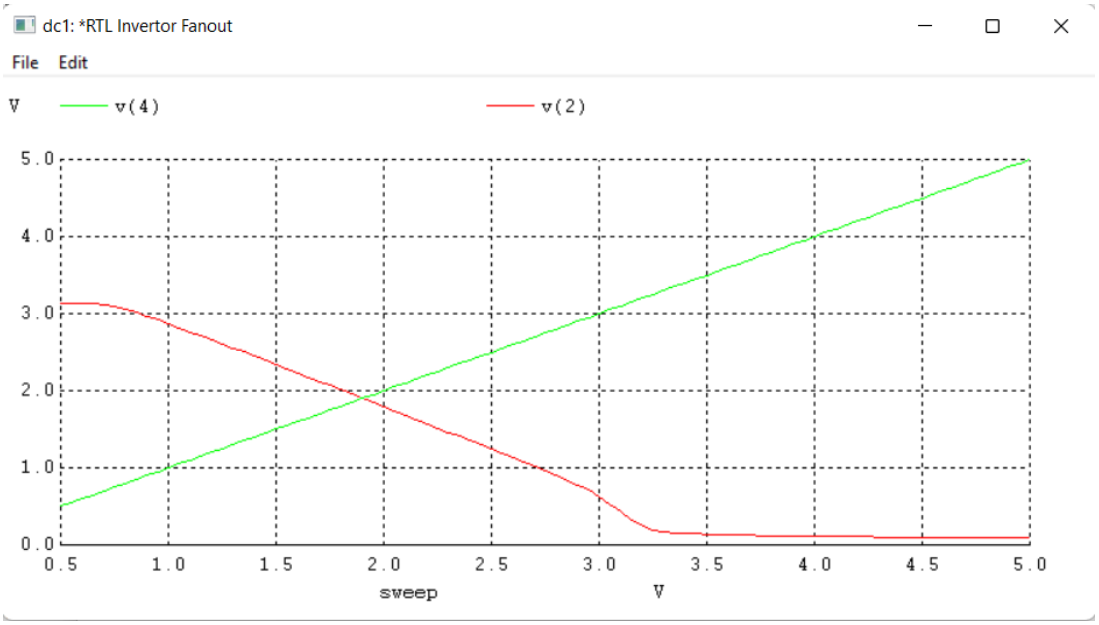
2. RTL Invertor Transient Analysis




tran1: *RTL Invertor Transient Analysis
File Edit
V
v(2)
v(4)
6.0
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
190.0
195.0
200.0
205.0
210.0
215.0
time
nS


tran1: *RTL Invertor Transient Analysis
File Edit
V
v(2)
v(4)
6.0
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
85.0
90.0
95.0
100.0
105.0
110.0
115.0
120.0
125.0
time
nS

3. RTL Invertor Fanout



THEORETICAL AND PRACTICAL CALCULATION:

1. DC Analysis
   V_{OH} = 5V, V_{IL} = 0.65V, V_{OL} = 0.25V and V_{IH} = 3.2
   $NM_H = V_{OH} - V_{IH} = 5 - 3.2 = 1.8V$
   $NM_L = V_{IL} - V_{OL} = 0.65 - 0.25 = 0.4V$
   $NM(overall) = \min(NM_H, NM_L) = 0.4V$

2. Transient Analysis
   τ_{PHL} = 0.785ns, τ_{PLH} = 0.464ns T_r = 2.33ns T_f = 0.9825ns

3. Fanout
   Practical = 7
   Theoretical = 7

$$N \leq \frac{20[5-3.2]}{[5-0.2]} = 7.5$$

CONCLUSION: From the experiment we implemented and observed RTL Invertor and calculated its various parameters from DC Analysis and Transient Analysis. We also calculated its Fanout from the practical as well as from the theoretical values which are exactly the same and hence verifying the practical value.

PRACTICAL 3

AIM: Implement DTL NAND Gate using NPN BJT.

1. Plot VTC and Calculate Noise Margin.
2. Verify its functionality by performing transient analysis.
3. Find theoretical and practical Fan Out and compare them.

SOFTWARE USED: WinSpice Software

THEORY:

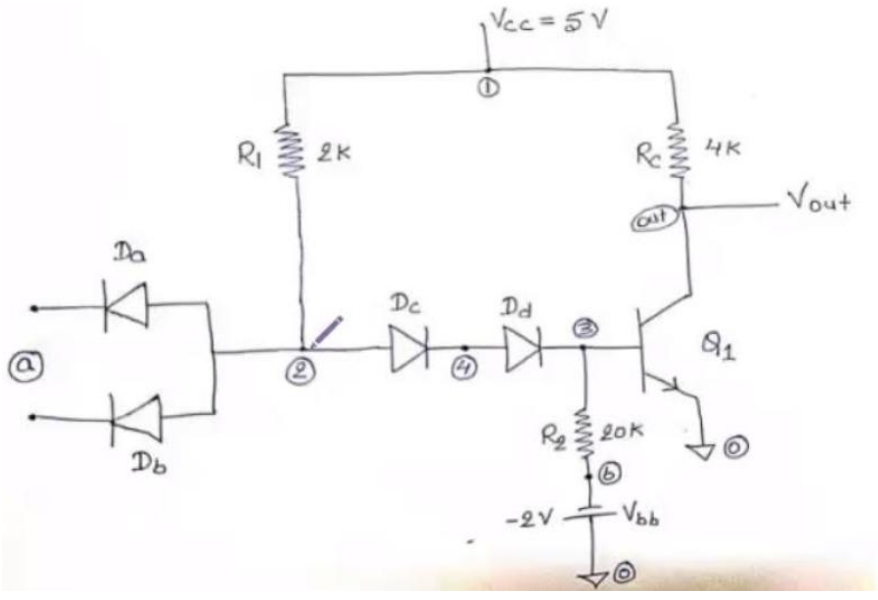
Introduction:

Diode-Transistor Logic, or DTL, refers to the technology for designing and fabricating digital circuits wherein logic gates employ both diodes and transistors. DTL offers better noise margins and greater fan-outs than RTL, but suffers from low speed, especially in comparison to TTL.

RTL allows the construction of NOR gates easily, but NAND gates are relatively more difficult to get from RTL. DTL, however, allows the construction of simple NAND gates from a single transistor, with the help of several diodes and resistors.

Below figure shows an example of an 2-input DTL NAND gate. It consists of a single transistor Q configured as an inverter, which is driven by a current that depends on the inputs to the three input diodes D1 and D2.

Circuit Diagram:



Working principle

In the NAND gate in Figure, the current through diodes DA and DB will only be large enough to drive the transistor into saturation and bring the output voltage Vo to logic '0' if all the input diodes D1 qne D3 are 'off', which is true when the inputs to all of them are logic '1'. This is because when D1-D3 are not conducting, all the current from Vcc through R will go through DA and DB and into the base of the transistor, turning it on and pulling Vo to near ground.

However, if any of the diodes D1 and D2 gets an input voltage of logic '0', it gets forward-biased and starts conducting. This conducting diode 'shunts' almost all the current away from the reverse-biased DA and DB, limiting the transistor base current. This forces the transistor to turn off, bringing up the output voltage Vo to logic '1'.

Application:

One advantage of DTL over RTL is its better noise margin. The noise margin of a logic gate for logic level '0', $\Delta 0$, is defined as the difference between the maximum input voltage that it will recognize as a '0' (Vil) and the maximum voltage that may be applied to it as a '0' (Vol of the driving gate connected to it). For logic level '1', the noise margin $\Delta 1$ is the difference between the minimum input voltage that may be applied to it as a '1' (Voh of the driving gate connected to it) and the minimum input voltage that it will recognize as a '1' (Vih).

WINSPICE CODES:

```
*DTL DC Analysis

.model myBJT NPN ( BF = 50 )
.model Y D

Q out 3 0 myBJT

Da 2 a Y
Db 2 a Y
Dc 2 4 Y
Dd 4 3 Y
```

```
R1 1 2 2k
R2 3 b 20k
Rc 1 out 4k

Vbb b 0 -2
Vcc 1 0 5

Va a 0 5

.dc Va 0.5 5 0.05

.control
run
plot V(a) V(out)
.endc
.end


*DTL Transient Analysis

.model myBJT NPN (BF = 50)
.model Y D

Q out 3 0 myBJT

Da 2 a Y
Db 2 a Y
Dc 2 4 Y
Dd 4 3 Y
```

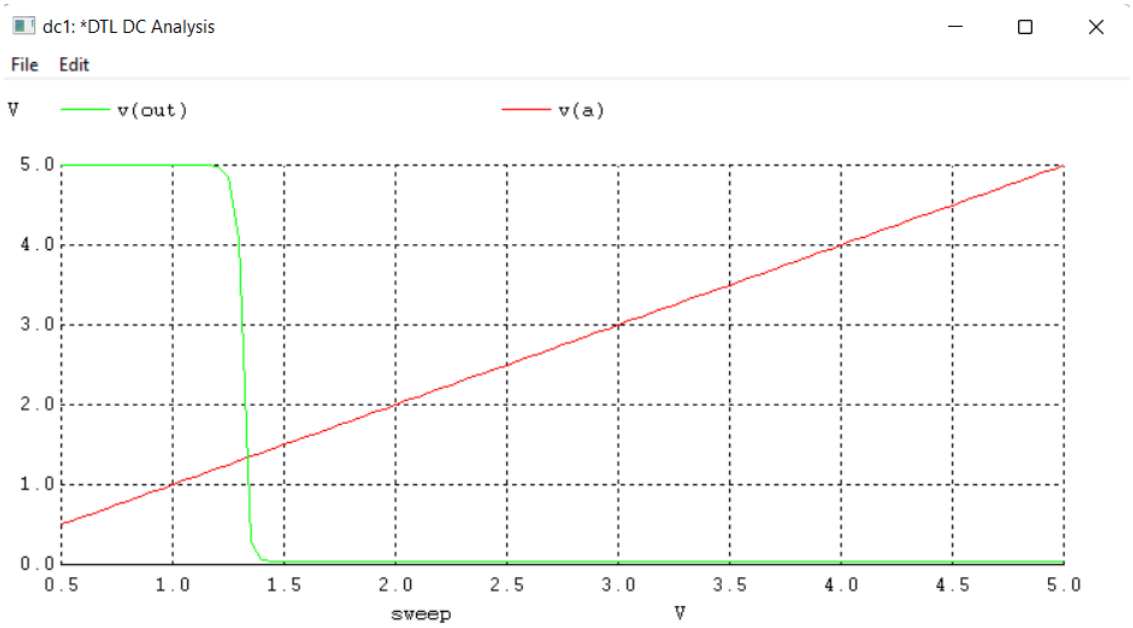
```
R1 1 2 2k
R2 3 b 20k
Rc 1 out 4k
C1 out 0 0.1p

Vbb b 0 -2
Vcc 1 0 5

Va a 0 pulse (0 5 1ns 1ns 1ns 100ns 200ns)

.tran 1ns 400ns

.control
run
plot v(a) v(out)
.endc
.end

*DTL Fanout
.model q1 npn bf=50
.model d1 d

.subckt dtlckt a b c 1 0 out
q1 out 4 0 q1
da 2 a d1
db 2 b d1
dc 2 3 d1
dd 3 4 d1
r1 2 1 2k
```

```
rc 1 out 4k
r2 4 c 20k
.ends dtlckt
*supply
vcc 1 0 5
vbb c 0 -2
Va a 0 5
*driver gate
Xd a a c 1 0 out1 dtlckt
*Load gates
XL1 out1 out1 c 1 0 out2 dtlckt
XL2 out1 out1 c 1 0 out3 dtlckt
XL3 out1 out1 c 1 0 out4 dtlckt
XL4 out1 out1 c 1 0 out5 dtlckt
XL5 out1 out1 c 1 0 out6 dtlckt
XL6 out1 out1 c 1 0 out7 dtlckt
XL7 out1 out1 c 1 0 out8 dtlckt
XL8 out1 out1 c 1 0 out9 dtlckt
XL9 out1 out1 c 1 0 out10 dtlckt
XL10 out1 out1 c 1 0 out11 dtlckt
XL11 out1 out1 c 1 0 out12 dtlckt
XL12 out1 out1 c 1 0 out13 dtlckt
XL13 out1 out1 c 1 0 out14 dtlckt
XL14 out1 out1 c 1 0 out15 dtlckt
XL15 out1 out1 c 1 0 out16 dtlckt
XL16 out1 out1 c 1 0 out17 dtlckt
XL17 out1 out1 c 1 0 out18 dtlckt
XL18 out1 out1 c 1 0 out19 dtlckt
XL19 out1 out1 c 1 0 out20 dtlckt
XL20 out1 out1 c 1 0 out21 dtlckt
```

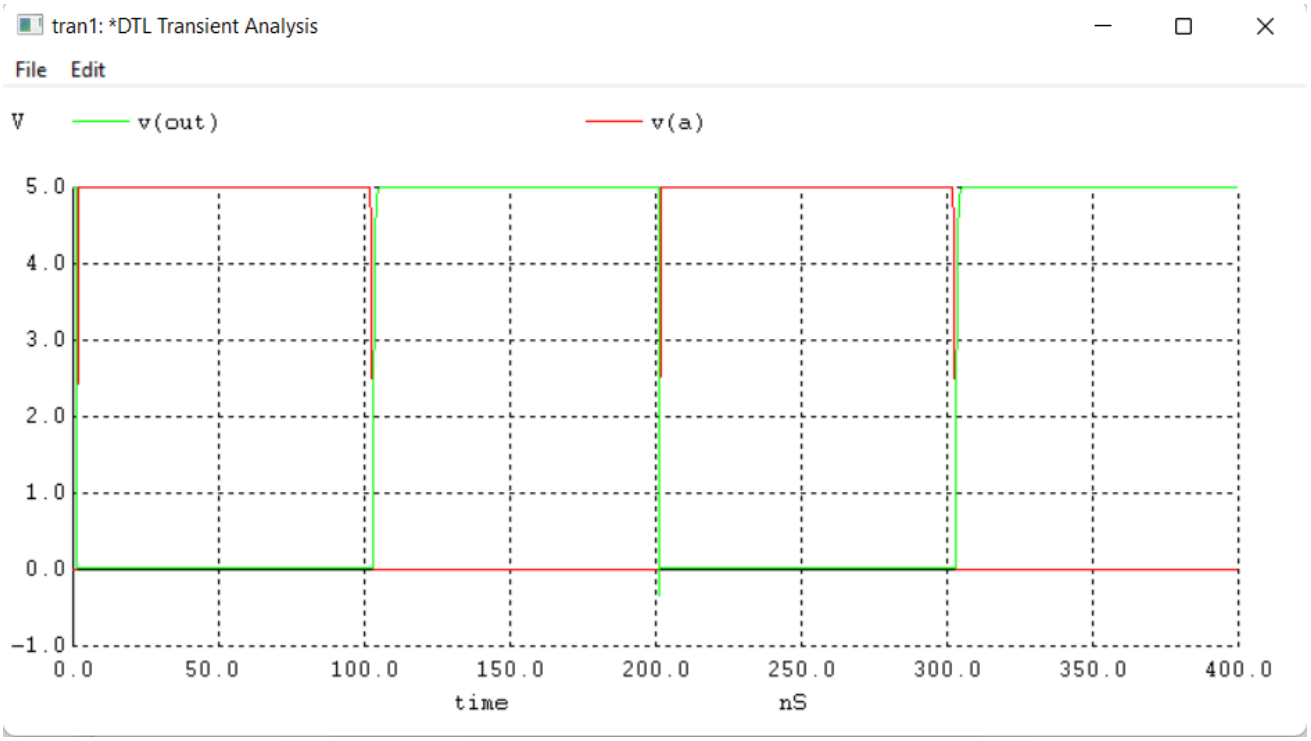
```
XL21 out1 out1 c 1 0 out22 dtlckt
XL22 out1 out1 c 1 0 out23 dtlckt
XL23 out1 out1 c 1 0 out24 dtlckt
XL24 out1 out1 c 1 0 out25 dtlckt
XL25 out1 out1 c 1 0 out26 dtlckt
XL26 out1 out1 c 1 0 out27 dtlckt
XL27 out1 out1 c 1 0 out28 dtlckt
XL28 out1 out1 c 1 0 out29 dtlckt
XL29 out1 out1 c 1 0 out30 dtlckt
XL30 out1 out1 c 1 0 out31 dtlckt
XL31 out1 out1 c 1 0 out32 dtlckt
XL32 out1 out1 c 1 0 out33 dtlckt
XL33 out1 out1 c 1 0 out34 dtlckt
XL34 out1 out1 c 1 0 out35 dtlckt
XL35 out1 out1 c 1 0 out36 dtlckt
XL36 out1 out1 c 1 0 out37 dtlckt
XL37 out1 out1 c 1 0 out38 dtlckt
XL38 out1 out1 c 1 0 out39 dtlckt
XL39 out1 out1 c 1 0 out40 dtlckt
XL40 out1 out1 c 1 0 out41 dtlckt
XL41 out1 out1 c 1 0 out42 dtlckt
XL42 out1 out1 c 1 0 out43 dtlckt
.dc Va 0.5 5 0.05
.control
run
plot I(Vout1) I(4)
.endc
.end
```

OUTPUT:

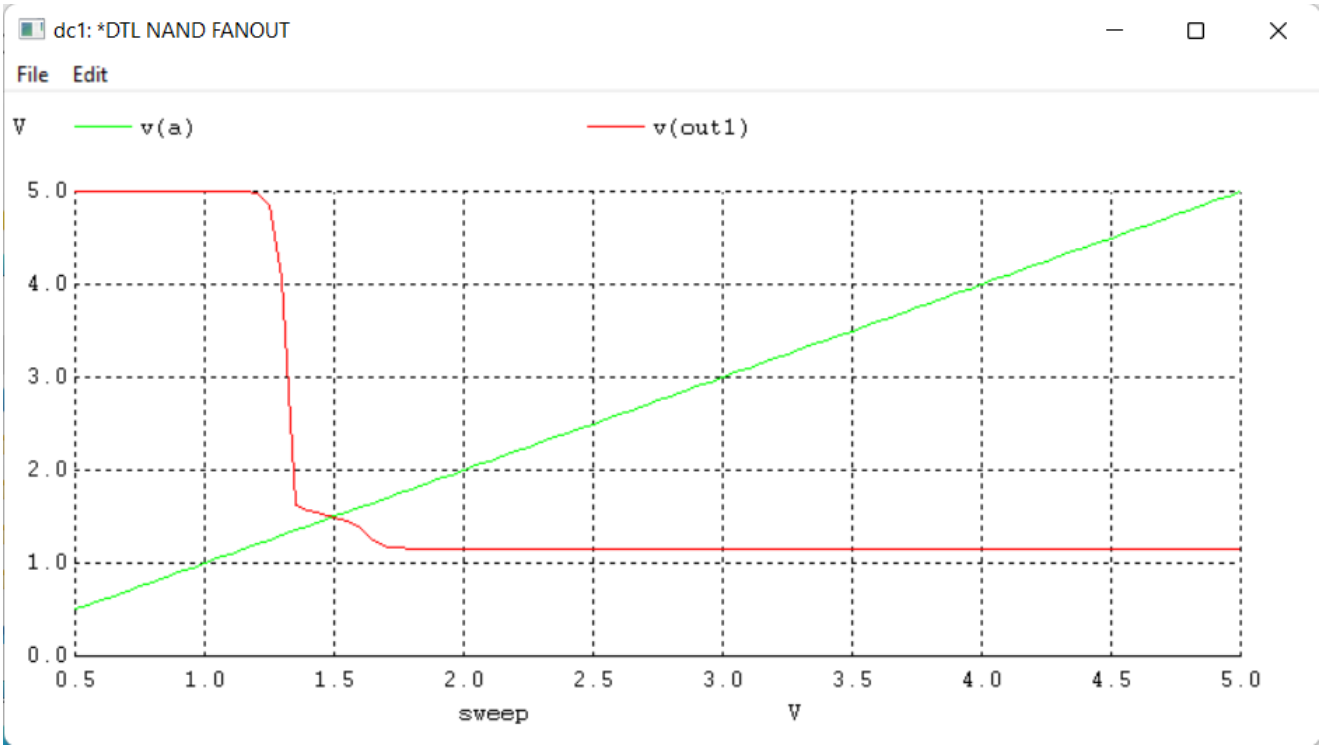
1. DTL NAND DC Analysis



2. DTL NAND Transient Analysis



3. DTL NAND Fanout



THEORETICAL AND PRACTICAL CALCULATION:

1. DC Analysis
   V_{OH} = 5V, V_{IL} = 1.2V, V_{OL} = 0.275V and V_{IH} = 1.35
   $NM_H = V_{OH} - V_{IH} = 5 – 1.35 = 3.65V$
   $NM_L = V_{IL} - V_{OL} = 1.2 – 0.275 = 0.925V$
   $NM(overall) = \min(NM_H, NM_L) = 0.925V$

2. Transient Analysis
   T_{PHL} = 0.186ns, T_{PLH} = 0.65ns T_r = 1ns T_f = 0.14ns

3. Fanout
   Practical = 42
   Theoretical = 42

CONCLUSION: From the experiment we implemented and observed DTL NAND Gate and calculated its various parameters from DC Analysis and Transient Analysis. We also calculated its Fanout from the practical as well as from the theoretical values which are exactly the same and hence verifying the practical value.

PRACTICAL 4

AIM: Implement Modified diode transister logic (MDTL) using NPN BJT. Bf = 20, R1 = 1.75k, R2 = 2k, R3 = 5k and Rc = 2k.

1. Verify its functionality as NAND gate and calculate propagation delay.
2. Plot VTC and Calculate Noise Margin.
3. Compare DTL with MDTL with respect to noise margin, fan-out and propagation delay comment about it.

SOFTWARE USED: WinSpice Software

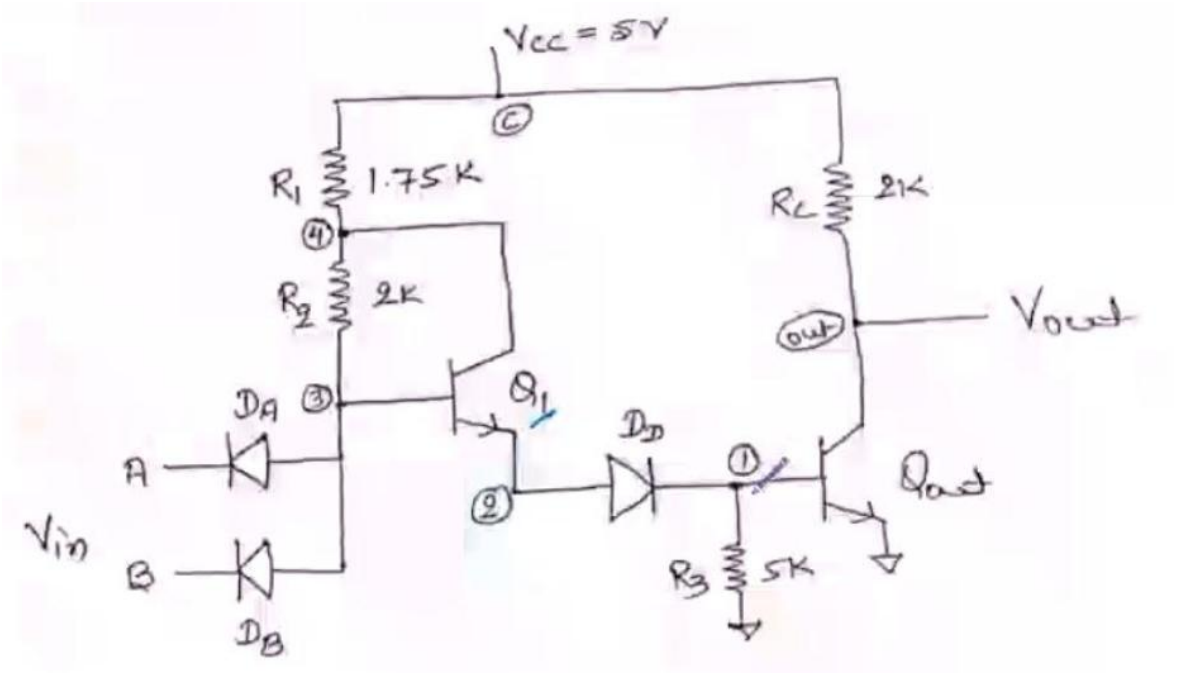
THEORY:

Introduction:

The diode-transistor logic, also termed as DTL, replaced RTL family because of greater fan-out capability and more noise margin. As its name suggests, DTL circuits mainly consists of diodes and transistors that comprises DTL devices.

Due to number of diodes used in this circuit, the speed of the circuit is significantly low. Hence this family of logic gates is modified to transistor-transistor logic i.e. TTL family.

Circuit Diagram:



Working principle:

The fan out of IC positive DTL NAND gate of may be increased by replacing the diode by a transistor Q1 as shown in figure 6. Thus, transistor Q1 while conducting is in its active region and not in saturation. This results from the fact that the current through resistor R1(1.75 K-OHMs) is in a direction to reverse bias the collector junction of NPN transistor Q1. Further the emitter current of Q1 provides the base current IB2 of Q_{out}. Hence Q_{out} is driven by a much larger base current I_B. Hence, for the same value of h_{FE},the collector current of Q_{out} is much larger permitting much greater fan out.

Application:

It is used in the applications where noise margin, fan Out requirements are high, and Propagation delay is low.

WINSPICE CODES:

```
*MDTL DC Analysis

.model myBJT NPN ( BF = 20 )
.model Y D

Q1 4 3 2 myBJT
Q2 out 1 0 myBJT

Da 3 a Y
Db 3 b Y
Dd 2 1 Y

R1 c 4 1.75k
R2 4 3 2k
R3 1 0 5k
Rc c out 2k
```

```
Vcc c 0 5

Va a 0 5

.dc Va 0.5 5 0.05

.control
run
plot V(a) V(out)
.endc
.end

*MDTL Transient Analysis

.model myBJT NPN ( BF = 20 )
.model Y D

Q1 4 3 2 myBJT
Q2 out 1 0 myBJT

Da 3 a Y
Db 3 b Y
Dd 2 1 Y

R1 c 4 1.75k
R2 4 3 2k
R3 1 0 5k
Rc c out 2k
C1 out 0 0.1p
```

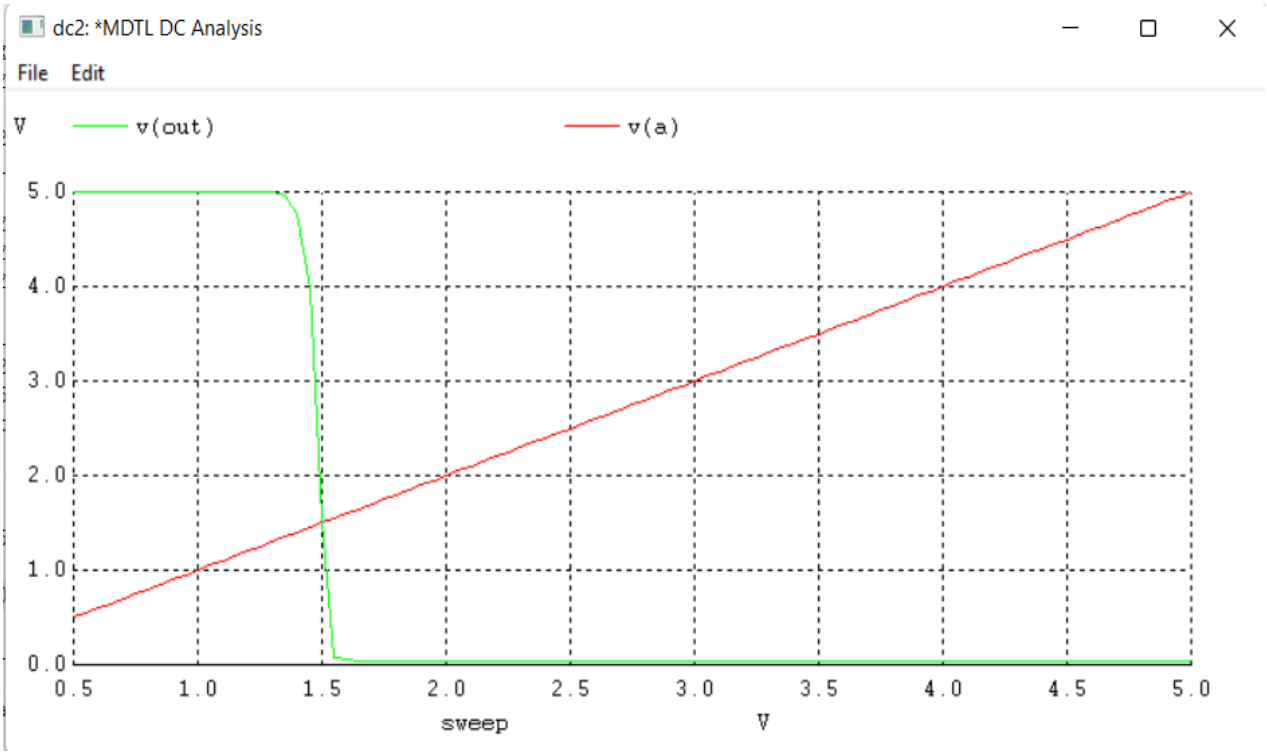
```
Vcc c 0 5

Va a 0 pulse (0 5 0ps 10ps 10ps 200ps 1000ps)

.tran 10ps 2000ps

.control
run
plot V(a) V(out)
.endc
.end

*MDTL Fanout

.model mybjt npn (Bf = 20)
.model mydiode d

.subckt modifiedDTL in1 in2 vccNode gnd out

Rc vccNode out 2k
Q2 out q2base gnd mybjt
R3 q2base gnd 5k
dd q1emmiter q2base mydiode
Q1 q1collector q1base q1emmiter mybjt
R2 q1collector q1base 2k
R1 q1collector vccNode 1.75k
Da q1base in1 mydiode
Db q1base in2 mydiode

.ends dtlckt
```

```
*supply
vcc vccNode 0 5
Va in 0 5

*driver gate
Xd in in vccNode 0 out1 modifiedDTL

*load gates
XL1 out1 out1 vccNode 0 out2 modifiedDTL
XL2 out1 out1 vccNode 0 out3 modifiedDTL
XL3 out1 out1 vccNode 0 out4 modifiedDTL
XL4 out1 out1 vccNode 0 out5 modifiedDTL
XL5 out1 out1 vccNode 0 out6 modifiedDTL
XL6 out1 out1 vccNode 0 out7 modifiedDTL
XL7 out1 out1 vccNode 0 out8 modifiedDTL
XL8 out1 out1 vccNode 0 out9 modifiedDTL
XL9 out1 out1 vccNode 0 out10 modifiedDTL
XL10 out1 out1 vccNode 0 out11 modifiedDTL
XL11 out1 out1 vccNode 0 out12 modifiedDTL
XL12 out1 out1 vccNode 0 out13 modifiedDTL
XL13 out1 out1 vccNode 0 out14 modifiedDTL
XL14 out1 out1 vccNode 0 out15 modifiedDTL
XL15 out1 out1 vccNode 0 out16 modifiedDTL
XL16 out1 out1 vccNode 0 out17 modifiedDTL
XL17 out1 out1 vccNode 0 out18 modifiedDTL
XL18 out1 out1 vccNode 0 out19 modifiedDTL
XL19 out1 out1 vccNode 0 out20 modifiedDTL
XL20 out1 out1 vccNode 0 out21 modifiedDTL
XL21 out1 out1 vccNode 0 out22 modifiedDTL
XL22 out1 out1 vccNode 0 out23 modifiedDTL
```

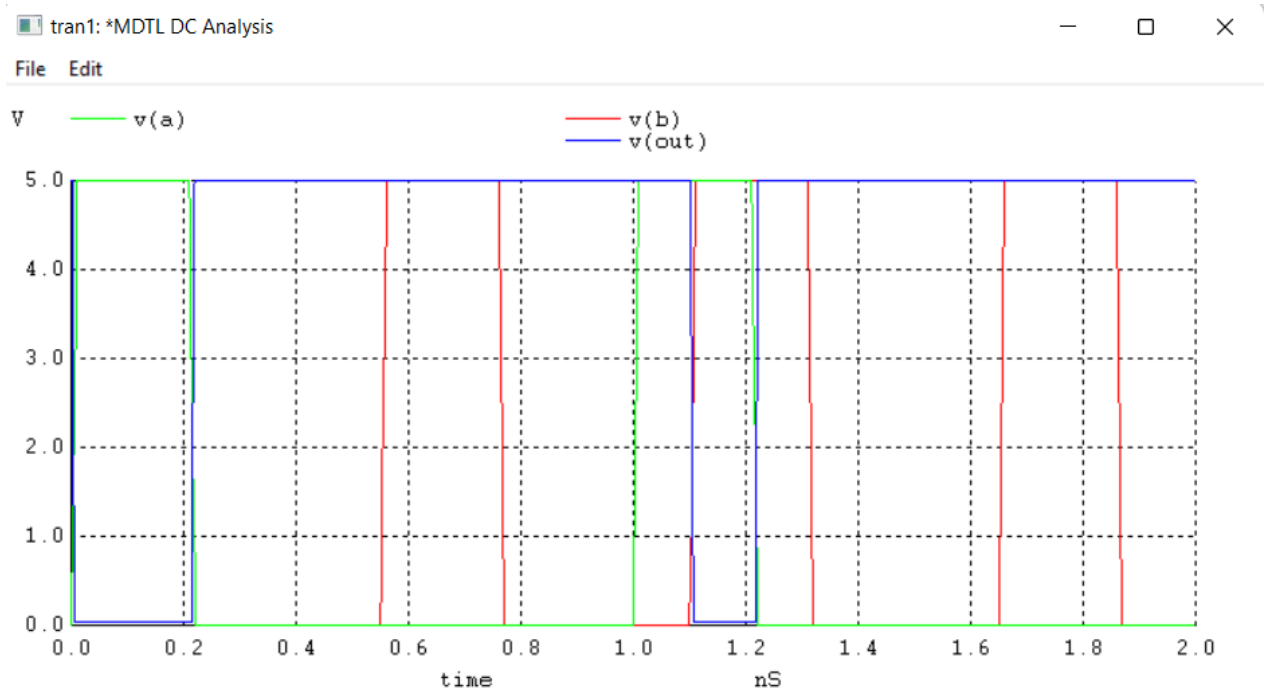
```
XL23 out1 out1 vccNode 0 out24 modifiedDTL
XL24 out1 out1 vccNode 0 out25 modifiedDTL
XL25 out1 out1 vccNode 0 out26 modifiedDTL
XL26 out1 out1 vccNode 0 out27 modifiedDTL
XL27 out1 out1 vccNode 0 out28 modifiedDTL
XL28 out1 out1 vccNode 0 out29 modifiedDTL
XL29 out1 out1 vccNode 0 out30 modifiedDTL
XL30 out1 out1 vccNode 0 out31 modifiedDTL
XL31 out1 out1 vccNode 0 out32 modifiedDTL
XL32 out1 out1 vccNode 0 out33 modifiedDTL
XL33 out1 out1 vccNode 0 out34 modifiedDTL

.dc Va 0.5 5 0.05

.control
run
plot V(out1) V(in)
.endc
.end
```

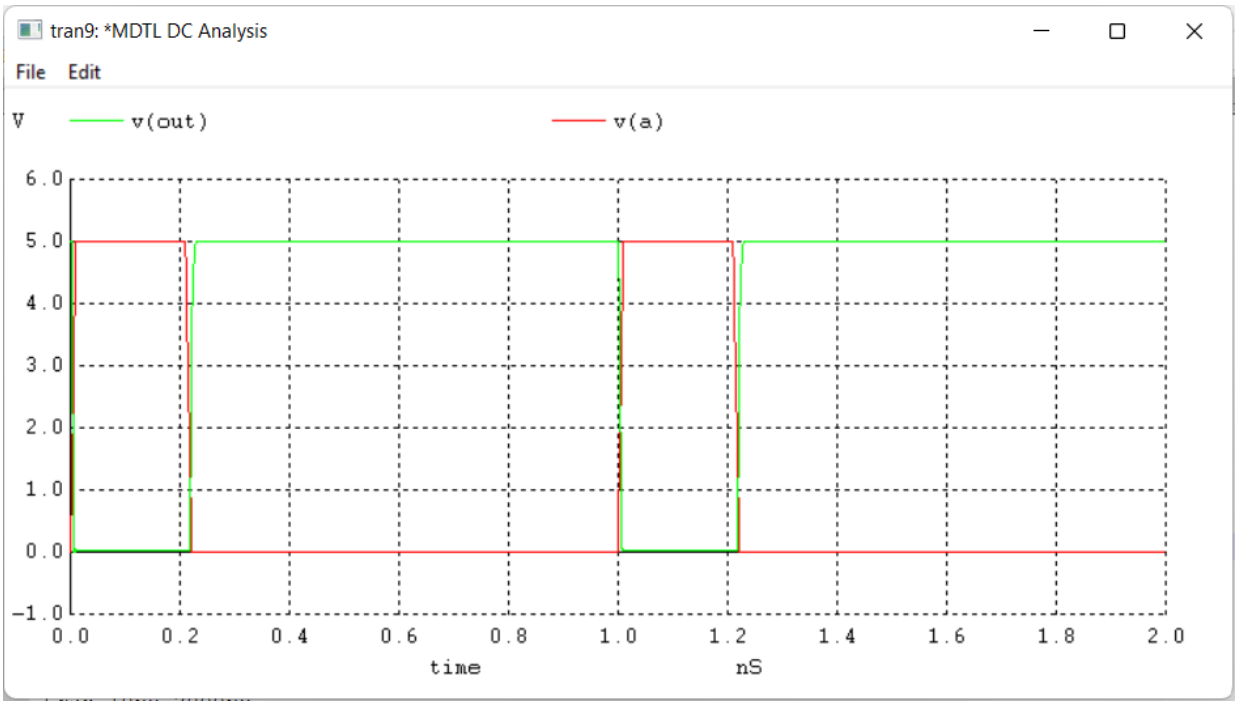
OUTPUT:

1. MDTL DC Analysis

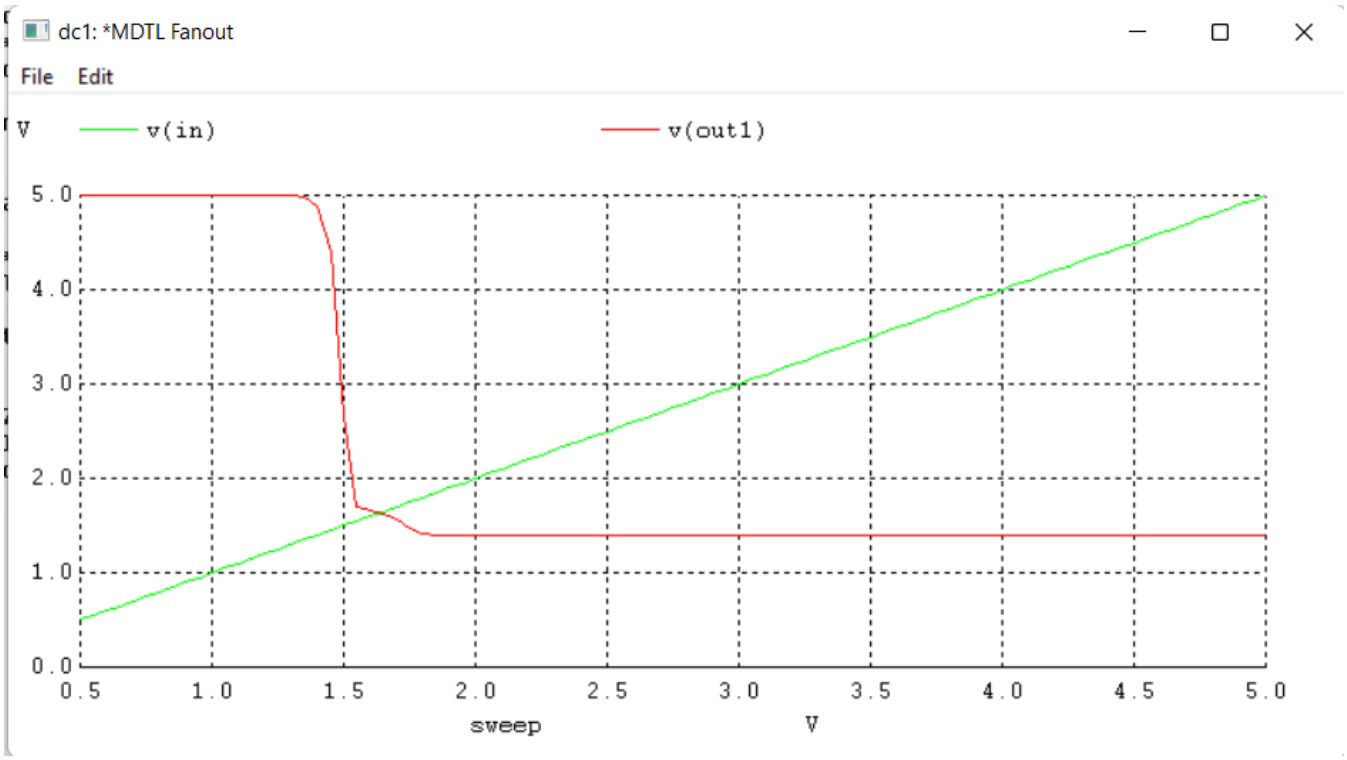


2. MDTL Transient Analysis





3. MDTL Fanout



THEORETICAL AND PRACTICAL CALCULATION:

4. DC Analysis
   V_{OH} = 5V, V_{IL} = 1.35V, V_{OL} = 0.075V and V_{IH} = 1.55V
   $NM_H = V_{OH} - V_{IH} = 5 – 1.55 = 3.45V$
   $NM_L = V_{IL} - V_{OL} = 1.35 – 0.075 = 1.275V$
   $NM(overall) = min(NM_H, NM_L) = 1.275V$

5. Transient Analysis
   τ_{PHL} = 9.4ps, τ_{PLH} = 5.135ps T_r = 6.3ps T_f = 4.09ps

6. Fanout
   Practical = 33
   Theoretical = 33

CONCLUSION: From the experiment we implemented and observed MDTL NAND Logic and calculated its various parameters from DC Analysis and Transient Analysis. We also calculated its Fanout from the practical as well as from the theoretical values which are exactly the same and hence verifying the practical value.

PRACTICAL 5

AIM: Implement TTL inverter using NPN BJT having Bf = 50, Rb = 4kΩ and Rc = 1.6kΩ.

4. Verify its functionality by performing transient analysis.
5. Plot the VTC & Calculate the Noise margin.
6. Find out theoretical and practical fan-out & compare them.

SOFTWARE USED: WinSpice Software

THEORY:

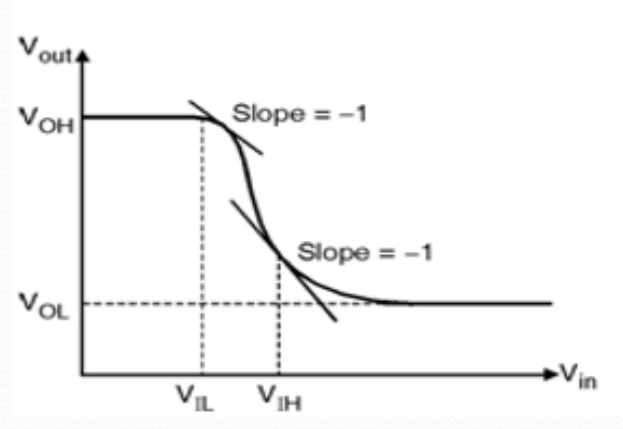
Introduction:

RTL Inverter is a circuit used to invert the input signal. It consists of one BJT transistor, Base connected with resistor (Rb), Collector connected with resistor (Rc) and Emitter is grounded. Input Signal is given to Base of transistor through Rb, Vcc is connected to Rc and Output is taken at collector terminal.

VOLTAGE TRANSFER CHARACTERISTICS (VTC):

To study the noise margins and the fan-out capability of the RTL inverter, we should know the static behaviour of the circuit output Vout when input Vin is increased from 0 to Vcc. When Vin is below the base-emitter cut-in voltage(V_{IL}), collector current is zero and transistor is in the cutoff mode, Vout is almost equal to Vcc (V_{OH}) (assuming no load is connected at output) and VTC will be constant output for 0<Vin<V_{IL}.

As Vin is increased beyond V_{IL}, the transistor enters active mode. The collector current (Ic = βIb) causes a voltage drop in the collector resistor and the collector voltage Vc = Vout = Vcc - IcRc falls. This fall continues until output saturation voltage (Vce=V_{OL}) BJT mode changes to saturation and corresponding input voltage is V_{IH}.



NOISE MARGINS:

Noise margin is the ratio by which the signal exceeds the minimum acceptable amount. It is normally measured in decibels. In a digital circuit, the noise margin is the amount by which the signal exceeds the threshold for a proper '0' or '1'.

$$NM_L = V_{IL} - V_{OL}$$

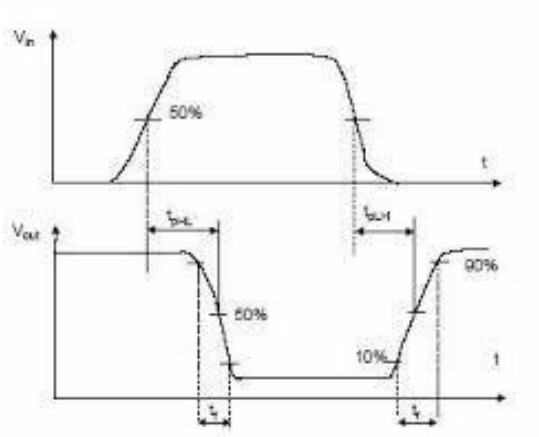
$$NM_H = V_{OH} - V_{IH}$$

In practice, noise margins are the amount of noise, that a logic circuit can withstand. Noise margins are generally defined so that positive values ensure proper operation, and negative margins result in compromised operation, or outright failure.

TRANSIENT RESPONSE:

Transient analysis means analyzing a system in unsteady state. If the variables involved in defining the state of a system does not vary with respect to time, then the system is said to be in steady state.

In Transient Analysis, also called time-domain transient analysis, computes the circuit's response a function of time. This analysis divides the time into segments and calculates the voltage and current levels for each interval.



PROPAGATION DELAY:

Propagation delay is a measure of how long it takes for a gate to change state. Ideally, should be as short as possible.

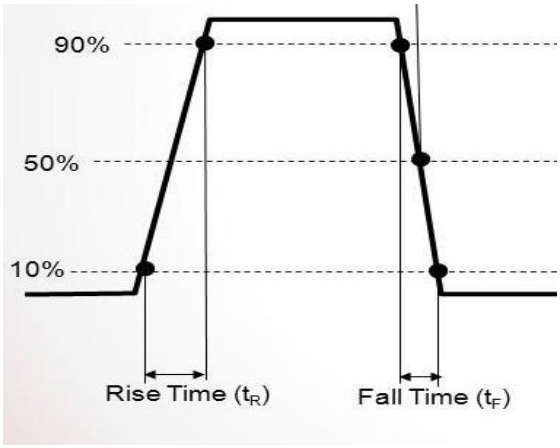
t_{PHL} – the time it takes the output to go from a high to low

t_{PLH} – the time it takes the output to go from a low to high

$$\text{Average Propagation Delay Time } (t_P) = \frac{t_{PHL} + t_{PLH}}{2}$$

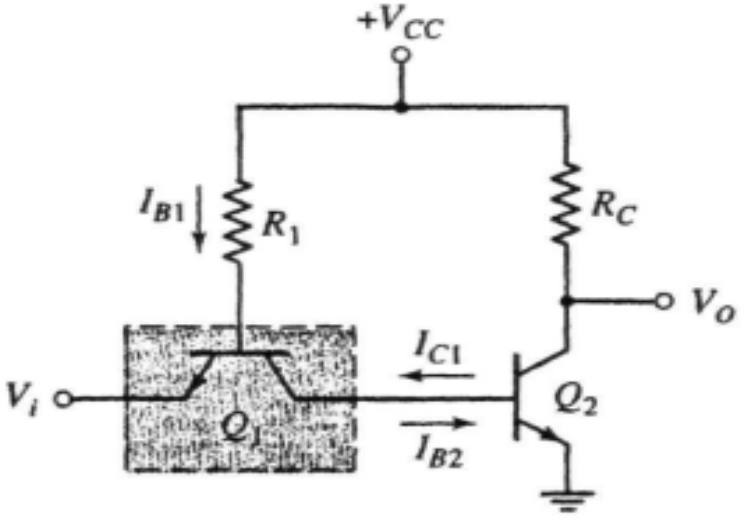
⇨ Rise Time (t_r) = Time from 10% to 90%

⇨ Fall Time (t_f) = Time from 90% to 10%



Circuit Diagram:

RTL inverter using NPN BJT



WINSPICE CODES:

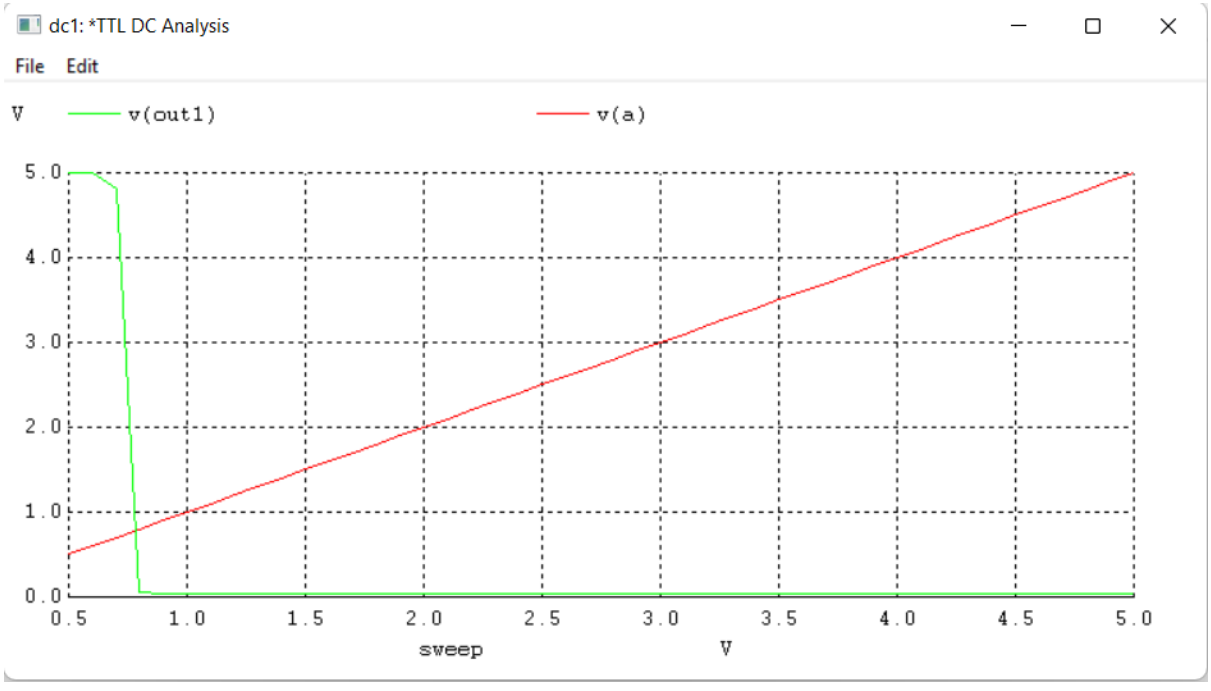
```
*TTL DC Analysis

.model myBJT NPN ( BF = 50 )

.subckt TTL a c out 0
Q1 1 3 a myBJT
Q0 out 1 0 myBJT
Rb c 3 4k
Rc c out 1.6k
.ends TTL

Vcc c 0 5
Vin a 0 5

Xd a c out1 0 TTL

.dc Vin 0.5 5 0.1

.control
run
plot V(a) V(out1)
.endc
.end

*TTL Transient Analysis

.model X NPN ( BF = 50 )

Q1 1 3 2 X
Q0 out 1 0 X
```

```
Rb c 3 4k
Rc c out 1.6k
C1 out 0 0.001p

Vcc c 0 5
Vin 2 0 pulse (0 5 0ps 10ps 10ps 200ps 1000ps)

.tran 10ps 2000ps

.control
run
plot v(2) v(out)
.endc
.end

*TTL Fanout

.model myBJT NPN ( BF = 50 )

.subckt TTL a c out 0
Q1 1 3 a myBJT
Q0 out 1 0 myBJT
Rb c 3 4k
Rc c out 1.6k
.ends TTL

Vcc c 0 5
Vin a 0 5

Xd a c out1 0 TTL

X1 out1 c out2 0 TTL
```

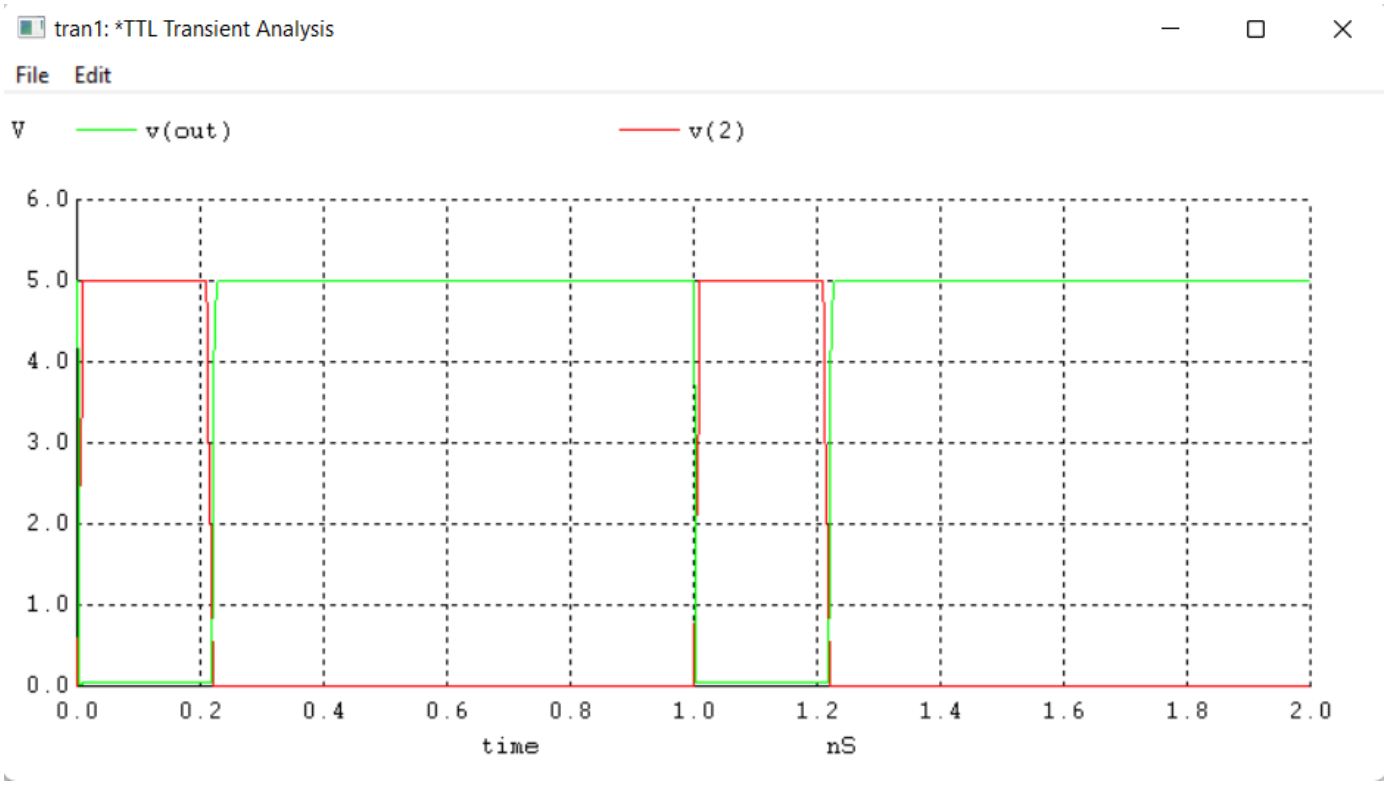
```
X2 out1 c out3 0 TTL
X3 out1 c out4 0 TTL
X4 out1 c out5 0 TTL
X5 out1 c out6 0 TTL
X6 out1 c out7 0 TTL
X7 out1 c out8 0 TTL

.dc Vin 0.5 5 0.1

.control
run
plot V(a) V(out1)
.endc
.end
```

OUTPUT:

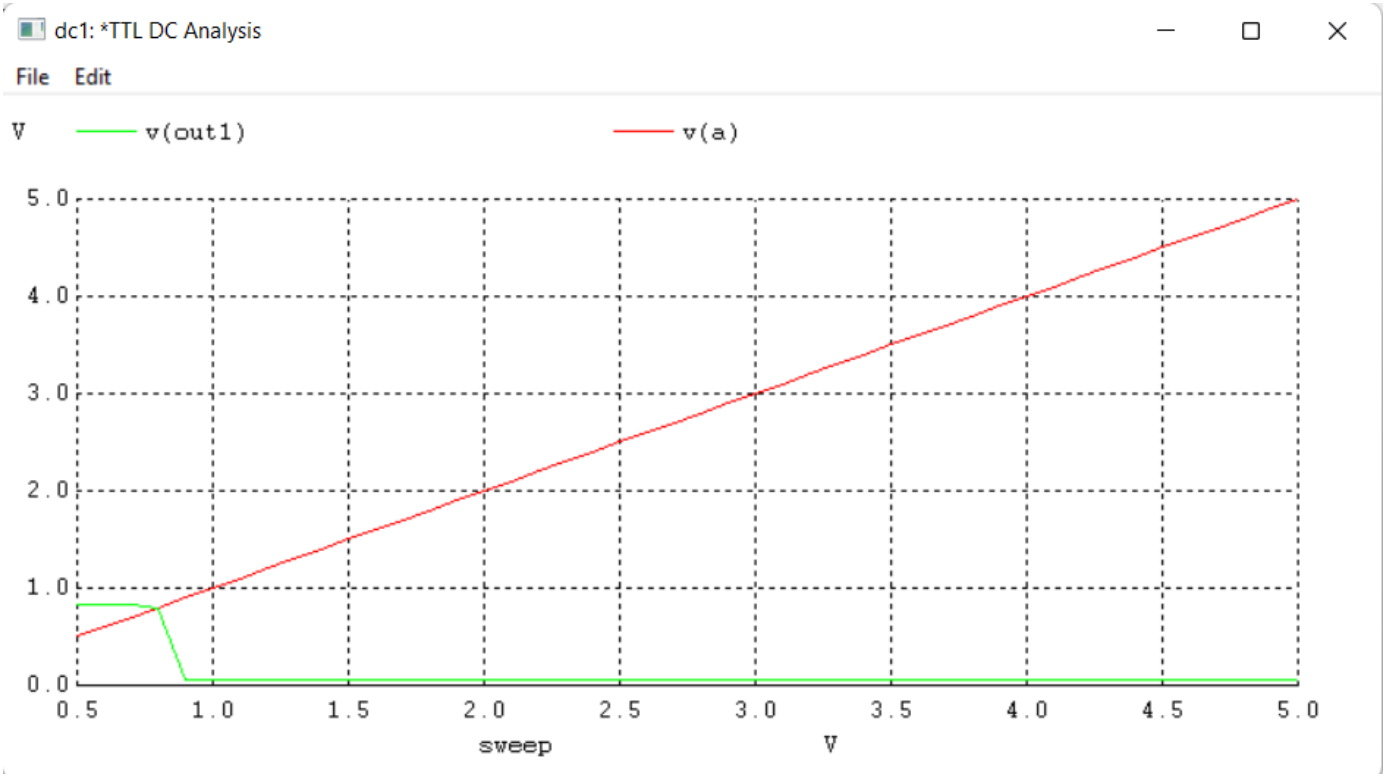
1. TTL Invertor DC Analysis



2. TTL Invertor Transient Analysis



3. TTL Invertor Fanout



THEORETICAL AND PRACTICAL CALCULATION:

7. DC Analysis
   V_{OH} = 5V, V_{IL} = 0.6V, V_{OL} = 0.06V and V_{IH} = 0.8V
   $NM_H = V_{OH} - V_{IH} = 5 – 0.8 = 4.2V$
   $NM_L = V_{IL} - V_{OL} = 0.6 – 0.06 = 0.54V$
   $NM(overall) = min(NM_H, NM_L) = 0.54V$

8. Transient Analysis
   τ_{PHL} = 3.3ps, τ_{PLH} = 5ps T_r = 4ps T_f = 0.4ps

9. Fanout
   Practical = 7
   Theoretical = 7

CONCLUSION: From the experiment we implemented and observed TTL Invertor and calculated its various parameters from DC Analysis and Transient Analysis. We also calculated its Fanout from the practical as well as from the theoretical values which are exactly the same and hence verifying the practical value.

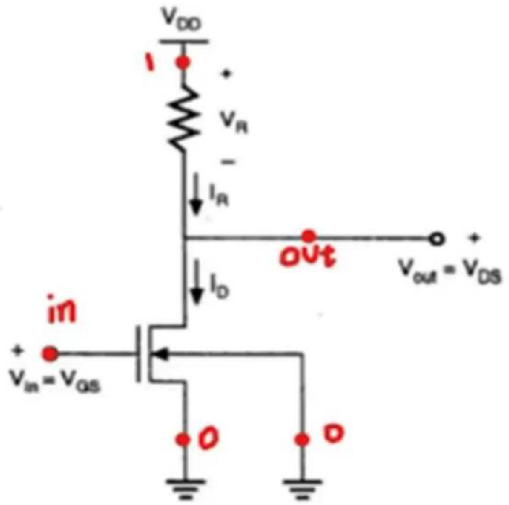
PRACTICAL – 06

AIM: To design and verify the performance of given Resistively Loaded NMOS inverter circuit to obtain VOL = 0.147V for the given specifications:

Kn' = 20uA/V, Vt0 = 0.8V, VDD = 5V, W/L = 2um/um.

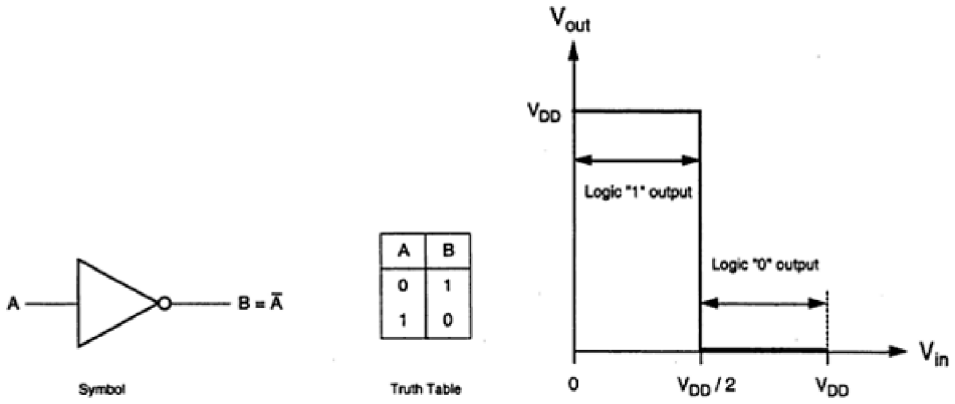
Find the noise margin of the circuit. Also see the effect of change in RL on noise margin and comment on it..

THEORY:

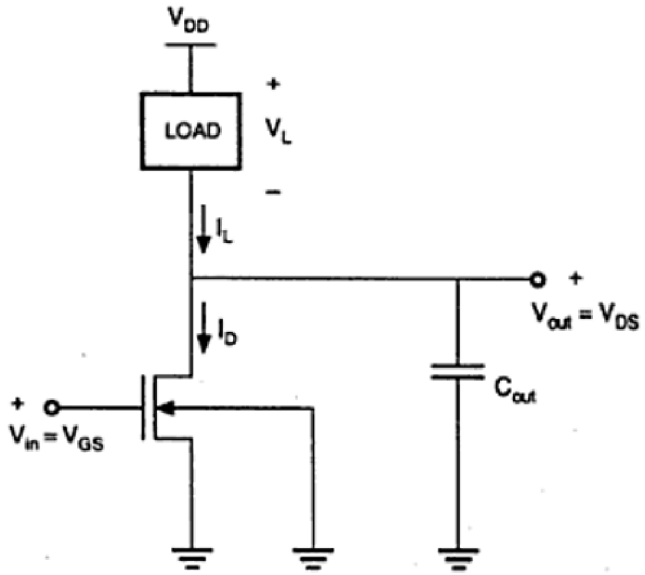


The logic symbol and truth table of ideal inverter is shown in figure given below. Here A is the input and B is the inverted output represented by their node voltages. Using positive logic, the Boolean value of logic 1 is represented by Vdd and logic 0 is represented by 0. Vth is the inverter threshold voltage, which is Vdd /2, where Vdd is the output voltage.

The output is switched from 0 to Vdd when input is less than Vth. So, for 0<Vin<Vth output is equal to logic 0 input and Vth<Vin< Vdd is equal to logic 1 input for inverter.



The characteristics shown in the figure are ideal. The generalized circuit structure of an nMOS inverter is shown in the figure below.



From the given figure, we can see that the input voltage of inverter is equal to the gate to source voltage of nMOS transistor and output voltage of inverter is equal to drain to source voltage of nMOS transistor. The source to substrate voltage of nMOS is also called driver for transistor which is grounded; so VSS = 0. The output node is connected with a lumped capacitance used for VTC.

WINSPICE CODES:

1. Static Analysis

```
# NMOS static analysis
.model M1 NMOS (Vt0=0.8 kp=20u)
M11 2 3 0 0 M1 w=2u L=1u
R1 2 4 200.537K
Vdd 4 0 5
Vin 3 0 dc 5

.dc Vin 0 5 0.05
.control
run

plot v(2) v(3)
.endc
.end
```

2. Transient Analysis:

```
#NMOS transient analysis
.model M1 NMOS (Vt0=0.8 kp=20u)
M11 2 3 0 0 M1 w=2u L=1u
R1 2 4 200K
Vdd 4 0 5
Vin 3 0 pulse (0 5 1ps 1ps 1ps 20us 40us)
c 2 0 1p

.tran 10ns 80us
.control
run
```

```
plot v(2) v(3)
.endc
.end
```

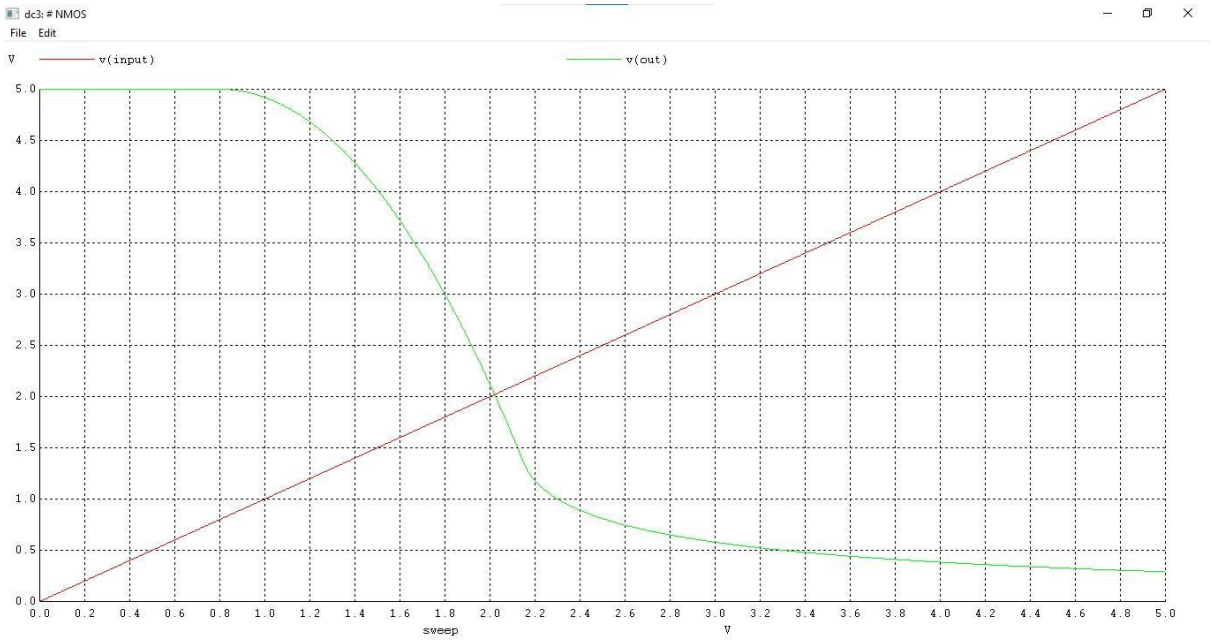
3. Varying load resistance:

```
*NMOS varying load resistance
.model M1 NMOS (Vt0=0.8 kp=20u)
*200k
M11 d g 0 0 M1 w=2u L=1u
RL1 1 d 200K
Vdd1 1 0 5
*100k
M12 d1 g 0 0 M1 w=2u L=1u
RL2 2 d1 100K
Vdd2 2 0 5
*400k
M13 d2 g 0 0 M1 w=2u L=1u
RL3 3 d2 400K
Vdd3 3 0 5
*800k
M14 d3 g 0 0 M1 w=2u L=1u
RL4 4 d3 800K
Vdd4 4 0 5
Vin g 0 dc 5
.dc Vin 0 5 0.05
.control
run
plot v(g) v(d) v(d1) v(d2) v(d3)
```

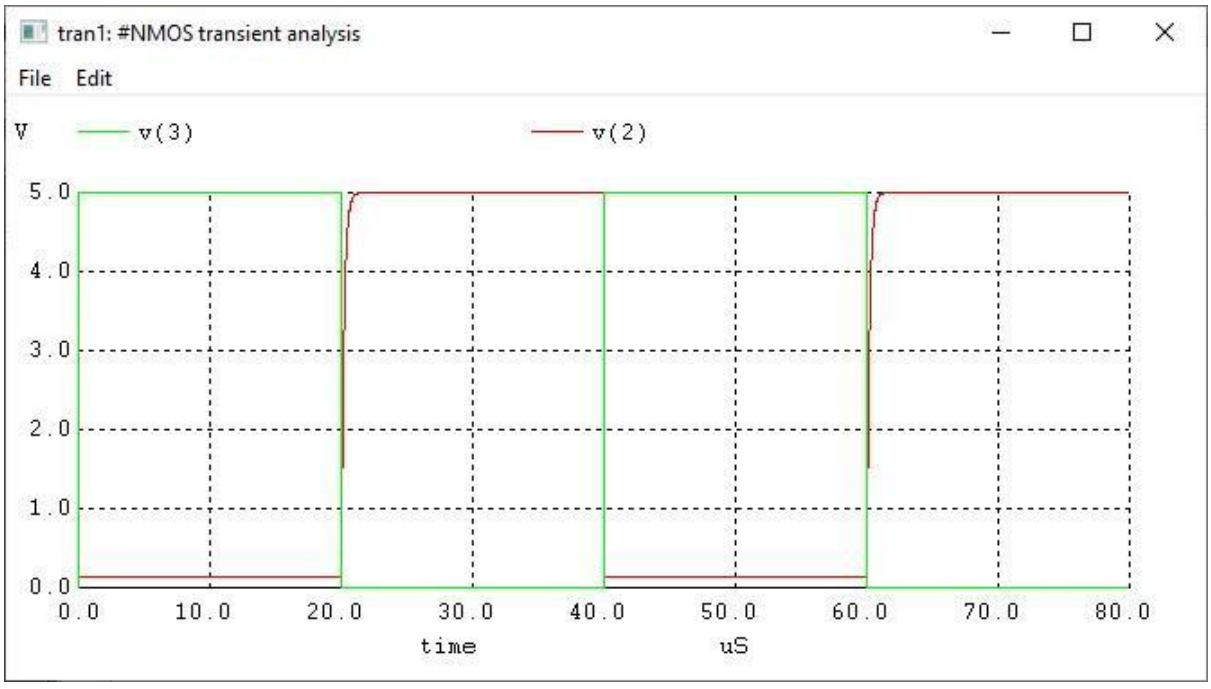
```
.endc
.end
```

OUTPUT:

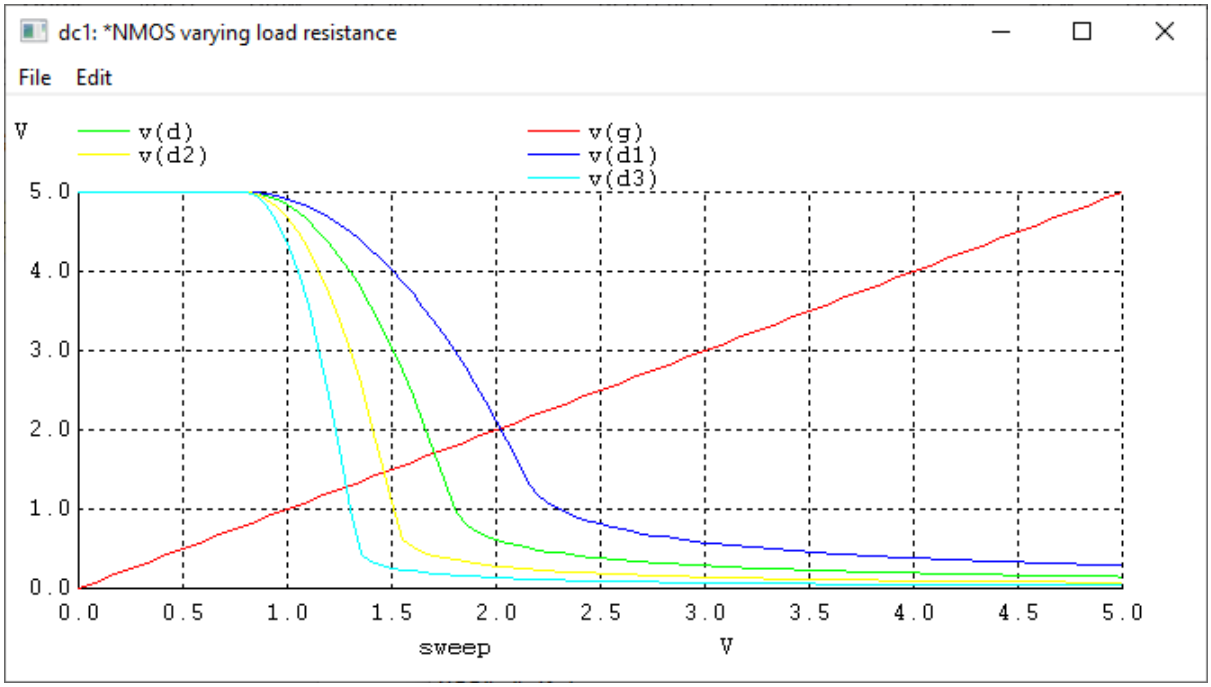
1. DC Analysis



2.. Transient Analysis:



2. Varying load resistance:



RESULT:

Theoretical NM	Practical NM

CONCLUSION: Thus, NMOS inverter can be designed using MOSFET and the noise margin calculated practically and theoretically were found to be almost similar. It was also observed that as we increase load the VTC tends toward more ideal characteristic.

PRACTICAL 7

AIM: Design and verify the performance of given saturated loaded NMOS inverter circuit to obtain Vih-2.9, for the given design parameter VDD=5V, Kn'=20ua/v^2, Vtl-0.8V, Vtl=0.8V, (W/L)driver=2um/1um.

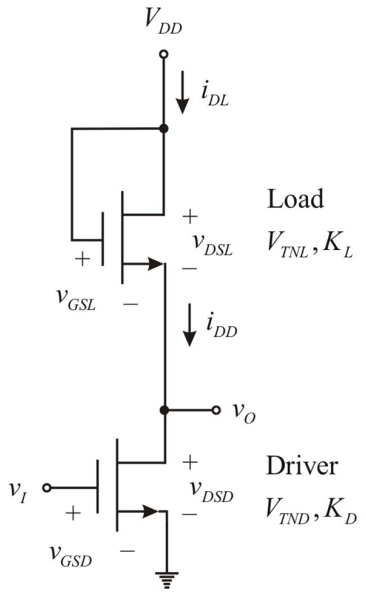
d) Compare the theoretical and practical values of the critical voltages on VTC& find noise margins of the circuit.
e) observe the effect of change in (W/L) loaded on noise margin &comment on it.
f) Also compare the results of noise with resistive loaded NMOS inverter for RL=200k

SOFTWARE USED: WinSpice Software

THEORY:

An n-channel enhancement-mode MOSFET with the gate connected to the drain can be used as load device in an NMOS inverter. Since the gate and drain of the transistor are connected, we have V_{GS}-V_{DS} When V_{GS}-V_{DS}>V_{TN}, a non zero drain current is induced in the transistor and thus the load circuit operates in saturation only. It has advantages over Resistive Load NMOS Inverter.

CIRCUIT DIAGRAM:



FORMULAS:

CALCULATIONS:

WINSPICE CODES:

1. Voltage Transfer Characteristics and Noise Margin

```
* saturated load Inverter DC Analysis

.model mymos NMOS (Vt0=0.8 kp=20u)
M1 1 1 out 0 mymos l=1u w=2u
M2 out in 0 0 mymos l=1u w=2u
Vdd 1 0 5V
Vin in 0 5V
.dc Vin 0 5 0.05
.control
run
plot V(out) V(in)
.endc
.end
```

2. Saturated inverter Static Multiple Analysis (For Different Kn)

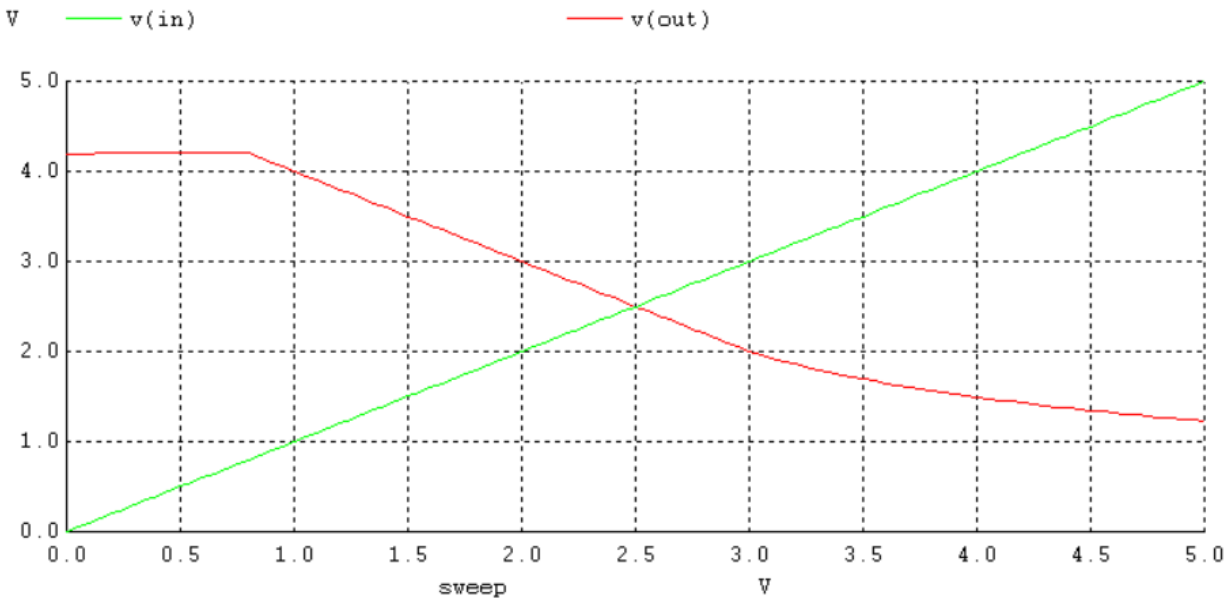
```
* saturated load Inverter DC Analysis For Different Kn


.model mymos NMOS (Vt0=0.8 kp=20u)
M1 d1 d1 out 0 mymos l=1u w=2u
M2 out in 0 0 mymos l=1u w=2u


Vdd1 d1 0 5V
Ma1 d2 d2 out1 0 mymos l=1u w=4u
Mb1 out1 in 0 0 mymos l=1u w=2u


Vdd2 d2 0 5V
Ma2 d3 d3 out2 0 mymos l=1u w=6u
Mb2 out2 in 0 0 mymos l=1u w=2u


Vdd3 d3 0 5V
```

```
Ma3 d4 d4 out3 0 mymos l=1u w=8u
Mb3 out3 in 0 0 mymos l=1u w=2u

Vdd4 d4 0 5V
Vin in 0 5V

.dc Vin 0 5 0.05
.control
run
plot V(out) V(out1) V(out2) V(out3) V(in)
.endc
.end
```

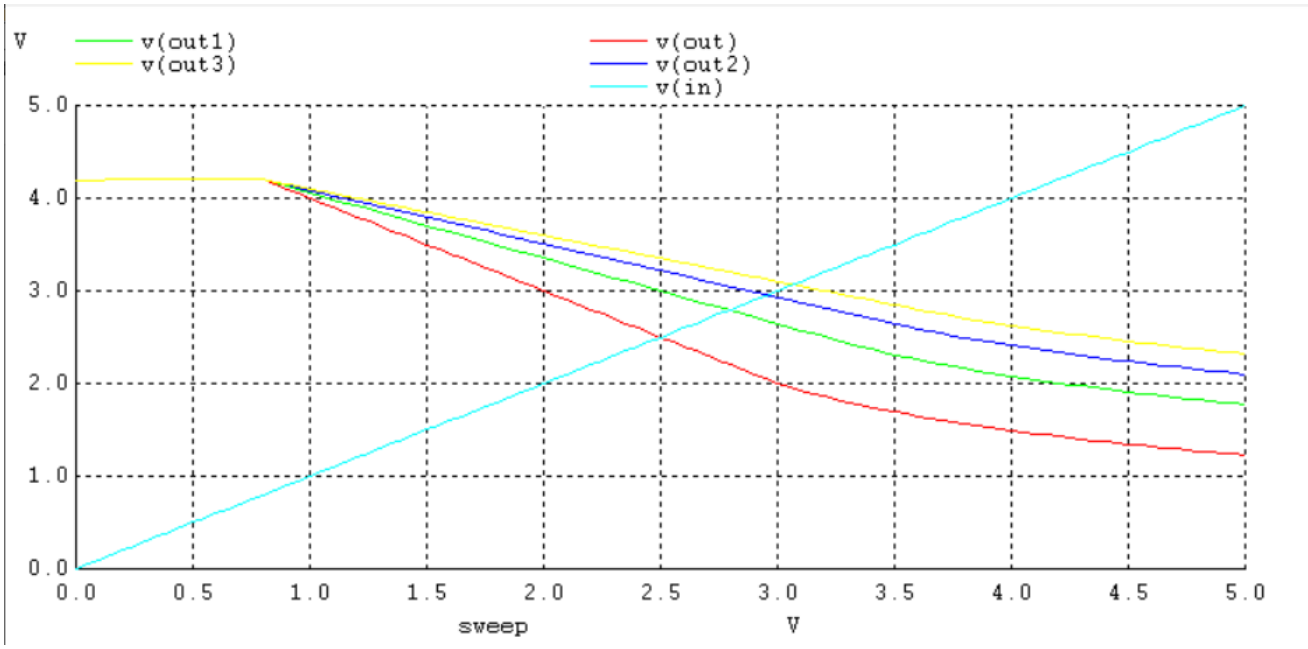
3. Saturated Load Inverter and Resistive Load Inverter(R=200kΩ)

```
* saturated load Inverter and Resistive Load Inverter

.model mymos NMOS (Vt0=0.8 kp=20u)
M1 1 1 out 0 mymos l=1u w=2u
M2 out in 0 0 mymos l=1u w=2u
Vdd 1 0 5V
Vin in 0 5V

r d1 out1 200k
MR out1 in 0 0 mymos l=1u w=2u
Vdd1 d1 0 5V

.dc Vin 0 5 0.05
.control
run
plot V(out) V(out1) V(in)
.endc
.end
```

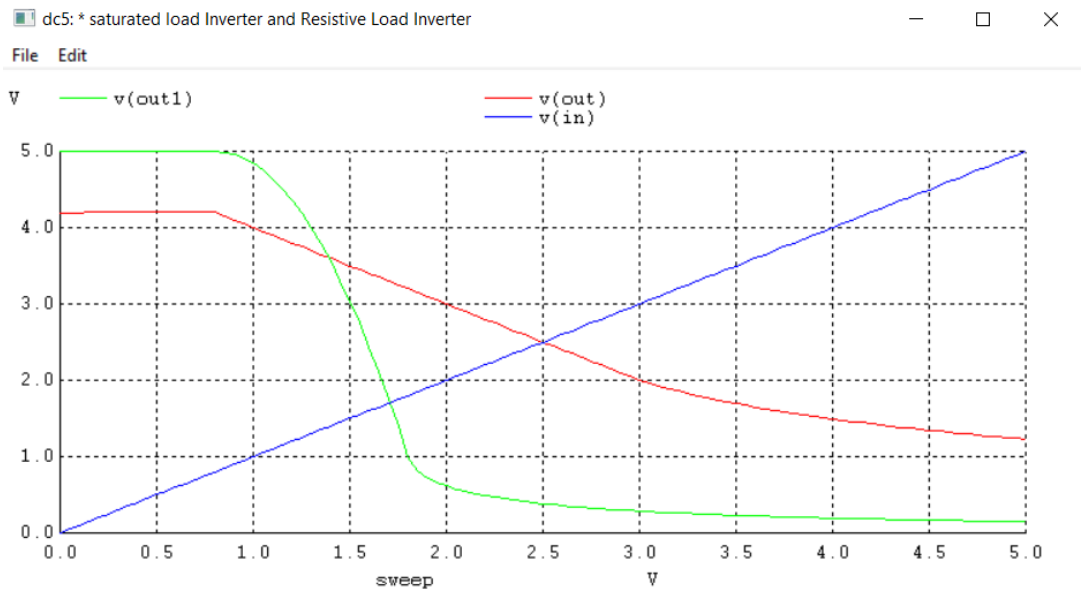
OUTPUT:



VTC and Noise Margin



For Different Kn



Saturated Load Inverter and Resistive Load Inverter VTC Plots combined

Table 1**:** Comparison Of theoretical and practical value of critical values of VTC.

Parameters	**Theoretical values (V)**	**Practically Values (V)**
V_{OL}		
V_{OH}		
V_{IL}		
V_{IH}		
V_{TH}		
NM_L		
NM_H		

Table 2: Effect of variation of $(W/L)_{load}$ on Noise Margin:

Parameters $(W/L)_{LOAD}$	**V_{OL}**	**V_{OH}**	**V_{IH}**	**V_{IL}**	**NM_L**	**NM_H**
4/1						
6/1						
8/1						

Table 3: Comparison Of Noise Margin of Resistively and Saturated Loaded NMOS inverter.

	NM_L	**NM_H**
Resistively Loaded NMOS		
Saturated Loaded NMOS		

CONCLUSION: From the above experiment we implemented a saturated load nmos invertor using winspice and observed their output plots. We also observed the output plots of VTC characteristics for different values of kn and observed that with the increase in the kn the transient time becomes more larger. We also compared it with the resistively loaded nmos invertor and observed its output plot from which we can observe that V_{OH} is increased and V_{OL} is reduced in case of saturated load and its transient time is reduced as well.

PRACTICAL 8

AIM: Design and verify the performance of given CMOS inverter circuit to obtain switching threshold voltage of 2.2V. Given specifications for the CMOS inverter are:
V_{TN} = 0.8V, V_{TP} = -1V, V_{DD} = 5V, K_n' = 20µA/V^2, K_p' = 50µA/V^2, L_n = L_p = 1µm.

Compare the theoretical and practical values of critical voltages on VTC and find the noise margin of the circuit. Observe the following parameters and comment on it.

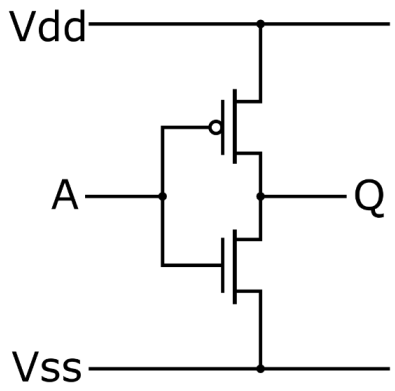
1. Variation of VDD from 5V to 3.3V on the switching threshold voltage of CMOS inverter.
2. Variation of Kr at 0.25, 1 and 4 on the switching characteristics.

SOFTWARE USED: WinSpice Software

THEORY:

The term CMOS stands for "Complementary Metal Oxide Semiconductor". CMOS technology is one of the most popular technology in the computer chip design industry and broadly used today to form integrated circuits in numerous and varied applications. This technology make use of both p-channel (PMOS) and nchannel (NMOS) semiconductor devices. The main advantage of CMOS over NMOS and bipolar technology is the much smaller power dissipation. Unlike NMOS or BIPOLAR circuits, a complementary MOS circuit has almost no static power dissipation. Power is only dissipated in case the circuit actually switches. VTC Characteristics are more symmetrical in CMOS than NMOS and noise margin offered is much higher. This allows integrating more CMOS gates on an IC than in MOS or bipolar technology, resulting in much better performance.

CIRCUIT DIAGRAM:



FORMULAS:

CALCULATIONS:

WINSPICE CODES:

1. Voltage Transfer Characteristics and Noise Margin

```
*CMOS Inverter
.model mynmos nmos Vto=0.8 Kp=50
.model mypmos pmos Vto=-1 Kp=20

.subckt cmosinverter1 in vdd_node out gnd
M1 out in gnd gnd mynmos w=1u l=1u
M2 vdd_node in out vdd_node mypmos w=1.51u l=1u
.ends cmosinverter1

xd1 in vdd_node out_1 0 cmosinverter1

Vdd vdd_node 0 5
Vin in 0 5
.dc Vin 0 5 0.005

.control
run
plot v(in) v(out_1)
.endc
.end
```

2. Transient Analysis

```
* CMOS Transient Analysis


.model mynmos NMOS (Vt0=0.8, Kp=50u)
.model mypmos PMOS (Vt0=-1, Kp=20u)


.subckt cmosinverter in vdd_node out gnd
    MN out in gnd gnd mynmos w=1um l=1um
    MP vdd_node in out vdd_node mypmos w=1.51um l=1um
.ends cmosinverter


Vdd vdd_node 0 5
```

```
Vin input 0 pulse(0 5 1ns 1ns 1ns 20us 40us)


Xd input vdd_node out 0 cmosinverter


.tran 1ns 80us


.control

run

plot v(input) v(out)

.endc

.end
```

3. Variation of Vdd.

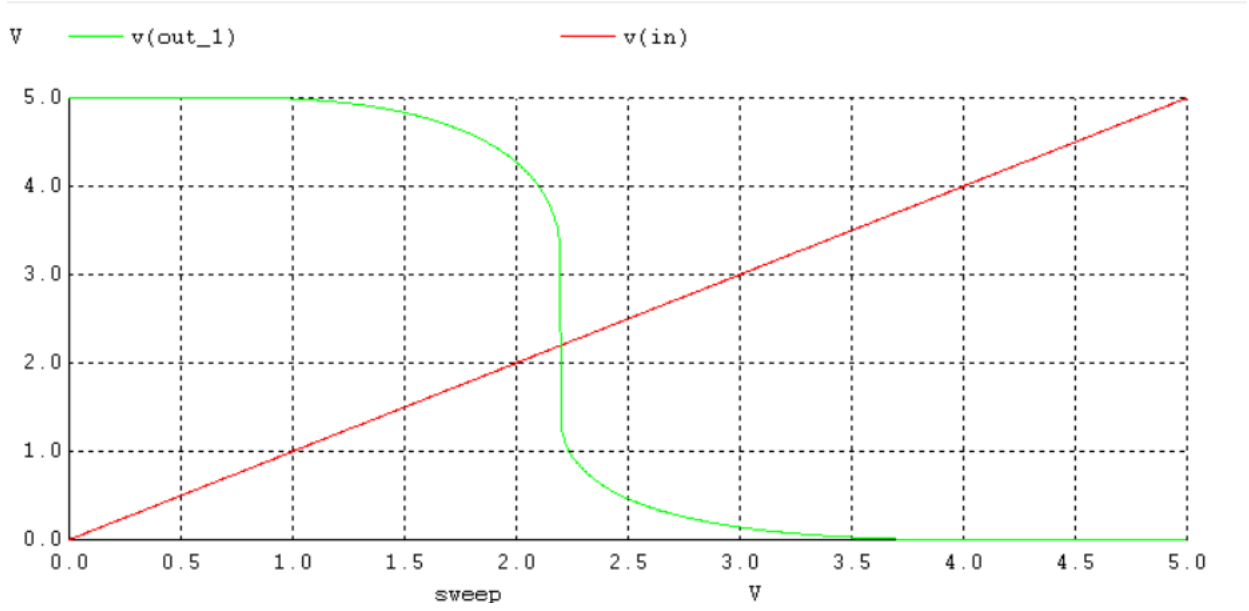
```
* CMOS Variation of Vdd
.model mynmos NMOS (Vt0=0.8, Kp=50u)
.model mypmos PMOS (Vt0=-1, Kp=20u)

.subckt cmosinverter in vdd_node out gnd
    MN out in gnd gnd mynmos w=1um l=1um
    MP vdd_node in out vdd_node mypmos w=1.51um l=1um
.ends cmosinverter

Vdd vdd_node 0 5
Vin input 0 5

Xd input vdd_node out 0 cmosinverter

.dc Vin 0 5 0.005 Vdd 3.3 5 1.7

.control
run
plot v(input) v(out)
.endc
.end
```

4. Varaiation of Kr

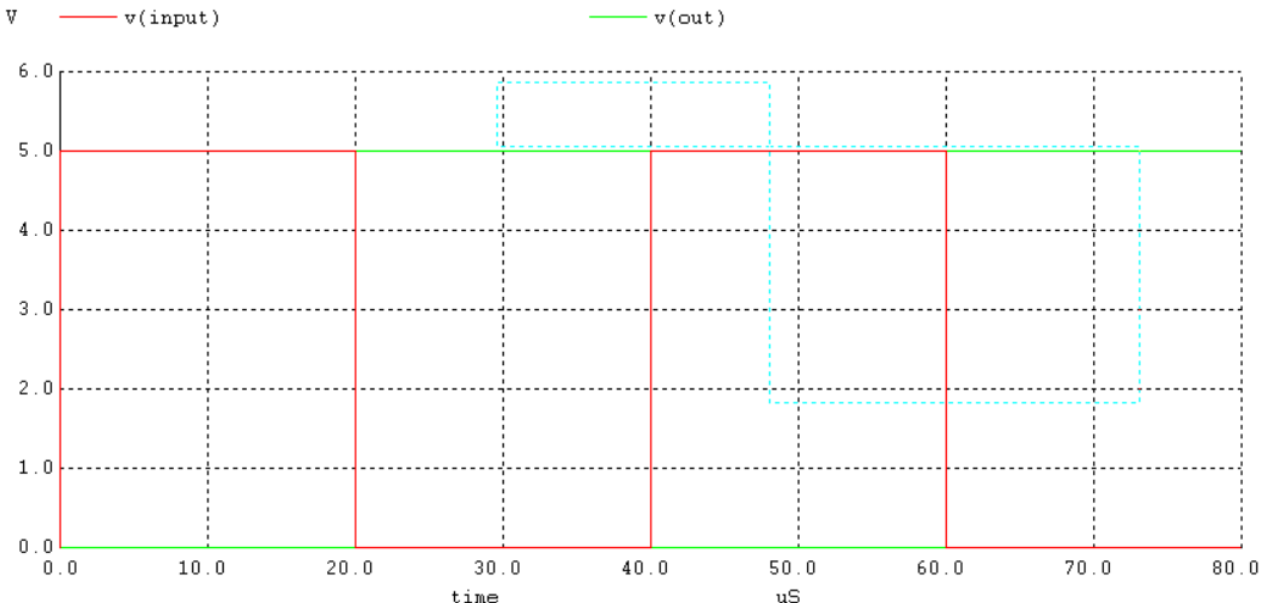
```
*CMOS Inverter
.model mynmos nmos Vto=0.8 Kp=50
```

```
.model mypmos pmos Vto=-1 Kp=20

.subckt cmosinverter1 in vdd_node out gnd
M1 out in gnd gnd mynmos w=0.02u l=1u
M2 vdd_node in out vdd_node mypmos w=0.05u l=1u
.ends cmosinverter1

.subckt cmosinverter2 in vdd_node out gnd
M1 out in gnd gnd mynmos w=0.02u l=1u
M2 vdd_node in out vdd_node mypmos w=0.2u l=1u
.ends cmosinverter2

.subckt cmosinverter3 in vdd_node out gnd
M1 out in gnd gnd mynmos w=0.08u l=1u
M2 vdd_node in out vdd_node mypmos w=0.05u l=1u
.ends cmosinverter3

xd1 in vdd_node out_1 0 cmosinverter1
xd2 in vdd_node out_2 0 cmosinverter2
xd3 in vdd_node out_3 0 cmosinverter3

Vdd vdd_node 0 5
Vin in 0 5
.dc Vin 0 5 0.005

.control
run
plot v(in) v(out_1) v(out_2) v(out_3)
.endc
.end
```

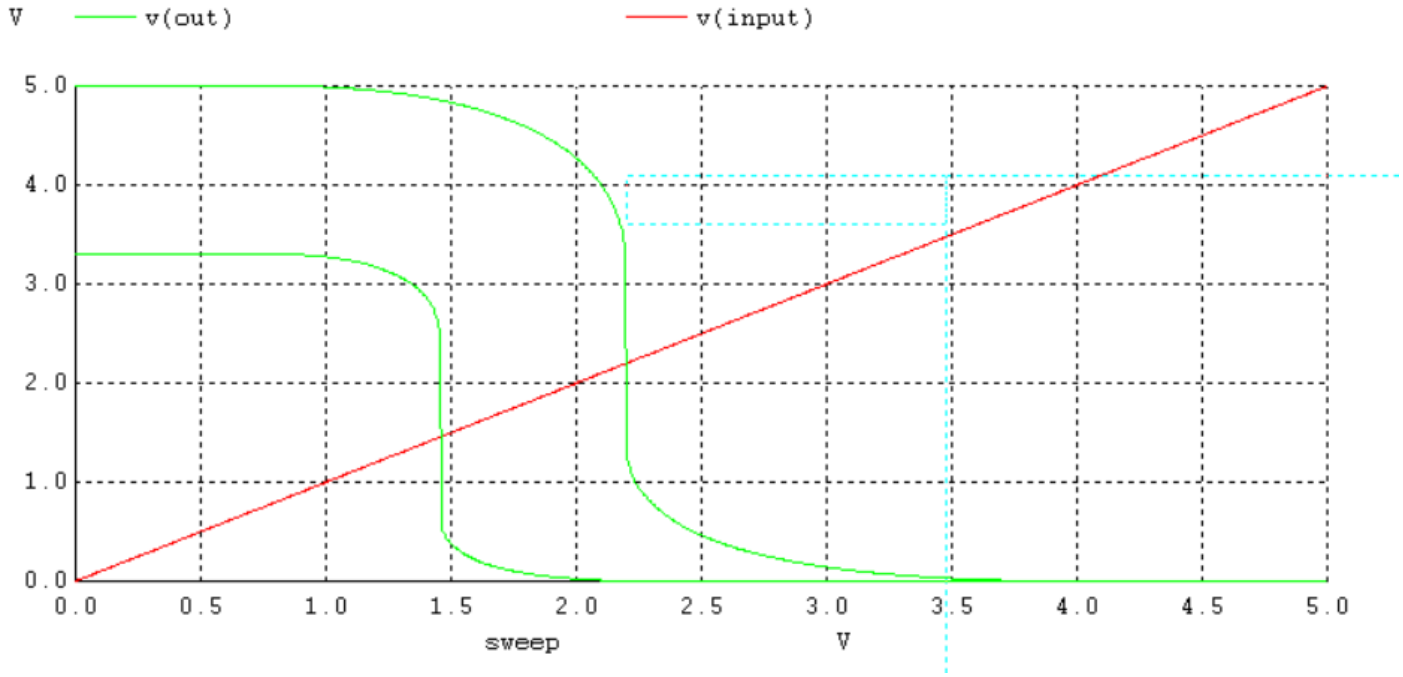
OUTPUT:



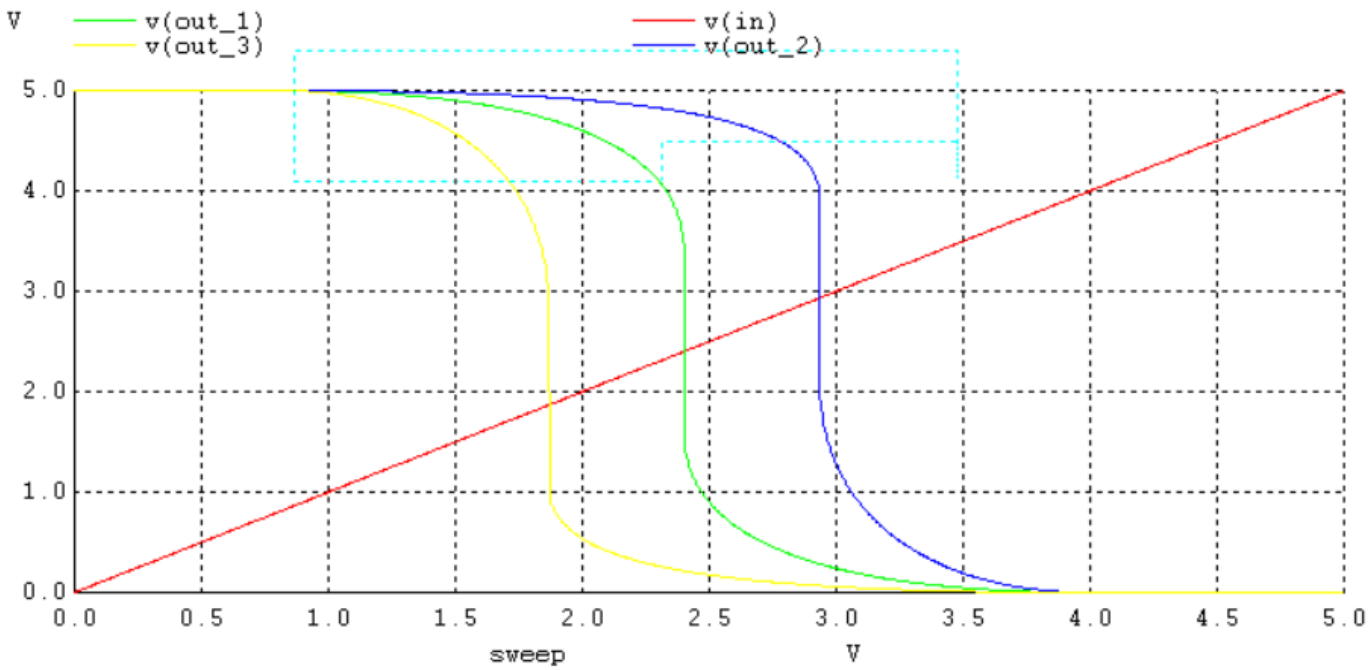
VTC and Noise Margin



Transient Analysis



Varaiation of Vdd



Varaition of Kr

Table 1: Noise Margin

Parameters	Theoretical	Practical
VOH		
VOL		
VIH		
VIL		
VTH		
Noise Margin High		
Noise Margin Low		
Noise Margin		

Table 2: Effect of V_{DD} variation on V_{TH}

V_{DD} (V)	VTH (V)
5	
4	
3	

Table 3: Effect of k_r variation on V_{TH}

k_r	V_{TH} (V)
0.25	
1	
4	

CONCLUSION: From the above experiment we implemented a cmos invertor using winspice and observed their output plots. We also observed the output plots of VTC characteristics for different values of kr and observed that with the increase in the kr the transient time becomes smaller. Also with the variations in V_{DD} the V_{OH} changes accordingly.

PRACTICAL 9

ASSIGNMENT 1

AIM: Write a winspice code to verify the functionality of given bicmos inverter circuit using default model parameters for the transistor.

SOFTWARE USED: WinSpice Software

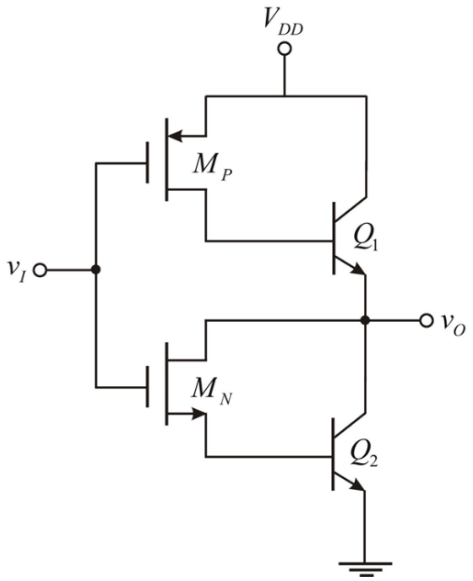
THEORY:

In BiCMOS technology, both the MOS and bipolar device are fabricated on the same chip.The objective of the BiCMOS is to combing bipolar and CMOS so as to exploit the advantages of both the technologies.Today BiCMOS has become one of the dominant technologies used for high speed, low power and highly functional VLSI circuits.

Advantages of bipolar and CMOS circuits can be retained in BiCMOS chips.

- BiCMOS technology enables high performance integrated circuits IC's but increases process complexity..
- CMOS technology offers less power dissipation, smaller noise margins, and high packing density.
- Bipolar technology, on the other hand, ensure high switching and I/O speed and good noise performance. Now we are in 3rd Generation BiCMOS Technology.
- BiCMOS technology accomplishes both improved speed over CMOS and lower power dissipation than bipolar technology.
- The main drawback of BiCMOS technology is the higher costs due to the added process complexity.
- This greater process complexity in BiCMOS results in a cost increase compared to conventional CMOS technology.

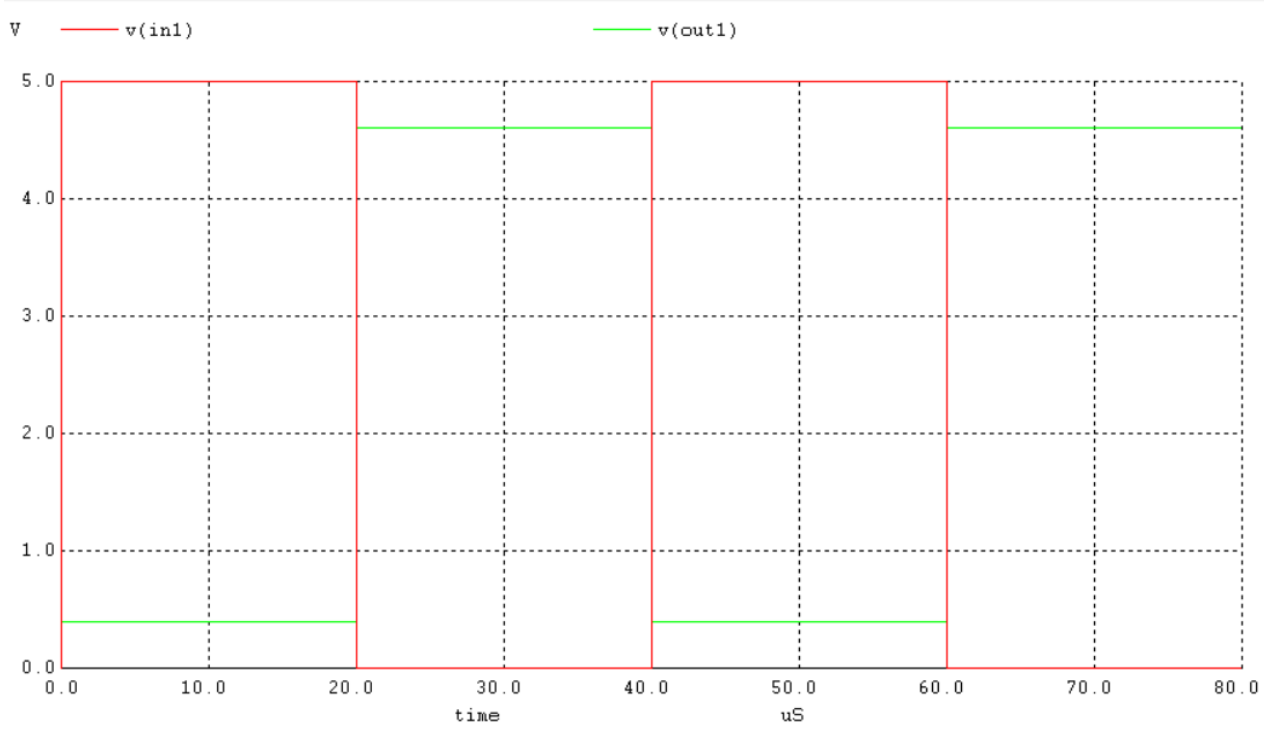
CIRCUIT DIAGRAM:



WINSPICE CODES:

```
*BICMOS transient char*

.model q1 npn bf=50
.model mynmos nmos Vto=0.8 Kp=50
.model mypmos pmos Vto=-1 Kp=20

.subckt BI in vdd_node out1 out2 src
M1 out1 in src src mynmos w=1u l=1u
M2 out2 in vdd_node vdd_node mypmos w=1.51u l=1u
.ends BI

q11 vdd_node out2 out1 q1
q12 out1 src 0 q1
xd1 in1 vdd_node out1 out2 src BI
Vdd vdd_node 0 5

Vin in1 0 pulse(0 5 1ns 1ns 1ns 20us 40us)

.tran 1ns 80us
.control
run
plot v(in1) v(out1)
.endc
.end
```

OUTPUT:



Transient Analysis

CONCLUSION: From the above experiment we implemented a Bi-CMOS circuit using WinSpice and verified its functionality using transient analysis as an invertor circuit.

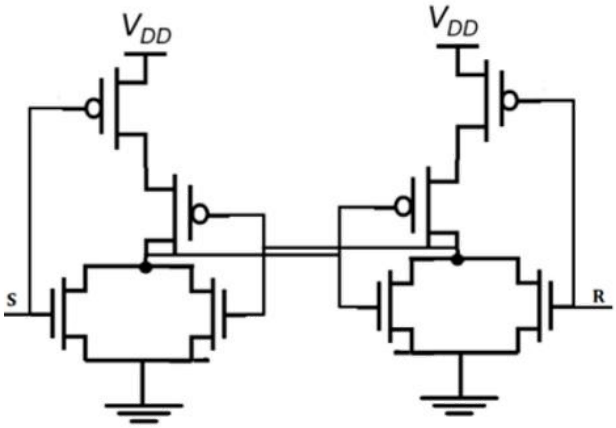
PRACTICAL – 9.2

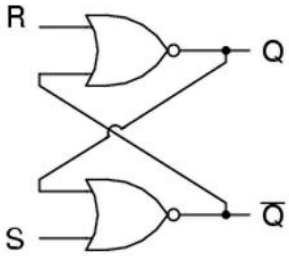
AIM:

Write a winspice code to verify the functionality of NOR based SR Latch

THEORY:

If the set input (S) is equal to logic "1" and the reset input is equal to logic "0." then the output Q will be forced to logic "1". While Q^- is forced to logic "0". This means the SR latch will be set, irrespective of its previous state. Similarly, if S is equal to "0" and R is equal to "1" then the output Q will be forced to "0" while Q^- is forced to "1". This means the latch is reset, regardless of its previously held state. Finally, if both of the inputs S and R are equal to logic "1" then both output will be forced to logic "0" which conflicts with the complementarity of Q and Q^-.





S	R	Q	$\overline{Q}$
0	0	latch	latch
0	1	0	1
1	0	1	0
1	1	0	0

Therefore, this input combination is not allowed during normal operation. Truth table of NOR based SR Latch is given in table. If the S is equal to VOH and the R is equal to VOL, both of the parallel-connected transistors M1 and M2 will be ON. The voltage on node Q^- will assume a logic-low level of VOL = 0.

At the same time, both M3 and M4 are turned off, which results in a logic-high voltage VOH at node Q. If the R is equal to VOH and the S is equal to VOL, M1 and M2 turned off and M3 and M4 turned on.

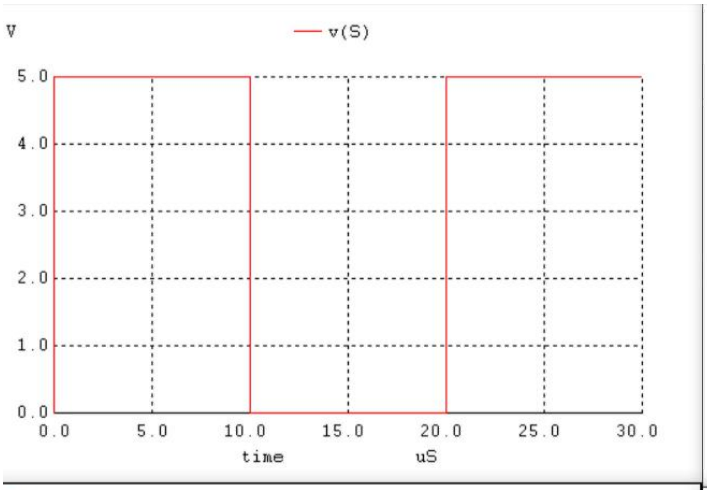
CIRCUIT DIAGRAM:

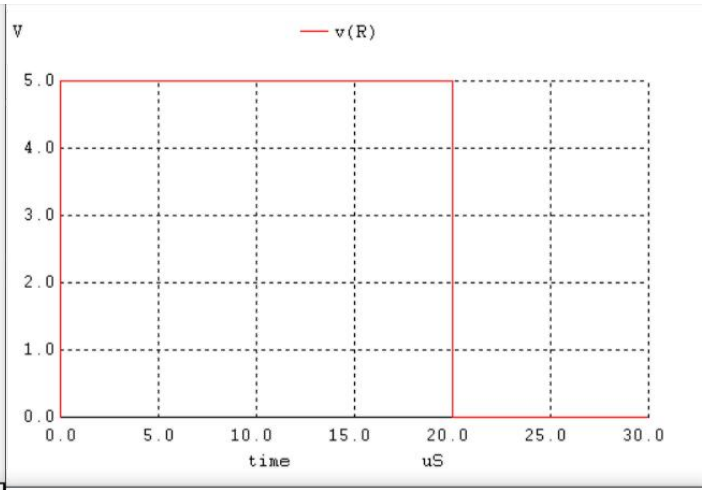
CODE:

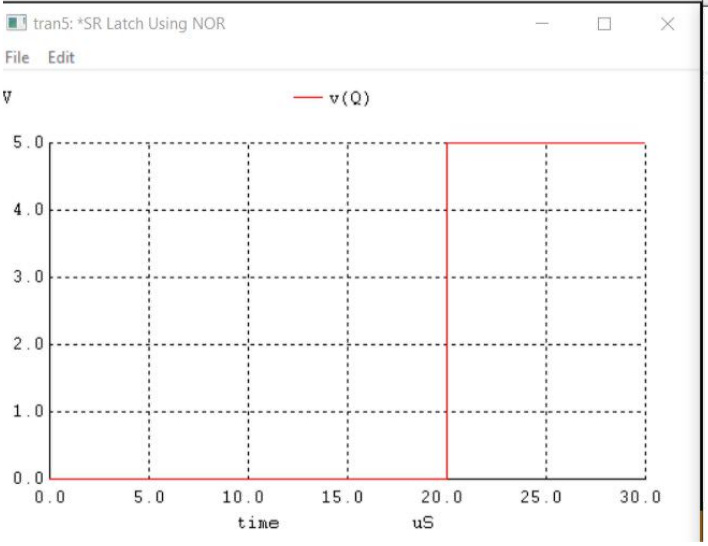
```
*SR Latch Using NOR

.model mynmos nmos Vto=0.8 Kp=50

.model mypmos pmos Vto=-1 Kp=20

.subckt cmosNOR in1 in2 vdd_node out

gnd M1 out in1 gnd gnd mynmos w=1u

l=1u M2 out in2 gnd gnd mynmos w=1u

l=1u

M3 outtemp in1 vdd_node vdd_node mypmos w=1.51u l=1u

M4 out in2 outtemp outtemp mypmos w=1.51u l=1u

.ends cmosNOR


Vdd high 0 5
```

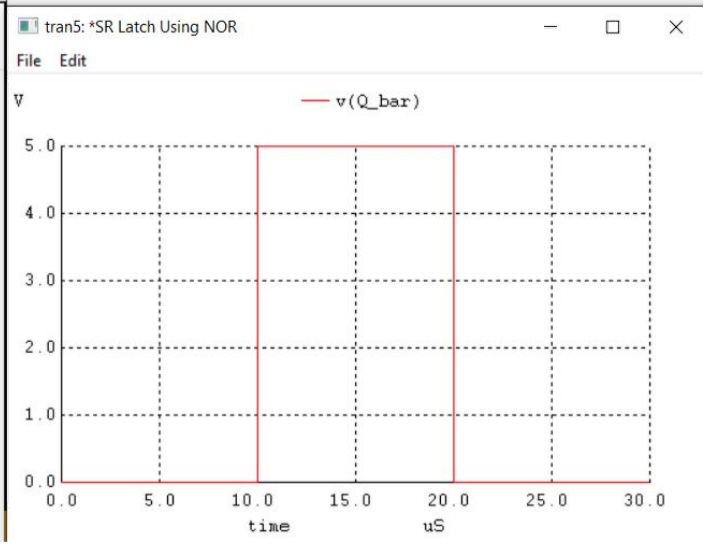
```
Vin1 in1 0 pulse(0 5 1ns 1ns 1ns 10us 20us)
Vin2 in2 0 pulse(0 5 1ns 1ns 1ns 20us 40us)
xd1 in1 out2 high out1 0 cmosNOR
xd2 out1 in2 high out2 0 cmosNOR

.tran 1ns 100us
.control
run
plot v(in1)
plot v(in2)
plot v(out1)
plot v(out2)

.endc
.end
```

Results


V
v(S)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
5.0
10.0
15.0
20.0
25.0
30.0
time
uS


V
v(R)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
5.0
10.0
15.0
20.0
25.0
30.0
time
uS


tran5: *SR Latch Using NOR
File
Edit
V
v(Q)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
5.0
10.0
15.0
20.0
25.0
30.0
time
uS


tran5: *SR Latch Using NOR
File
Edit
V
v(Q_bar)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
5.0
10.0
15.0
20.0
25.0
30.0
time
uS