Design and Simulation of 4-bit Ring Counter using 28nm Technology

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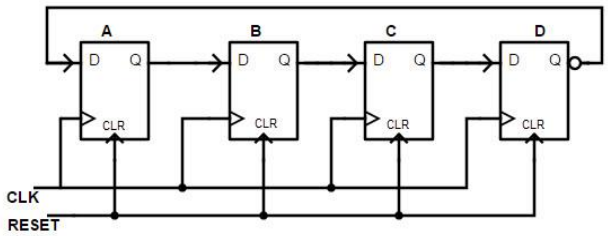
***Abstract*—In the era of technical world, sequential circuits are playing their vital role in the designing of digital system. A counter is a sequential circuit having various applications in the field of embedded system, pattern generations, signal synthesis, Digital to Analog conversion etc. In this paper, an optimized designing mechanism has been deployed to design a high speed, cost effective and low power 4-bit ring counter which can also be extended to higher order ring counter designs.**

I. INTRODUCTION

In sequential circuits, ring counter has made its place in controlling application based on its unique counting sequence. It uses a shift register in which set of flip flop are cascaded to circulate a bit „1" through all the flip flops. Therefore, inputs of flip flops are derived from the output of previous flip flop. and in the case of first flip flop, the output of last stage is given back to first stage. Initially, first stage is required to be set by external input „preset" and other flip flops are cleared. So for 4-bit ring counter, we start with 1000 binary pattern and then 1 circulate as 0100, 0010, 0001 and then again to 1000 binary pattern in next 4 input clock.

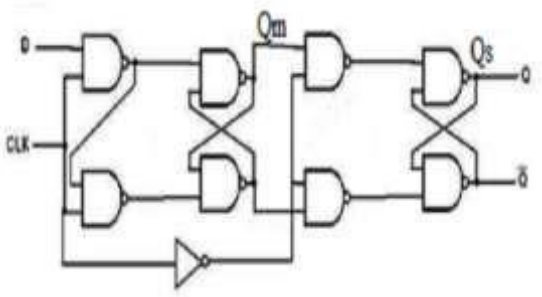


Block diagram of ring counter

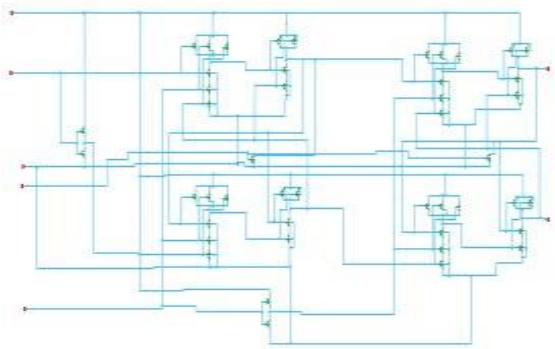
In a 4 bit ring counter the modulus count is 4. Four D flip flops are cascaded with the output of one given as the input to the next and output of the last is given as input to the first. The flip flops are provided with the same clock pulse justifying the synchronous nature of the ring counter. As soon as the clock pulse is first applied to the flip flops one of the flip flops is set at logic 1. This 1 would circulate in the flip flops as per the counting sequence shown in table I

II RING COUNTER DESIGN & WAVEFORM

Ring counter is a synchronous circuit having basic element as flip flop. A flip flop can store data on the rising edge of clock pulse or falling edge respectively called as positive edge and negative edge flip flop. A master slave D flip flop has 8 NAND gates and an inverter as shown in fig.



The same specification of NMOS and PMOS are used in the designing of conventional D flip flop. This master slave D flip-flop is designed using single inverter and eight NAND gates as shown in fig.



Conventional master slave D flip flop

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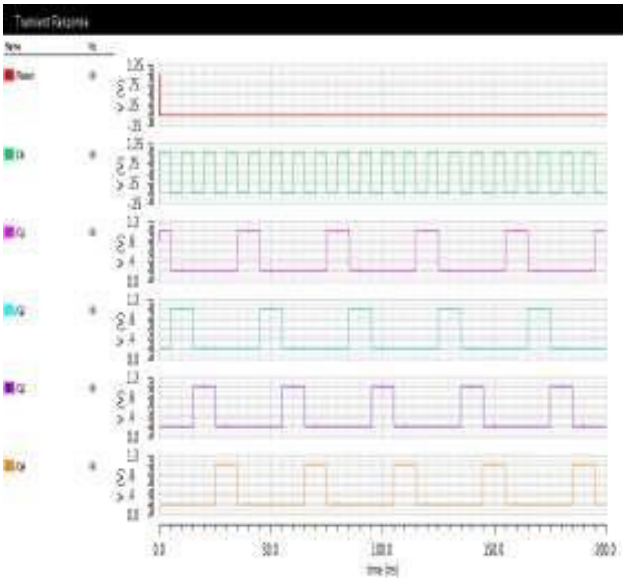
So for 4-bit ring counter, we start with 1000 binary pattern and then 1 circulate as 0100, 0010, 0001 and then again to 1000 binary pattern in next 4 input clock pulses



III REFERENCES

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