DIGITAL ELECTRONICS 20-21

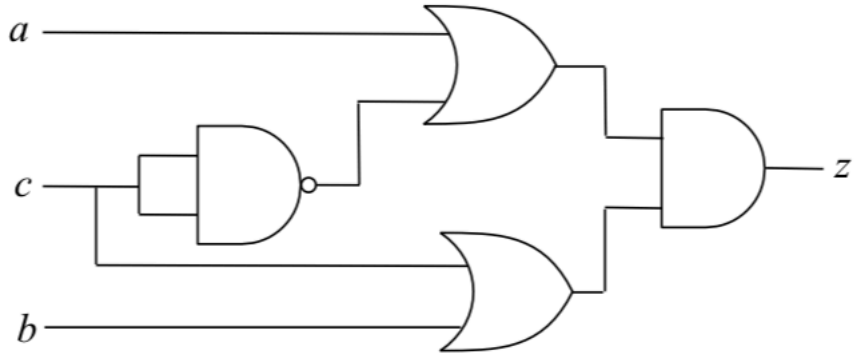
Supervision 2

Lecture: Combinational logic, Hazards, Gate propagation

1) Explain briefly:
   a) The main feature of a combinational logic block.
   b) The difference classes of hazards in digital circuit.
2) A logic function that represents a circuit's output is:

   F = (A + C) • (A' + D') • (B' + C' + D)

   a) Draw the circuit (with a static 0-hazard)
   b) Write down the Karnaugh map for the circuit and show how you can eliminate the hazard.
   c) Draw the timing diagram illustrating the static 0-hazard (assume a delay of 3-time units for each individual inverter and a delay of 5-time units for each AND gate and each OR gate)
3) Each gate in the following circuit has a propagation delay of τ .



   a) Draw a timing diagram showing the output of each gate for a = b = 0; and c initially 0, switching to 1 for a time t ($t >> \tau$), and then returning to 0. Hence show that a static hazard exists. Is it a static 1 or static 0 hazard?
   b) Write down a product of sums expression for from the circuit and use de Morgan's theorem to obtain a sum of products expression for z'.
   c) Draw a Karnaugh map for z' and thus show how the hazard can be removed by adding one more OR gate to the circuit.
4) Implement the function:
   a) F = ∑m (0, 1, 3, 4, 6, 7) by using a 3-to-8 binary decoder and an OR gate.
   b) F = ∑m (1, 2, 3, 5, 6) by using a 3-to-8 binary decoder and an OR gate.
5) Consider the function F = w1'w3'+w2w3'+w1'w2. Use the truth table to derive a circuit for F that uses one 2-to-1 multiplexer and gates.

6) Construct a three input XOR logic function with only 2-to-1 multiplexers and NOT gates.
7) In digital systems it is often necessary to have circuits that can shift the bits of a vector by one or more-bit positions to the left or right. Design a circuit that can shift a four-bit vector W = w3w2w1w0 one-bit position to the right when a control signal Shift is equal to 1. Let the outputs of the circuit be a four-bit vector Y = y3y2y1y0 and a signal k, such that if Shift = 1 then y3 = 0, y2 = w3, y1 = w2, y0 = w1, and k = w0. If Shift = 0 then Y = W and k = 0. (Hint: use 2-to-1 multiplexers)

8) The shifter circuit in Exercise 7 shifts the bits of an input vector by one-bit position to the right. It fills the vacated bit on the left side with 0. A more versatile shifter circuit may be able to shift by more bit positions at a time. If the bits that are shifted out are placed into the vacated positions on the left, then the circuit effectively rotates the bits of the input vector by a specified number of bit positions. Such a circuit is often called a barrel shifter. Design a four-bit barrel shifter that rotates the bits by 0, 1, 2, or 3 bit positions as determined by the valuation of two control signals s1 and s0.
(Hint: use 4-to-1 multiplexers)