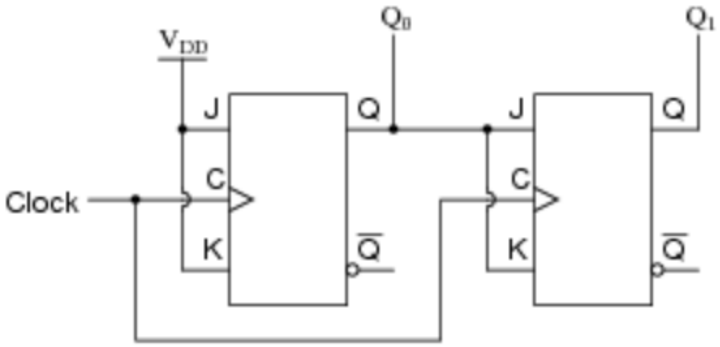
DIGITAL ELECTRONICS 20-21

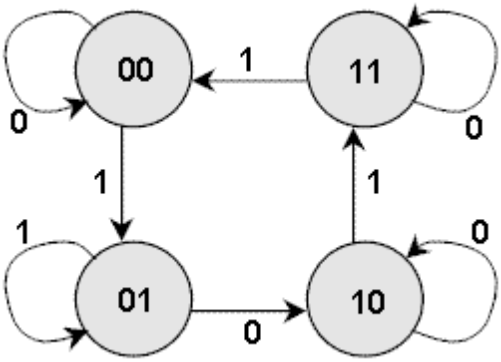
Supervision 3

Lecture: Sequential logic, Synchronous State Machines

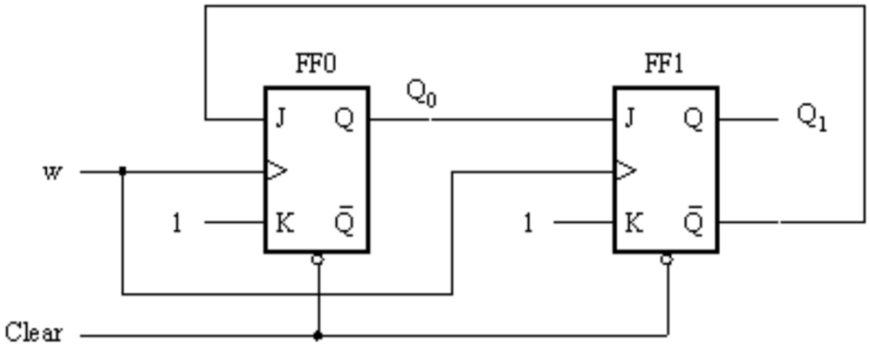
1) State the main features of a synchronous finite state machine (FSM) and describe its two main forms.
2) Flip-Flop Types: SR, JK, D, T. Write down the truth tables, State Diagram and Excitation Table for each one.
3) 2-bit synchronous counter is shown in the figure below:



   a) Draw the time diagram.
   b) Draw the schematic of 4-bit synchronous up-counter (based on the previous diagram).
   c) Draw the schematic of 4-bit synchronous down-counter (based on the previous diagram).
4) Design a synchronous sequential circuit whose state diagram is shown in the following Figure. The type of flip-flop to be use is J-K.
   (Hint: State Table->Excitation Table for JK->Logic Functions->circuit)



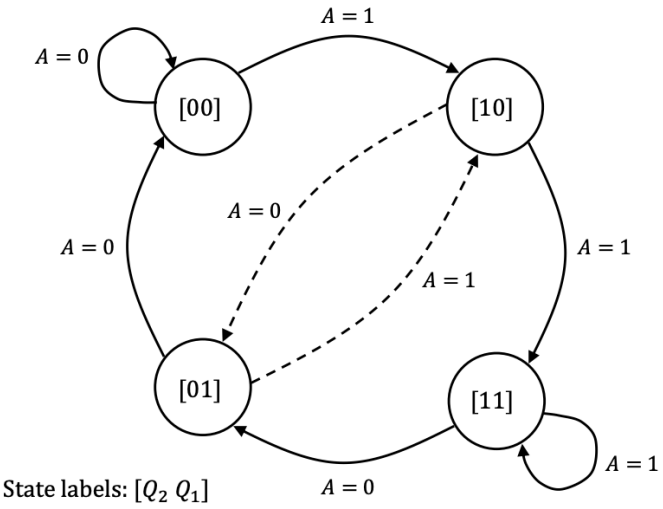
5) Determine the functional behavior of the circuit shown in the following figure.



6) We wish to design a sequence detector circuit, which detects three or more consecutive 1's in a string of bits coming through an input line.
   a) Find the state diagram.
   b) Determine the type of the circuit (Moore or Mealy model).
   c) Tabulate state (or transition) table of sequence detector.
   d) Implement the circuit using D and J-K flip-flops.

7)
   a) Draw the state diagram only (Moore form) for a system with a single input Y, connected to a line carrying serial digital data on which it is desired to detect a sequence Y = 0010. The sequence 00100010 should give an output twice at the instants underlined.
   b) Write down the state table for the state diagram in part (a). Now apply row matching to remove a redundant state. What problem arises in the state table if you do so?
   c) Show how the problem present in the state diagram in part (b) can be overcome by representing the corresponding state diagram in a Mealy form.

8) An FSM with input A has the function described in the following state diagram and is to be implemented using two synchronously clocked D-Type flip-flops as the state registers.



a) Write down the corresponding state table taking into account all transitions in the state diagram, indicated by both solid and dashed lines. Show that the required FSM can be implemented by connecting the D-Type flip-flops in the form of a shift register.

b) For the implementation in Part (a), what effect does increase the clock rate of the D-Type flip-flops have on the likelihood of occurrence of the dashed-line transitions?

c) The two dashed-line transitions have the property of inverting Q1. We now wish to replace both of them with transitions that occur under the same circumstances but instead have the property that Q1 is unchanged. Give the four possible state diagrams satisfying this requirement and, for each state diagram, determine the next-state logic for the D-Type flip-flops.