

BIPOLAR JUNCTION TRANSISTOR [BJT]

Transistor is a three terminal, three layered two junction semiconductor device.

- There are two types of transistors NPN & PNP
- Terminals of the transistor are Emitter, Base & Collector
- Emitter is the source of majority charge carriers, whose function is to emit or supply majority charge carriers to Collector through base region.
- Collector is the destination for majority charge carriers. Collector receives the majority charge carriers emitted by Emitter region.
- Base is the region of transistor which controls or regulates the flow of charge carriers from Emitter to Collector region.

* Doping Profile of transistors region:

- ✓ Emitter region of a transistor is the source of majority charge carriers hence it is heavily doped.
- ✓ Base is the regulator hence it should not accumulate more charge carriers emitted by emitter, Base should only attract the charge carriers of emitter & push them into Collector region therefore "Base is lightly doped".

✓ Collector region is moderately doped.

*) Doping: It is the process of adding impurities to enhance the conductivity of the semiconductor material.

→ By adding trivalent impurity atoms to tetravalent semiconductor material a P-type semiconductor material is formed.

→ By adding pentavalent impurity atoms to tetravalent semiconductor material a N-type semiconductor material is formed.

Trivalent atoms → An atom with three valence electrons ex: Boron

Pentavalent atoms → An atom with five valence electrons ex: Phosphorous

Tetravalent atom → An atom with four valence electrons ex: Silicon & Germanium.

*) Physical size of transistors region:

✓ Collector is the destination of majority charge carriers, it has to accommodate its own charge carriers & as well as has to provide space for majority charges of emitter region hence the "Physical size of collector region is largest" amongst three regions of a transistor.

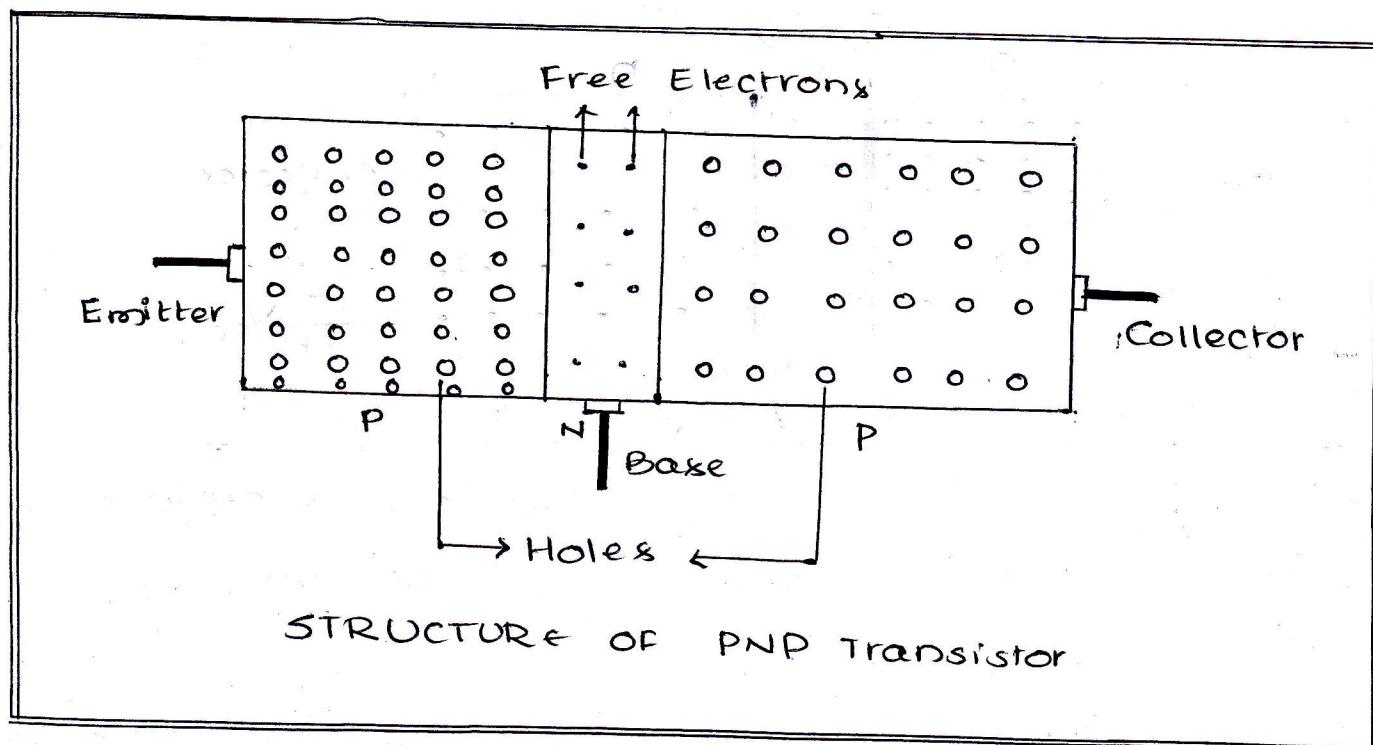
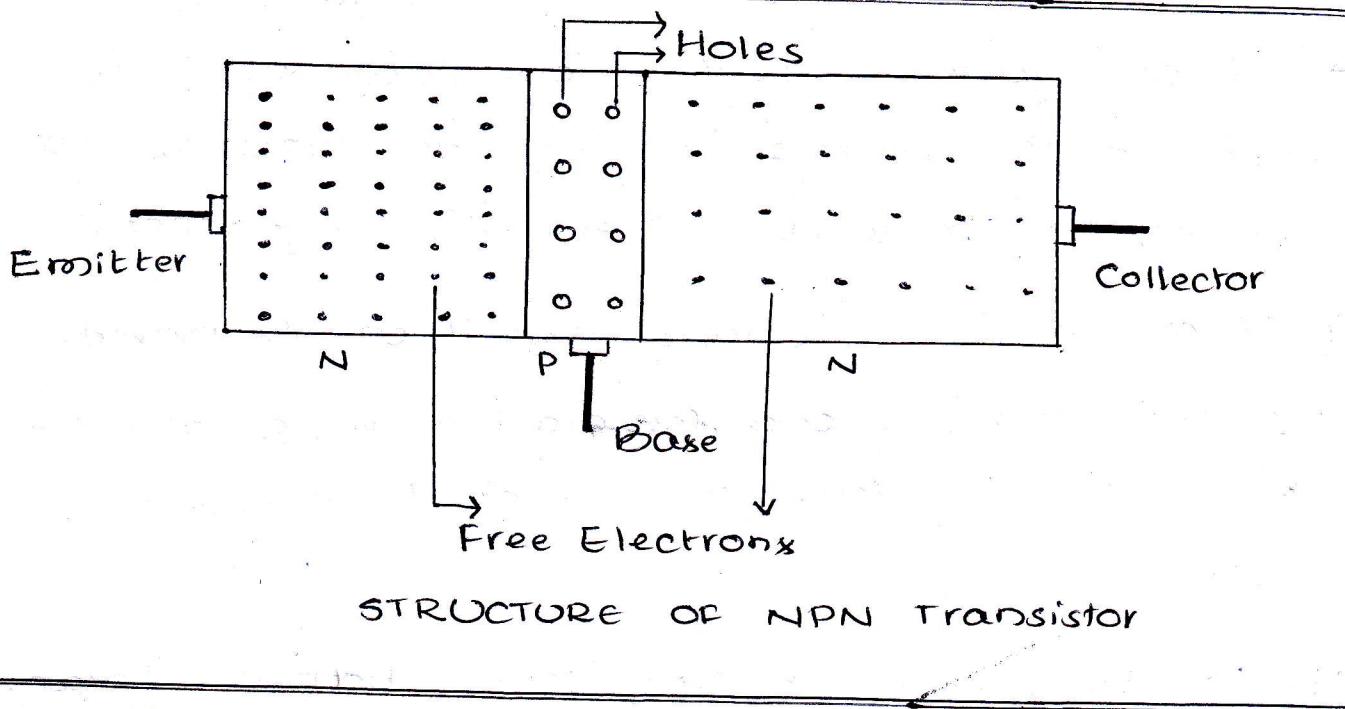
✓ Physical size of base region is very thin, because it should not provide any space to the charges emitted by emitter.

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Base has to attract the majority charges of emitter & immediately push them into collector region.

- Physical size of emitter is moderate.

*> STRUCTURE OF NPN & PNP TRANSISTOR



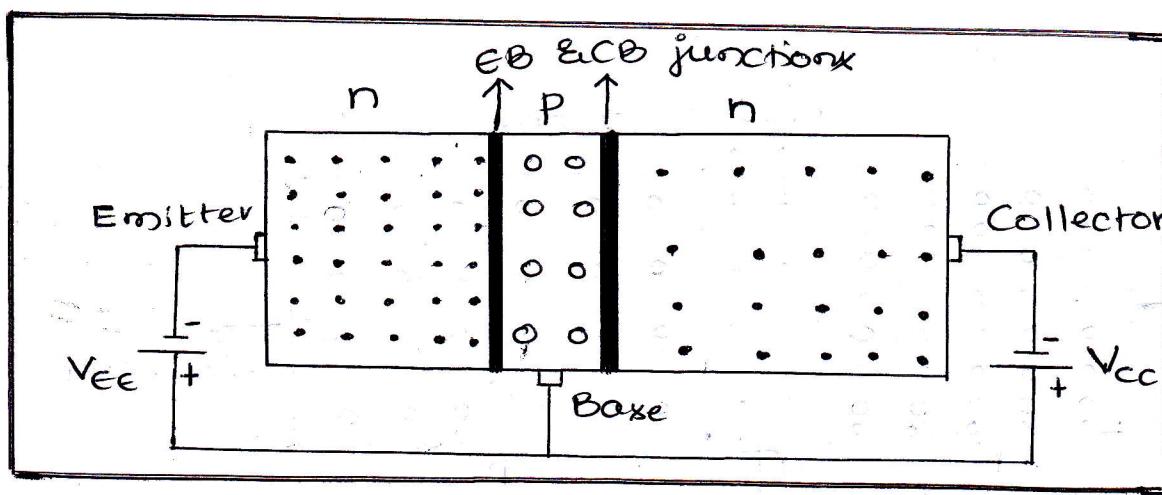
*> Biasing of the transistor:

Biasing: Applying an external power supply or DC source across any electronic device is called biasing.

- Transistor has two junctions, namely, Emitter-Base EB-junction & Collector Base CB-junction.
- If one junction is there one power supply is required to energize it. Transistor requires two external power supplies to energize its junctions.
- If one junction is there then it can be biased in two ways [i.e. once forward biasing & later reverse biasing]. Therefore transistor can be biased in four ways.

Case i> EB-junction & CB-junction both are Forward

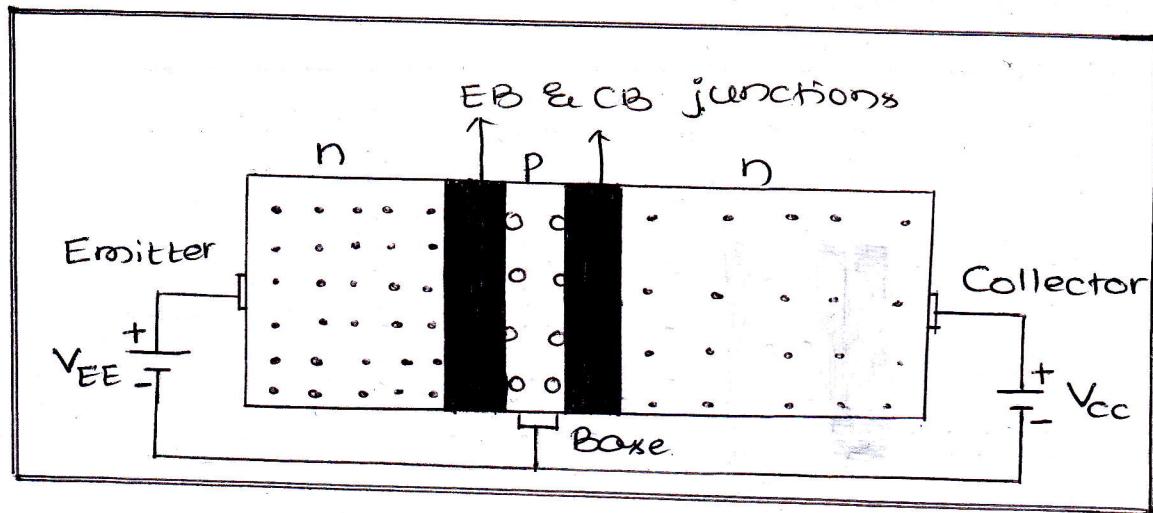
Biased [FB]



- ✓ Depletion layer width of EB junction & CB junction is very narrow because both the junctions are forward biased.
- ✓ Here ^{the} signal is transferred from low resistance EB-junction to low resistance CB-junction.
- This biasing method is called "saturation".

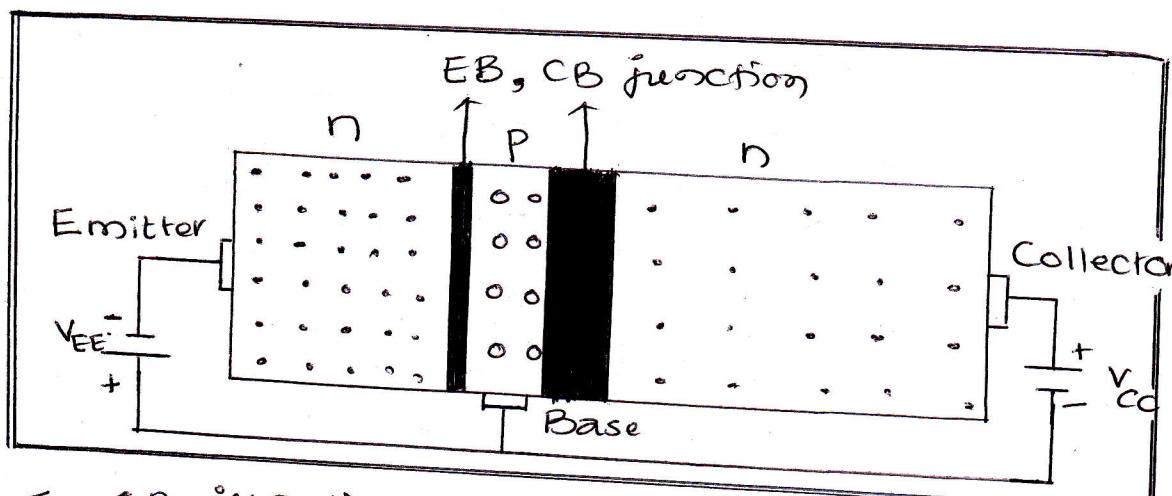
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case ii) EB-junction & CB-junction both are Reverse Biased [RB]



- ✓ Depletion layer width of EB junction & CB junction is very large because both the junctions are reverse biased.
- ✓ Here the input signal is transferred from high resistance EB-junction to high resistance CB-junction.
- This mode of transistor operation is called "cut-off"

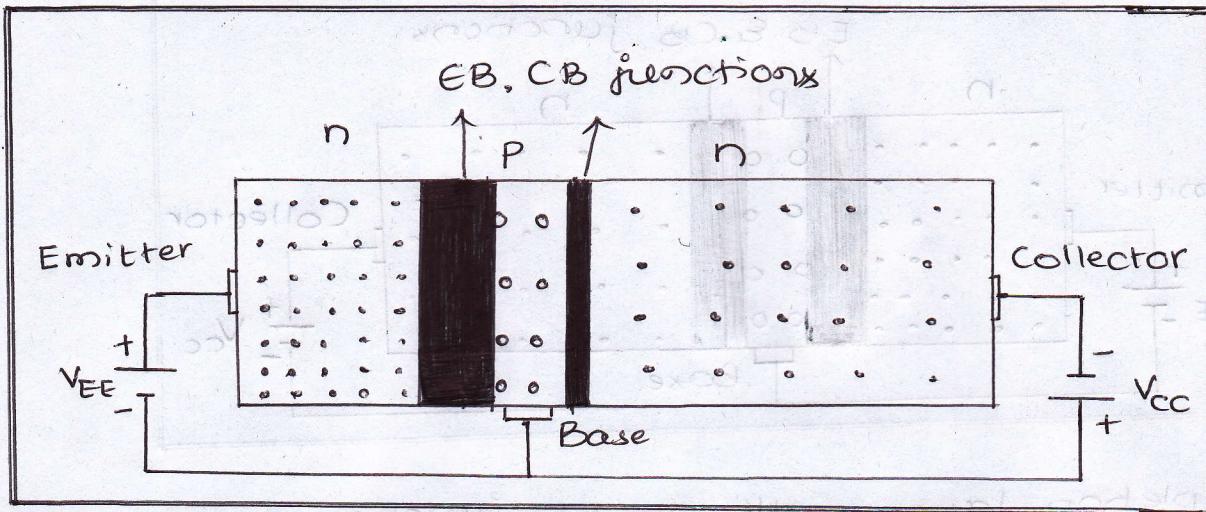
case iii) EB-junction is forward biased & CB-junction is reverse biased.



- ✓ EB-junction \rightarrow narrow depletion layer $\because EB \Rightarrow FB$
- ✓ CB-junction \rightarrow large depletion layer $\because CB \Rightarrow RB$
- ✓ Signal is transferred from low resistance EB-junction to high resistor CB-junction
- This mode of transistor operation is called 'Active'

case iv) EB-junction Reverse Biased & CB-junction Forward Biased.

Forward Biased.

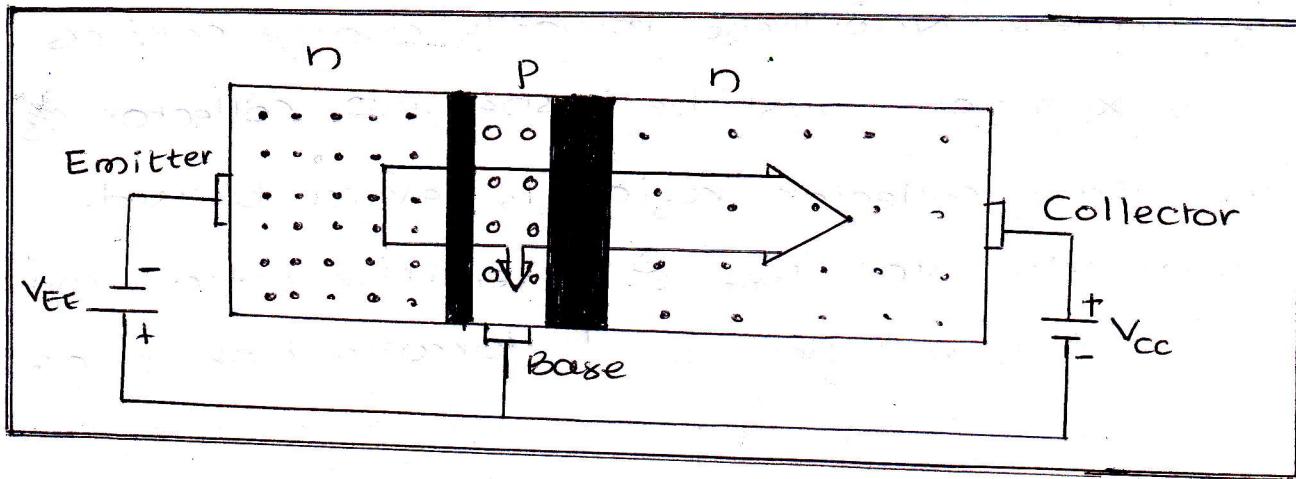


- EB-junction \rightarrow large depletion $\therefore EB \Rightarrow RB$
- CB-junction \rightarrow Narrow depletion layer $\therefore CB \Rightarrow FB$
- ✓ Signal is transferred from high resistance EB-junction to low resistance CB-junction
- This mode of transistor operation is called as "Inverter" mode.

REGION	DOPING PROFILE	PHYSICAL SIZE
Emitter	Heavily	Moderate
Base	Lightly	Thin
Collector	Moderately	Largest

From above four biasing methods, it indicates signal is transferred from one resistor region to other resistor region hence the name TRANSFER + RESISTOR = TRANSISTOR

*> Working of NPN transistor:



*> For the Normal operation of transistor, it is operated under "Active region": i.e Emitter-Base junction is forward biased & Collector base junction is reverse biased.

*> From the above figure, Emitter-Base junction is forward biased by power supply V_{EE} & Collector-Base junction is reverse biased by the power supply V_{CC} .

*> Majority charge carriers of Emitter are free electrons, these free electrons will be pushed into base region by -ve terminal of " V_{EE} " due to force of repulsion.

→ Due to jumping of free electrons from emitter to base constitute the current called as "Emitter Current I_E ".

→ 2% to 5% of emitter's free e^- 's recombine with holes of base region & they stick to base region & constitutes base current " I_B ".

*> 98% to 95% of emitter's free e^- 's which now resided in base region, they jump into collector region due to force of attraction from "+ve terminal of V_{CC} ".

→ When majority charge carriers of emitter region [free δ s] jumps into base they become minority charge carriers. Now these minority charge carriers of base [] region must be pushed into collector region hence Base-collector region is reverse biased. In NPN transistor free δ of emitter which have drifted into base region due to forward biasing of EB-junction must be pushed into collector region. This is achieved by attracting minority charge of base region [i.e free δ of emitter now they are minority charges of base regions] from the of V_{cc} .

→ Drifting of minority charge carriers of base into collector region constitutes 'Collector current I_c '.

→ The recombined 2% to 5% of ^{free} electrons in base region & the drifted 98% to 95% free electrons into collector region together sums to donated majority charges of Emitter region.

Therefore Emitter, Base & Collector currents relation is given by,

$$I_E = I_B + I_C \rightarrow (1)$$

where I_E & I_C are measured in terms of "mA" but I_B is measured in terms of "mA".

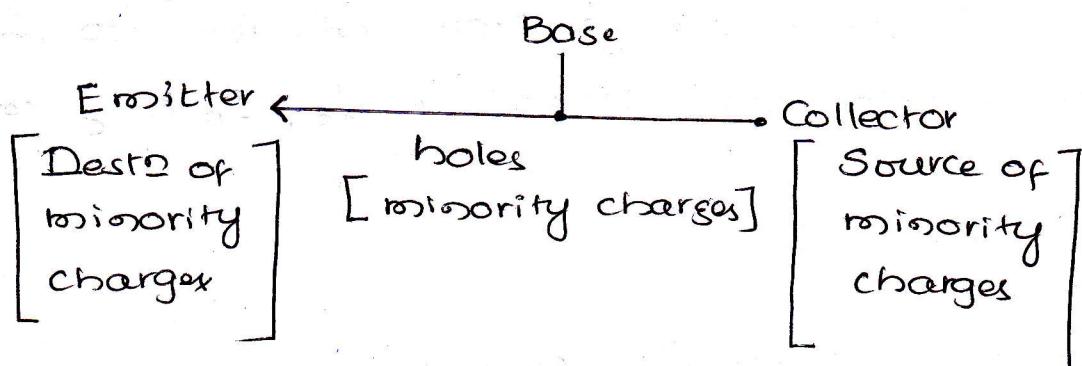
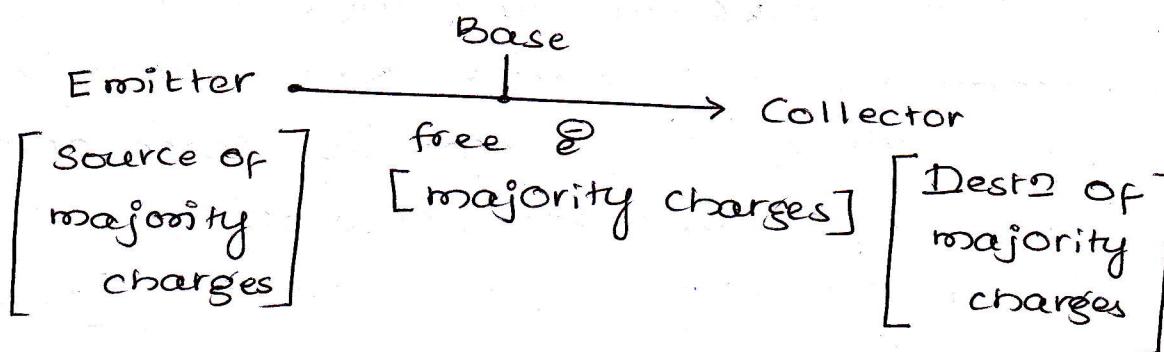
⇒ Due to reverse biasing of collector-base junction minority charge carriers of collector region i.e holes will drift into base region to [] fetch 98% to 95% of free δ

⑨

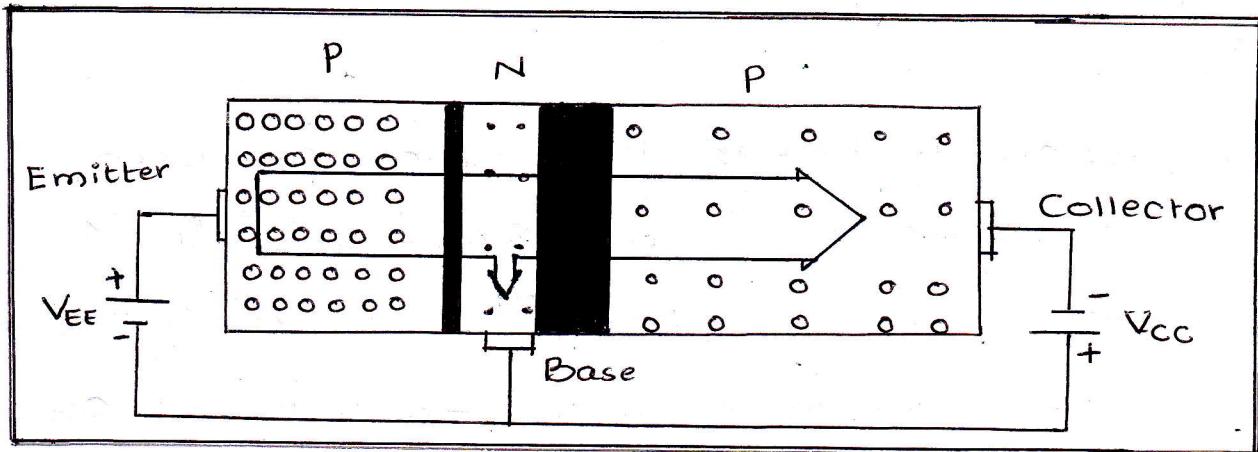
⇒ when the minority charge carriers of collector drifts into base they become majority charge carriers.

⇒ Base region is having holes which have been donated by collector region [98% to 95%] & its own majority charge carriers [2% to 5%] of holes all these holes are attracted by -ve terminal of "+VEE" which connected to Emitter region. Hence the flow of minority charge carriers from Collector to emitter via base.

*⇒ Majority charge carriers will flow from Emitter to collector through base region. Minority minority charge carriers will flow from collector to Emitter via base.



*> Working of PNP transistor:



*> Emitter Base junction is forward biased & Collector base junction is reverse biased by power supplies V_{EE} & V_{CC} . i.e PNP transistor is operated under "Active region".

*> Majority charge carriers of Emitter region, holes will repel by the +ve terminal of V_{EE} hence these charge carriers will get sufficient kinetic energy to drift into base region.

*> When these holes (majority charges) drift into base they become minority charges. Now these minority charges are pushed into collector by force of attraction of -ve terminal of V_{CC} . Hence flow of majority charges [holes] from source[Emitter] to destination[Collector].

*> Now, due to flow charges from emitter, into base & finally to collector region constitute I_E , I_B & I_C respectively,

$$\text{i.e } I_E = I_B + I_C$$

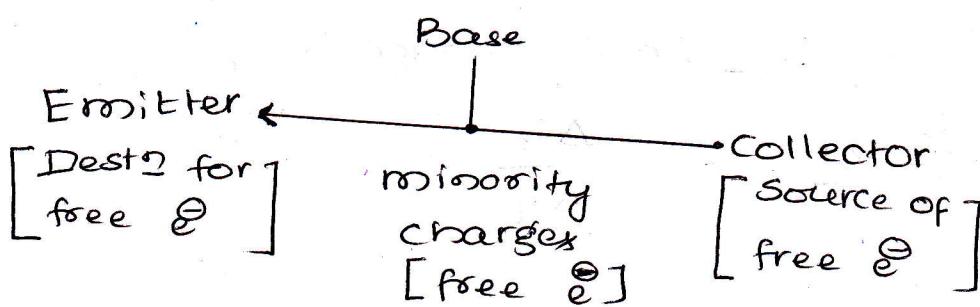
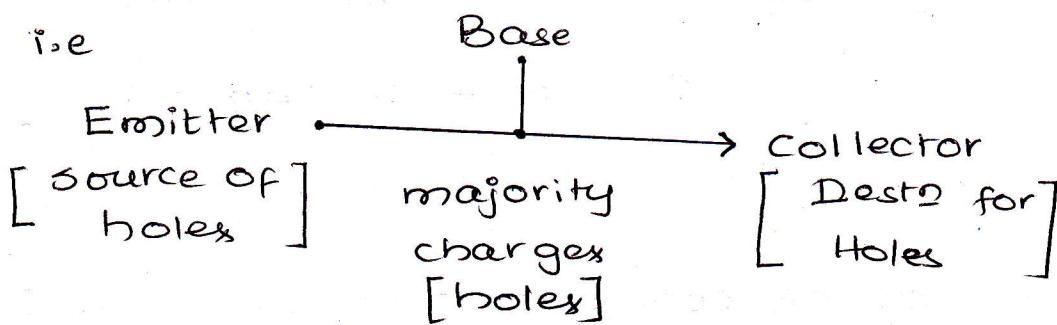
*> And also there will be flow of minority charge carriers [free e^-] from collector to base due reverse biasing of CB-junction.

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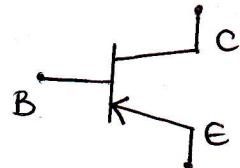
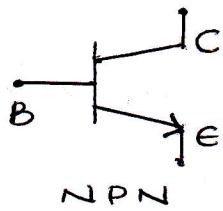
→ When minority charges [free e^-] of collector jumps into base region they become majority charges. Now these majority charges of base region will be drifted into emitter by the terminal V_{EE} .

→ In a PNP transistor holes moves from [holes (majority) charges moves from] Emitter to Collector via base. While free electrons [minority] moves from Collector to Emitter via base.

i.e



#] Symbol of NPN & PNP transistor



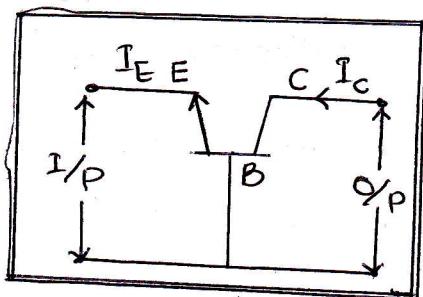
→ Where arrow head indicates directional flow of current

- In NPN transistor current enters emitter terminal. i.e. source of current is collector & desto is emitter

- ✓ In PNP transistor, current leaves the emitter terminal, i.e. Source of current is emitter & dest. is collector.

#> TRANSISTOR CONFIGURATIONS [Connections]

1> Common Base [CB] Configuration:



In CB Configuration,

Base \rightarrow common for both i/p section & o/p section

Emitter \rightarrow I/p terminal

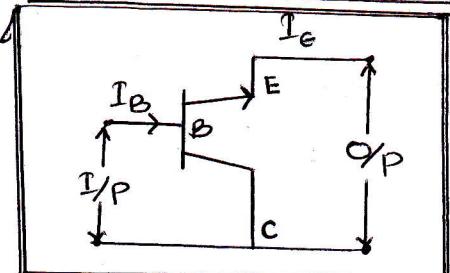
Collector \rightarrow O/p terminal

Input current I_E , Output current I_C

- ✓ Current gain of CB configuration (α): It is the ratio of Collector current I_C [Small change in I_C] to Emitter current I_E [Small change in I_E]

$$\text{i.e } \alpha = \frac{I_C}{I_E} \text{ or } \alpha = \frac{\Delta I_C}{\Delta I_E}$$

2> Common Collector [CC] Configuration:



In CC Configuration,

Base \rightarrow I/p terminal, Emitter \rightarrow O/p terminal

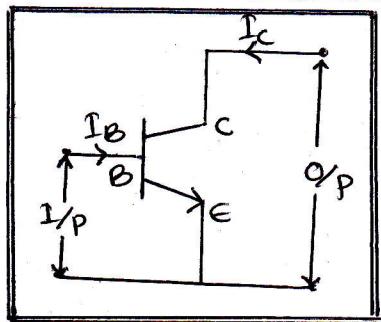
Collector \rightarrow common for both i/p section & o/p section

I/p current "I_B", O/p current "I_E"

- ✓ Current gain of CC configuration (γ): It is the ratio of Emitter current I_E [or small change in I_E] to Base current I_B [or small change in I_B]

$$\text{i.e } \gamma = \frac{I_E}{I_B} \text{ or } \gamma = \frac{\Delta I_E}{\Delta I_B}$$

3) Common Emitter [CE] Configuration:



In CE configuration,

Base \rightarrow I/p terminal, Emitter \rightarrow Common
Collector \rightarrow O/p terminal.

$I_B \rightarrow$ I/p Current, $I_C \rightarrow$ O/p Current,

- ✓ Current Gain of CE Configuration (β): It is the ratio of collector current I_C [small change in I_C] to base current I_B [small change in I_B].

$$\text{i.e. } \beta = \frac{I_C}{I_B} \text{ or } \beta = \frac{\Delta I_C}{\Delta I_B}$$

*>> Range of α is 0.95 to 0.99

*>> Range of B is 20 to 500

*>> Range of γ is 21 to 501 hence $\gamma \approx B$

#] RELATION $B/\alpha \propto \beta$

$$\text{O.K.T} \quad \alpha = \frac{I_C}{I_E} \text{ or } \frac{1}{\alpha} = \frac{I_E}{I_C} \rightarrow (1)$$

$$\beta = \frac{I_C}{I_B} \text{ or } \frac{1}{\beta} = \frac{I_B}{I_C} \rightarrow (2)$$

From basic relations of transistor currents,

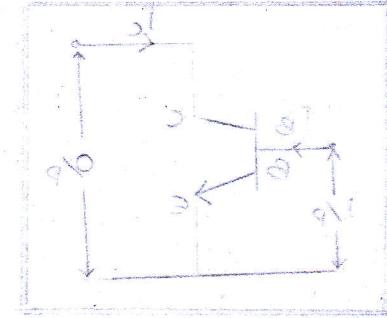
$$I_E = I_B + I_C \rightarrow (3)$$

divide the eqn (3) by I_C

[P.T.O]

$$eq2(3) \Rightarrow \frac{I_E}{I_C} = \frac{I_B}{I_C} + 1 \rightarrow (4)$$

From eqs (1) & (2)



$$eq2(4) \Rightarrow \frac{1}{\alpha} = \frac{1}{\beta} + 1 \rightarrow (5)$$

Case i) α in terms of β

consider eq2 (5)

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1$$

$$\text{or } \frac{1}{\alpha} = \frac{1+\beta}{\beta}$$

$$\boxed{\alpha = \frac{\beta}{\beta+1}}$$

case ii) β in terms of α

Consider eq2 (5)

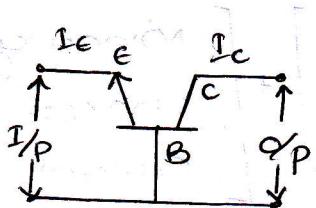
$$\frac{1}{\alpha} = \frac{1}{\beta} + 1 \quad \text{or} \quad \frac{1}{\alpha} - 1 = \frac{1}{\beta}$$

$$\frac{1}{\beta} = \frac{1-\alpha}{\alpha} \quad \text{or}$$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}}$$

#] I_c [Collector Current] expression for a transistor

in CB mode



$$\text{Collector Current} = \text{Majority charges current} + \text{Minority charges current}$$

$$\downarrow$$

$$\alpha I_E$$

$$\downarrow$$

$$I_{\text{LEAK}}$$

$$\therefore I_c = \alpha I_e + I_{\text{LEAK}}$$

In CB mode, I_{LEAK} is the current flowing from collector to base when emitter (i_p terminal) is not considered (open)

$$\text{i.e } I_{\text{LEAK}} = I_{\text{CBO}}$$

$$\therefore I_c = \alpha I_e + I_{\text{LEAK}}$$

or $I_c = \alpha I_e + I_{\text{CBO}}$

where $I_e = I_B + I_C$

$$\Rightarrow I_c = \alpha [I_B + I_C] + I_{\text{CBO}}$$

$$\underline{I_c = \alpha I_B + \underline{\alpha I_C} + I_{\text{CBO}}}$$

or $I_c - \alpha I_c = \alpha I_B + I_{\text{CBO}}$

$$I_c [1 - \alpha] = \alpha I_B + I_{\text{CBO}}$$

$$\Rightarrow I_c = \left[\frac{\alpha}{1-\alpha} \right] I_B + \left[\frac{1}{1-\alpha} \right] I_{\text{CBO}}$$

or

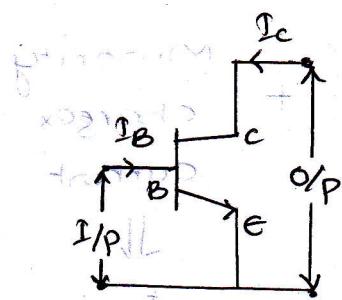
$$I_c = \beta I_B + (\beta + 1) I_{\text{CBO}}$$

where $\frac{\alpha}{1-\alpha} = \beta$ &
 $\frac{1}{1-\alpha} = \beta + 1$

Hence I_c in CB mode

#] Collector current [I_C] expression for a transistor

in CE mode



$$\text{Collector current} = \begin{bmatrix} \text{Majority} \\ \text{charge} \\ \text{current} \end{bmatrix} + \begin{bmatrix} \text{Minority} \\ \text{charge} \\ \text{current} \end{bmatrix}$$

$$\downarrow$$

$$\beta I_B$$

$$\downarrow$$

$$I_{\text{LEAK}}$$

$$\downarrow$$

$$I_{\text{CEO}}$$

$$\therefore I_C = \beta I_B + I_{\text{CEO}} \rightarrow (*)$$

from eqn 8 ⚫ & (*)

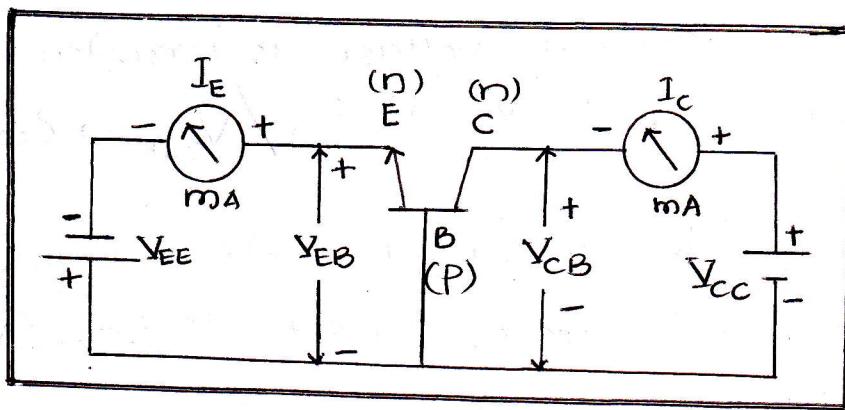
$$I_{\text{CEO}} = (\beta + 1) I_{\text{CBO}}$$

\therefore Leakage current in CE mode is larger CB mode.

※ Transistor is called as Bipolar junction Transistor because in this device flow current is due to both majority & minority charges i.e. due to both free electrons & holes.

#] TRANSISTOR CHARACTERISTICS:Need for characteristics

- To understand behaviour of the device
- To determine electrical parameter ratings [like current rating, voltage critical value]
- To find relation b/w voltage & current.

[*] Transistor characteristics in CB mode:* CIRCUIT DIAGRAM

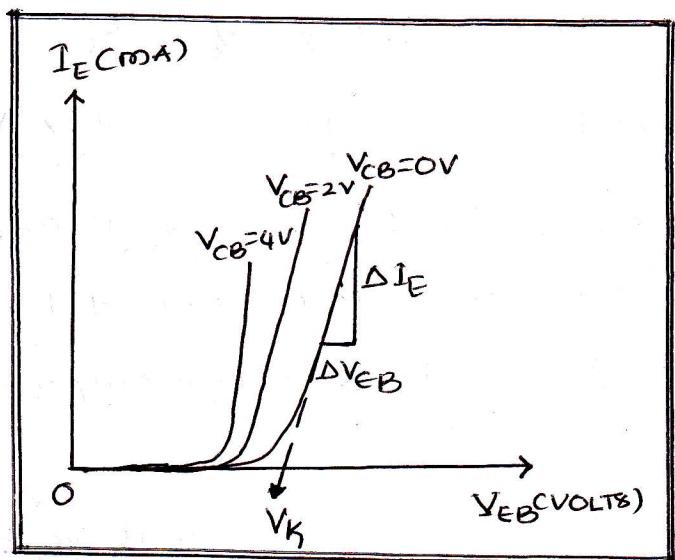
- *) Transistor used in above circuit is n-p-n & which configured in CB mode.
- **) Transistor is biased in Active region. i.e. EB-junction is forward biased by the power supply " V_{EE} " & CB-junction is reverse biased by the power supply " V_{CC} ".
- **) Input current " I_E " is measured in terms of milliAmps by using the current meter "mA" & I_C is measured by using the current meter "mA" & which signifies output current.
- **) In the above circuit diagram, V_{EB} is input voltage of CB mode transistor & V_{CB} is output voltage.

→ Transistor has two sets of electrical parameters as Input Current [I_E] & Input voltage [V_{EB}] and Output Current [I_C] & Output voltage [V_{CB}]. Therefore characteristics of the transistor are divided into two parts, such as Input characteristics [Input voltage Vs Input current] & Output characteristics [Output voltage Vs Output current]

i) Input characteristics of transistor in CB mode:

Defn: It is the graph plotted between variations in input Voltage with respect to changes in respective input current value when Output voltage is maintained with constant value. [i.e. $V_{in} \propto I_{in} / V_{out} \rightarrow \text{const}$]

For CB mode → It is the graph plotted between variations in voltage drop across emitter to base (V_{BE}) versus input current " I_E " in XY-plane when output voltage drop across Collector to base V_{CB} is kept as constant. [i.e. $V_{EB} \propto I_E / V_{CB} \rightarrow \text{constant}$]



→ Since the Emitter-Base junction is forward biased, the input characteristics resemble the forward V-I characteristics of a semiconductor Diode. Hence there exists a knee voltage [V_k]

→ Below the knee voltage

the emitter current I_E is almost zero. Above the knee voltage, I_E increases very sharply.

→ A slight increase in V_{EB} produces large increase in I_E

→ For the increased values, output voltage leads to upward shift [slopes] in the curves as shown in the graph [for different values of $V_{CB}(\uparrow)$ new curves bend towards y-axis]

*> Input Resistance in CB mode:

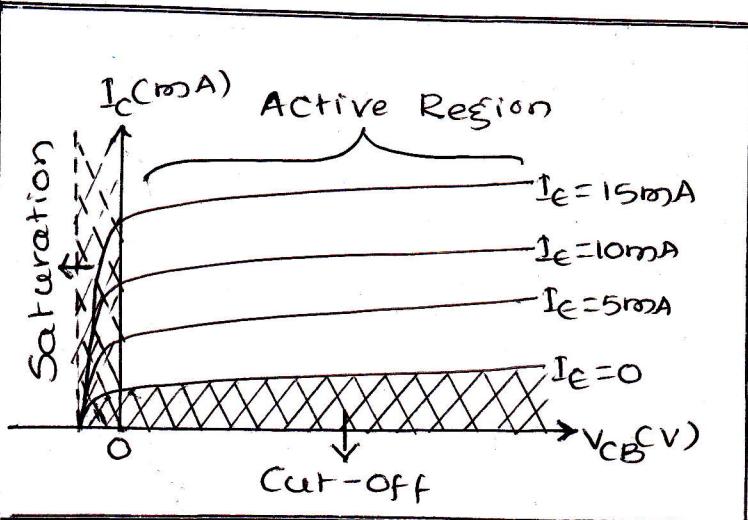
- It is the ratio of small change in Emitter to Base voltage [V_{EB}] to small change in Emitter current [I_E] for a constant value of V_{CB} .

i.e
$$R_{in} = \frac{\Delta V_{EB}}{\Delta I_E} / V_{CB} \rightarrow \text{constant}$$

ii) Output characteristics in CB-mode:

Defn: It is the graph plotted between variations in output voltage to ^{respective} variations in output current when the input current is maintained with a constant value.
[i.e V_{out} vs I_{out} / $I_{in} \rightarrow \text{constant}$]

For CB mode: It is the graph plotted between variations in Collector to Base voltage [V_{CB}] & respective changes in Collector current [I_C] for a constant value of input current [I_E] in XY-plane. [V_{CB} vs I_C / $I_E \rightarrow \text{constant}$]



- Curves show that, I_C is almost independent of V_{CB} & almost equal to I_E
- The Collector current I_C flows even when V_{CB} is zero

The output characteristics can be divided into three regions

i) Active region. ii) Saturation & iii) Cut-off region

•> Active Region: The region in which EB-junction is forward biased & CB-junction reverse biased.

Output current (I_C) ^{is} independent of output voltage V_{CB} .

The flat of the graph indicates Active Region.

•> Saturation Region: It is the region in which EB & CB both junctions are forward biased. Linear current increasing part of the graph is called as "Saturation"

•> Cut-off Region: It is the region in which both EB & CB junctions acts like reverse biased. The region of output characteristics below $I_C = 0A$ is called as Cut-off region.

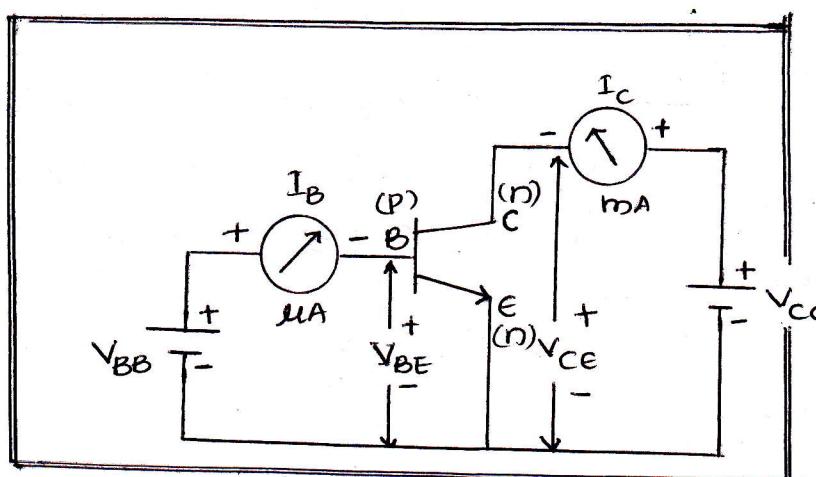
※※ Output resistance in CB mode:

It is the ratio of small change in Collector to Base voltage $[\Delta V_{CB}]$ to small change in collector current $[\Delta I_C]$ for constant input current (I_E).

$$\text{i.e } R_{out} = \frac{\Delta V_{CB}}{\Delta I_C} \quad / \quad I_E \rightarrow \text{constant}$$

[*] CE characteristics of a Transistor:

*> CIRCUIT DIAGRAM:



V_{CE} → O/P voltage across C & E terminals

I_B → micro Ammeter

I_c → milli Ammeter

V_{BB} & V_{CC} → External Power Supplies

V_{BE} → I/p Voltage across EB-junction

**> The transistor used in the above circuit is npn & which configured in CE mode.

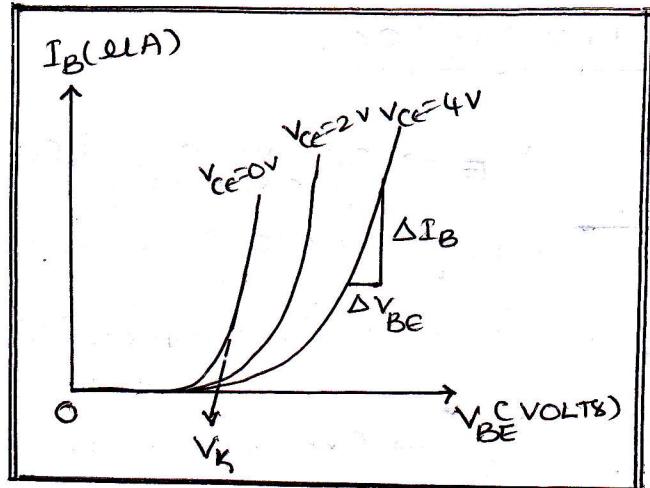
**> Transistor is biased in Active region i.e. EB-junction is forward biased by "V_{BB}" & CB-junction is reverse biased by "V_{CC}".

**> Where I_B is input current measured in terms of "mA" & I_c is output current measured in terms of "mA"

•> Above circuit depicts four electrical parameters. I_B & V_{BE} as input parameters and I_c & V_{CE} as output parameters. Therefore characteristics are divided into input characteristics [V_{BE} vs I_B] and output characteristics [V_{CE} & I_c].

i> Input characteristics of Transistor in CE mode.

Defn: It is the graph plotted between input voltage [V_{BE}] variations and respective changes in input current [I_B] when output voltage [V_{CE}] with a constant value. { i.e. V_{BE} vs I_B / $V_{CE} \rightarrow \text{constant}$ }



→ CE input characteristics also resemble the V-I characteristics of a forward biased diode

→ When V_{BE} is below knee voltage V_K , the base current I_B is negligibly small.

→ Above the knee voltage I_B increases sharply with the increase in V_{BE} .

→ Increase in V_{CE} shift the new input response curves towards Y-axis hence new curves experience "down shift" [for different higher & constant values of V_{CE}]

*> Input resistance in CE mode:

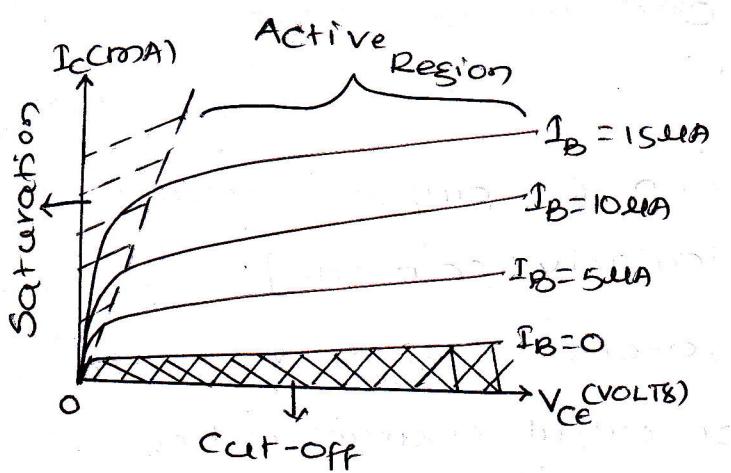
Defn: The ratio of small change in the base emitter voltage [ΔV_{BE}] to the corresponding change in the base current [ΔI_B] at a constant collector to emitter voltage (V_{CE}).

$$\text{i.e } R_{in} = \frac{\Delta V_{BE}}{\Delta I_B} \quad / V_{CE} \rightarrow \text{constant}$$

ii) Output characteristics in CE-mode:

Defn: It is the graph plotted between output voltage V_{CE} and output current I_C when input current I_B is at a constant value.

i.e $[V_{CE} \text{ vs } I_C] / I_B \rightarrow \text{constant}$ in XY-plane.



→ when I_B is zero, a very small collector current due to collector to emitter leakage current I_{CEO} flows. The CE output characteristics can also be divided into three regions.

※※ Saturation Region: The region in which both the junctions i.e. $E_B \& C_B$ are forward biased. Linearly increasing part of the graph is called Saturation Region.

※※ Cut-off Region: The region in which both the junctions i.e. $E_B \& C_B$ are reverse biased. Region of the graph $I_B = 0$ depicts cut-off.

※※ Active Region: The region in which E_B -junction is forward biased & C_B -junction is reverse biased, indicates Active Region. Flat part of the graph is called "Active". In Active Region output current [I_C] is independent of output voltage [V_{CE}].

※※ Output Resistance in CE mode:

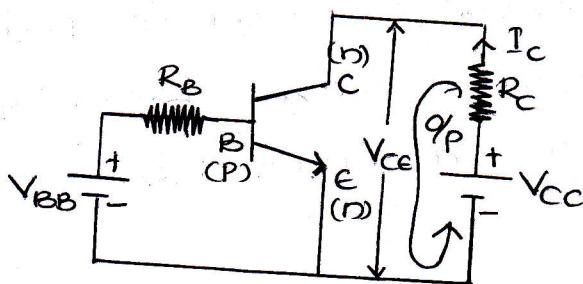
It is the ratio of small change in output voltage [ΔV_{CE}] to small change in output current (ΔI_C) when input current (I_B) is constant.

$$\text{i.e. } R_{out} = \frac{\Delta V_{CE}}{\Delta I_C} / I_B \rightarrow \text{constant}$$

#] DC LOAD LINE & OPERATING POINT

*> DC LOAD LINE:

- > It is a straight line drawn on output characteristics of the transistor. [particularly ce mode]
- > It is the line joining co-ordinates on x-axis & y-axis in xy-plane of output characteristics.



Apply KVL to output loop

$$\text{i.e } V_{CC} = I_C R_C + V_{CE}$$

$$\text{or } V_{CC} - V_{CE} = I_C R_C$$

$$I_C = \left[-\frac{1}{R_C} \right] V_{CE} + \frac{V_{CC}}{R_C} \rightarrow (1)$$

W.K.T equation of a straight line is $Y = mx + c \rightarrow (2)$

by comparing eqns (1) & (2), eqn (1) resembles equation of straight line, co-ordinates of this straight line are,

case i) when $I_C = I_{C\max}$ then $V_{CE} = 0$

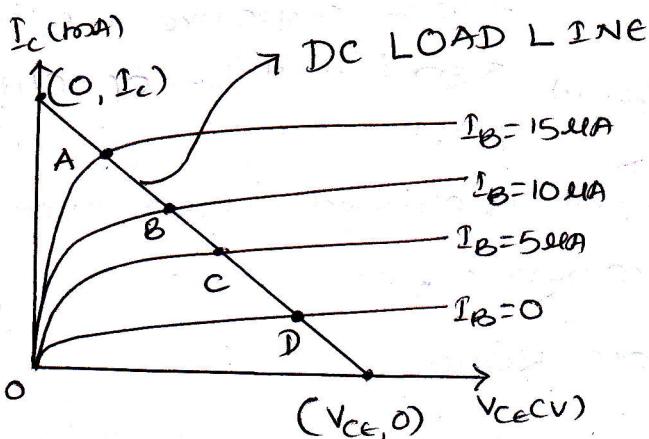
$$\therefore \text{eqn (1)} \Rightarrow I_{C\max} = \frac{V_{CC}}{R_C}$$

i.e co-ordinates on y-axis of output characteristics is $(0, y)$ i.e $[0, \frac{V_{CC}}{R_C}]$

case ii) when $V_{CE} = V_{CE_{max}}$ then $I_C = 0$

$$\therefore \text{eqn (1)} \Rightarrow V_{CE_{max}} = V_{CC}$$

i.e. co-ordinates on x-axis of output characteristics
is point $(x, 0)$ i.e. $[V_{CC}, 0]$



» DC LOAD LINE is straight line joining the points between $(V_{CE}, 0)$ (Cut-off voltage) and $(0, I_c)$ [Saturation current]

OPERATING POINT (Q):

The point of intersection between DC load line & output characteristics of a transistor is called as operating point.

- » Operating point depicts transistors mode of operation.
- » In the above diagram points A, B, C & D indicates operating point.

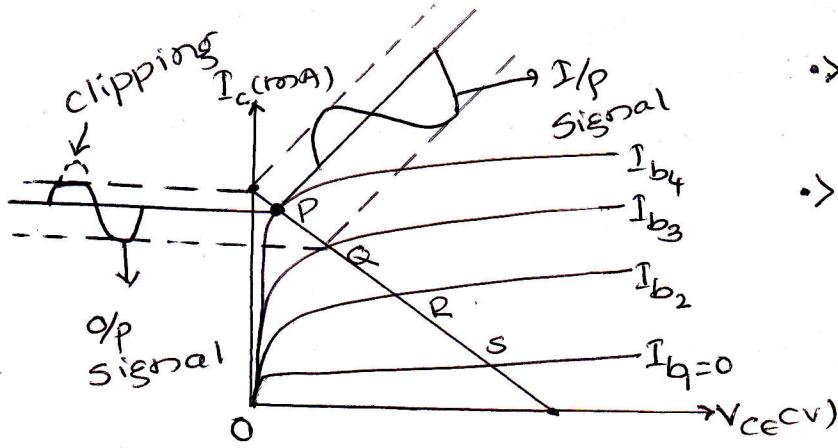
Point A \rightarrow Saturation mode

Point D \rightarrow Cut-off mode &

Points B & C \rightarrow Active mode of operation.

#> SELECTION OF OPERATING POINT :

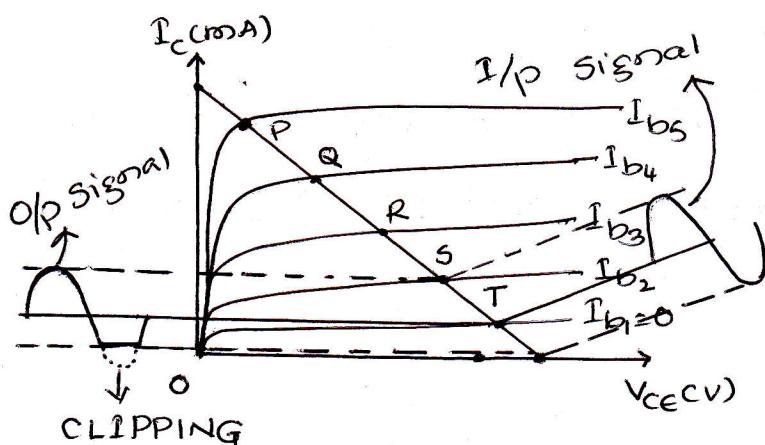
i) Operating Point in Saturation Region:



- > when P is selected as operating point
- > when an sinusoidal signal is applied as input signal, whose response i.e o/p signal will be of clipped part.

•> +ve peak of output signal is clipped when operating point is selected in saturation region.

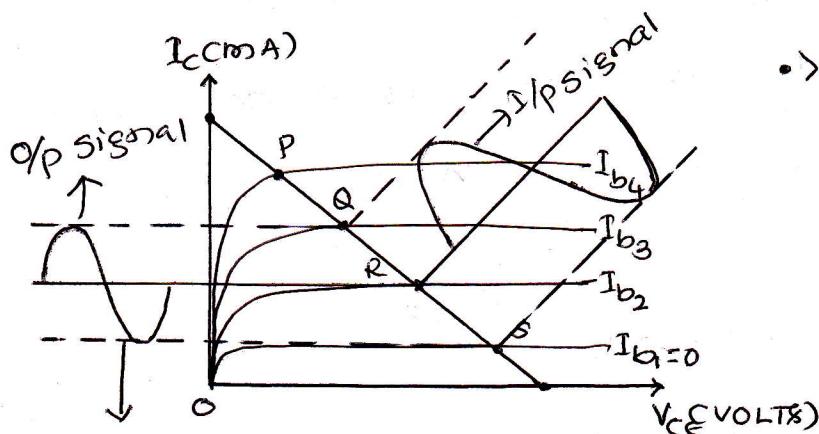
ii) Operating point in cut-off Region:



- > when point 'T' is selected as operating point i.e in cut-off region
- > when operating point is selected in "cut-off region", -ve peak of the output signal is clipped hence

the output signal is 'distorted'.

iii) Operating point in Active Region:



NO clipping
hence
No Distortion

- > when the point 'R' is selected as operating point i.e in Active Region, then the output signal no clipping & hence no distortion.

•> Active mode of transistor operation is best preferable for "Amplification".

LIST OF FORMULAE

(27)

i) $I_E = I_B + I_C$

ii) $\alpha = \frac{I_C}{I_E}$

iii) $\beta = \frac{I_C}{I_B}$

iv) $\beta = \frac{\alpha}{1-\alpha}$

v) $\alpha = \frac{\beta}{\beta+1}$

vi) Collector current expression for CB-mode is

$$I_C = \left[\frac{\alpha}{1-\alpha} \right] I_B + \left(\frac{1}{1-\alpha} \right) I_{CBO} \quad \text{where } I_{CBO} \rightarrow \text{Leakage Current}$$

or

Current in
AC mode
CB mode

$$I_C = \beta I_B + (\beta+1) I_{CBO}$$

vii) Collector current expression for CE-mode is,

$$I_C = \beta I_B + I_{CEO}$$

$I_{CEO} \rightarrow$ Leakage Current

viii) Leakage current relations between CE & CB mode is,

$$I_{CEO} = (\beta+1) I_{CBO}$$

1) Calculate the value of I_C , I_E & β_{dc} for a transistor with $\alpha = 0.99$ and $I_B = 110\text{mA}$

Sol Ω : Given $\alpha = 0.99$, $I_B = 110\text{mA}$ $I_C = ?$, $I_E = ?$ & $\beta = ?$

$$\text{W.K.T } \beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{1-0.99}$$

$$\beta = 99$$

$$\text{Hence } \beta = \frac{I_C}{I_B} \text{ or } I_C = \beta I_B = (99)(110 \times 10^{-6})$$

$$I_C = I_B \beta = 10.89\text{mA}$$

$$I_E = I_B + I_C = (0.11 \times 10^{-3}) + (10.89 \times 10^{-3})$$

$$I_E = 11\text{mA}$$

2) For a certain transistor circuit, $I_C = 12.42\text{mA}$ & $I_B = 200\text{mA}$, find i) I_E ii) α & β of a transistor

Sol Ω : $I_C = 12.42\text{mA}$, $I_B = 200\text{mA}$, $I_E = ?$, $\alpha = ?$ & $\beta = ?$

$$\rightarrow I_E = I_B + I_C = [0.2 \times 10^{-3}] + [12.42 \times 10^{-3}]$$

$$\therefore I_E = 12.62\text{mA}$$

$$\rightarrow \alpha = \frac{I_C}{I_E} = \frac{12.42 \times 10^{-3}}{12.62 \times 10^{-3}}$$

$$\therefore \alpha = 0.9841$$

$$\rightarrow \beta = \frac{I_C}{I_B} = \frac{12.42 \times 10^{-3}}{0.2 \times 10^{-3}} = 62.1$$

$$\beta \approx 62$$

(29)

3> The Collector current in a transistor is 5mA. If $\beta = 140$ and base current is 35mA determine leakage current I_{CBO} .

Sol: Given $I_C = 5\text{mA}$, $I_B = 35\text{nA}$ & $\beta = 140$ $I_{CBO} = ?$

$$\text{N.K.T } I_C = \beta I_B + (\beta+1) I_{CBO}$$

$$\text{or } I_{CBO} = \frac{(I_C - \beta I_B)}{(\beta+1)}$$

$$= \frac{(5 \times 10^{-3}) - (140 \times 35 \times 10^{-3})}{141}$$

$$= \frac{(5 \times 10^{-3}) - 4.9 \times 10^{-3}}{141} = \frac{(0.1) \times 10^{-3}}{141}$$

$$\therefore I_{CBO} = 0.709\text{nA}$$

4> For a silicon transistor $\alpha = 0.995$, emitter current is 10mA and leakage current I_{CO} is 0.5nA Find I_C , I_B , β & I_{CEO}

Sol: $\alpha = 0.995$, $I_E = 10\text{mA}$, $I_{CO} = 0.5\text{nA}$, $I_C = ?$, $I_B = ?$, $\beta = ?$ & $I_{CEO} = 0$

$$\rightarrow I_C = \alpha I_E = 0.995 \times 10 \times 10^{-3}$$

$$\therefore I_C = 9.95\text{mA}$$

$$\rightarrow I_B = I_E - I_C = (10 - 9.95)\text{mA}$$

$$\therefore I_B = 0.05\text{mA}$$

$$\rightarrow \beta = \frac{I_C}{I_B} = \frac{9.95\text{mA}}{0.05\text{mA}}$$

$$\therefore \beta = 199$$

$$\rightarrow I_{CEO} = (\beta+1) I_{CO} = (199+1) \times 0.5 \times 10^{-6} = 200 \times 0.5 \times 10^{-6}$$

$$I_{CEO} = 100\text{nA}$$

#> TRANSISTOR BIASING METHODS

①

*> Need for Biasing:

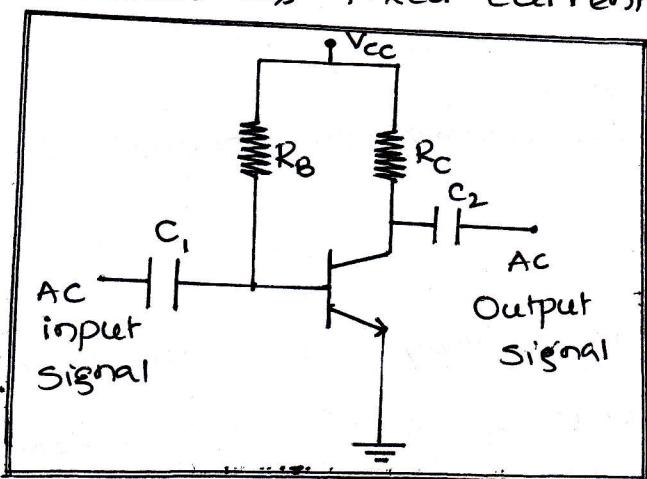
- Transistor parameters [like output voltage & output current] should be made as independent of temperature.
- Operating point must be made as independent of temperature.
- Operating point position must be maintained under Active Region

(*> Operating point of transistor varies due to change ⁱⁿ [transistor] temperature. To maintain the operating point stable by keeping I_c & V_{ce} constant so that the transistor will always work in Active region, to achieve above said parameters ^{the} following biasing techniques are designed & implemented.

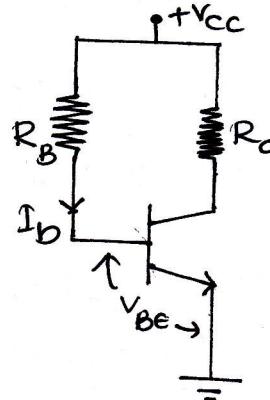
- 1> Base Bias 2> Collector to Base Bias
- 3> Voltage Divider Bias

*> BASE BIAS METHOD:

- In base bias method base current i.e. i_b current is controlled by V_{cc} & R_B . Hence this circuit is also known as fixed current bias or fixed bias circuit.



$\xrightarrow{\text{DC}}$
Equivalent



Step 1: Apply KVL to i/p section:→

In the input section V_{CC} is voltage source, E_B , R_B & V_{BE} are the voltage drops well as base to emitter [V_{BE}] are the voltage drops

i.e $V_{CC} = V_{RB} + V_{BE}$

$$V_{CC} = I_B R_B + V_{BE}$$

or $I_B = \frac{V_{CC} - V_{BE}}{R_B} \rightarrow (1)$

∴ Output Current

$$I_C = \beta I_B \rightarrow (2)$$

Step 2: Apply KVL to o/p section:→

In the output section, V_{CC} is the source voltage, voltage drops are V_{RC} & V_{CE}

$$\therefore V_{CC} = V_{RC} + V_{CE}$$

$$V_{CC} = I_C R_C + V_{CE}$$

or $V_{CE} = V_{CC} - I_C R_C \rightarrow (3)$

→ The main aim of designing the transistor biasing circuit is to determine operating point i.e combination of output voltage & output current.

Hence eqns (2) & (3) together represent operating point of base bias method.

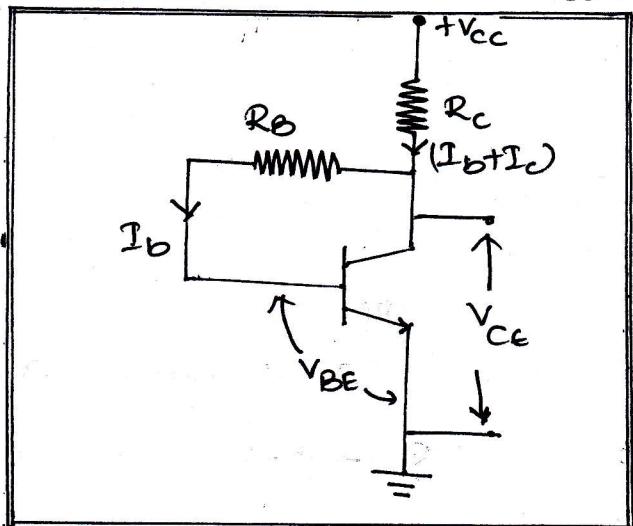
•> Eqns (2) & (3) indicates that they are independent of temperature hence operating is also independent of temperature & it can be maintained always in "Active"

*> COLLECTOR TO BASE BIAS METHOD:

(3)

→ It is an improvement of base bias method.

→ In this circuit a feedback resistor R_B is connected between collector and base region.



→ Current flowing through R_B is I_b & through R_c is $[I_b + I_c]$

→ In the i/p section, the supply & components are V_{cc} , R_c , R_B & Base to Emitter region

→ Similarly in the o/p section, the supply & components are V_{cc} , R_c & Collector to Emitter region.

Step 1: Apply KVL to i/p loop or to i/p Section.

$$\text{we get, } V_{cc} = V_{R_c} + V_{R_B} + V_{BE}$$

where $V_{R_c} \rightarrow$ Voltage drop across "R_c"

$V_{R_B} \rightarrow$ Voltage drop across resistor R_B

$$\therefore V_{cc} = (I_c + I_B) R_c + I_B R_B + V_{BE}$$

$$V_{cc} = I_c R_c + I_B R_c + I_B R_B + V_{BE} \rightarrow (1)$$

$$\text{but } I_c = (I_B) (\beta)$$

$$\therefore (1) \Rightarrow V_{cc} = (I_B \beta) R_c + I_B R_c + I_B R_B + V_{BE}$$

$$= I_B [\beta R_c + R_c + R_B] + V_{BE}$$

$$V_{cc} = I_B [\{ \beta + 1 \} R_c + R_B] + V_{BE}$$

$$\text{or } I_B = \frac{(V_{cc} - V_{BE})}{(\beta + 1) R_c + R_B} \rightarrow (2)$$

→ operating point current i.e $I_c = \beta I_B \rightarrow (3)$
[where I_B is eq 2]

step 2: Apply KVL to o/p loop or to o/p section,

we get, $V_{cc} = (I_c + I_B) R_c + V_{ce}$

or $V_{ce} = V_{cc} - [I_c + R_B] R_c \rightarrow (4)$

∴ The combination of eqs (3) & (4) is called as operating point of 'collector to base bias Technique'.

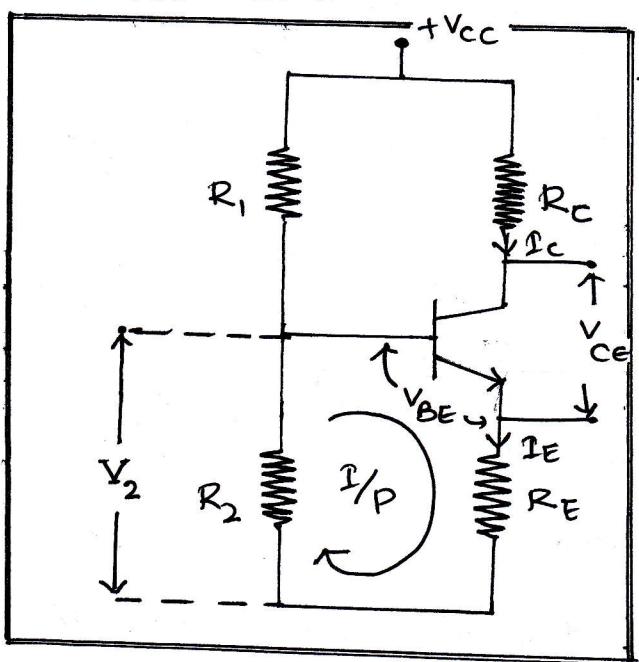
→ Equations (2), (3) & (4) indicates all parameters are independent of temperature variations hence transistor's operating point's position cannot be altered hence it is maintained in "Active region".

→ In this circuit R_B connects input section & output section of the circuit. A part of the o/p is fed back to the i/p section hence this circuit is also called as voltage feedback bias circuit.

*>> VOLTAGE DIVIDER BIAS NETWORK:

(5)

- In this network transistor's mode of operation is depending on R_1 , R_2 & R_E
- It has highest stability against temperature variations hence it is the most commonly used biasing Network.



→ where resistors R_1 & R_2 are called as voltage dividing resistors.

→ Voltage drop across resistor " R_2 " acts like Source to I/P loop.

→ And also " V_2 " [i.e. voltage drop across R_2] Switches "on" base emitter junction & remaining voltage will drop across " R_E ".

→ I_c is Current flowing through Collector as well as resistor R_E & I_E is current flowing through the resistor R_E .

→ If I_b is neglected then $I_E \approx I_c$

[VDR]

Step 1: Apply voltage divider rule across resistor " R_2 "

- resistor R_1 & R_2 are connected in series combination
∴ the source of voltage is V_{CC}

$$\therefore \text{Voltage divider rule} = \frac{\text{(Total Voltage)}}{\text{[Sum of all resistors]}} \left[\begin{array}{l} \text{Voltage drop} \\ \text{across that} \\ \text{resistor} \end{array} \right]$$

$$\text{i.e } V_x = \frac{(V_T)(R_x)}{\sum R}$$

\therefore VDR across R_2 is

$$V_{R_2} = V_2 = \frac{V_{CC} R_2}{R_1 + R_2} \rightarrow (1)$$

Step 2: Apply KVL to i/p loop

we get, $V_2 = V_{BE} + I_E R_E$

where $I_E \approx I_c$

$$\therefore V_2 = V_{BE} + I_c R_E$$

or

$$I_c = \frac{V_2 - V_{BE}}{R_E} \rightarrow (2)$$

Step 3: Apply KVL to o/p loop

in the o/p loop of voltage divider bias source is V_{CC} & components of that loop are R_C , collector to Emitter region & R_E

$$\therefore V_{CC} = V_{R_C} + V_{CE} + V_{R_E}$$

or $V_{CC} = (I_c R_C) + V_{CE} + (I_E R_E)$

where $I_E \approx I_c$

$$\therefore V_{CC} = I_c R_C + V_{CE} + I_c R_E$$

$$V_{CC} - V_{CE} = I_c (R_C + R_E)$$

or $I_c = \frac{V_{CC} - V_{CE}}{(R_C + R_E)}$ & also

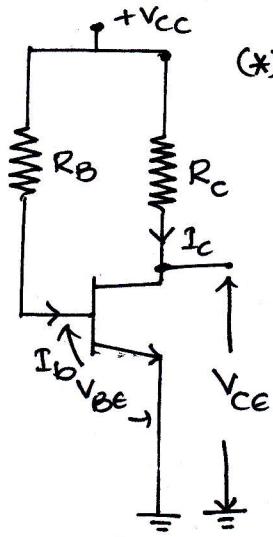
$$V_{CE} = V_{CC} - I_c [R_C + R_E] \rightarrow (3)$$

(7)

The combination of Equations (2) & (3) together represents operating point of voltage divider bias.

#> DESIGNING OF BIASING CIRCUITS

1) Base Bias circuit



(*) Design equations

$$\bullet \quad R_c = \frac{V_{cc} - V_{ce}}{I_c}$$

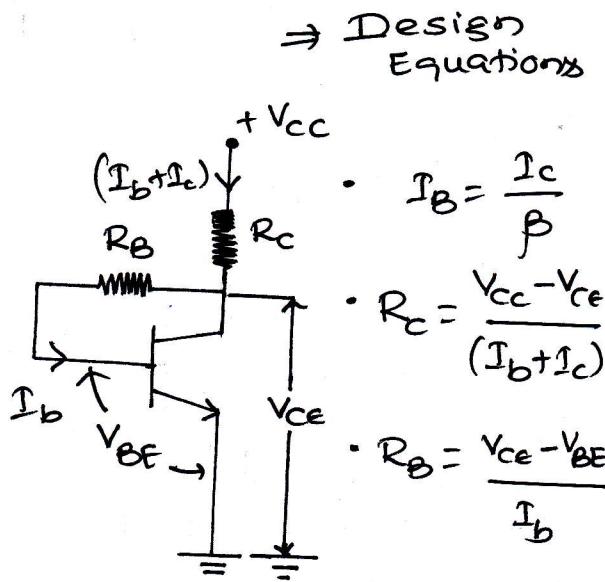
$$\bullet \quad R_b = \frac{V_{cc} - V_{be}}{I_b}$$

$$\bullet \quad I_c = \beta I_b$$

or

$$I_b = \frac{I_c}{\beta}$$

2) Collector to Base Bias



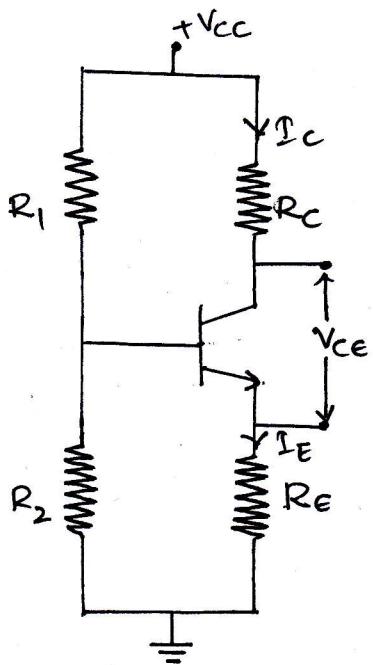
⇒ Design Equations

$$\bullet \quad I_b = \frac{I_c}{\beta}$$

$$\bullet \quad R_c = \frac{V_{cc} - V_{ce}}{(I_b + I_c)}$$

$$\bullet \quad R_b = \frac{V_{ce} - V_{be}}{I_b}$$

3) Voltage Divider Bias



$$\bullet \quad I_b = \frac{I_c}{\beta}$$

$$\bullet \quad R_c = \frac{V_{cc} - V_{ce}}{I_c} = \frac{V_{rc}}{I_c}$$

$$\bullet \quad R_e = \frac{V_{re}}{I_e} \approx \frac{V_{re}}{I_c}$$

#] LIST OF FORMULAE

1) Base Bias Method

$$\begin{aligned} \rightarrow I_B &= \frac{V_{CC} - V_{BE}}{R_B} & \rightarrow I_{Cmax} &= \frac{V_{CC}}{R_C} \\ \rightarrow I_C &= \beta I_B & \rightarrow V_{Cemax} &= V_{CC} \\ \rightarrow V_{CE} &= V_{CC} - I_C R_C & & \end{aligned} \quad \left. \begin{array}{l} \text{DC LOAD LINE} \\ \text{LINE} \end{array} \right\}$$

2) Collector to Base Bias Method

$$\begin{aligned} \rightarrow I_B &= \frac{[V_{CC} - V_{BE}]}{[(\beta+1)R_C + R_B]} & \rightarrow I_{Cmax} &= \frac{V_{CC}}{R_C} \\ \rightarrow I_C &= \beta I_B & \rightarrow V_{Cemax} &= V_{CC} \\ \rightarrow V_{CE} &= V_{CC} - (I_C + I_B) R_C & & \end{aligned} \quad \left. \begin{array}{l} \text{DC LOAD LINE} \\ \text{LINE} \end{array} \right\}$$

3) Voltage Divider Bias Method

$$\begin{aligned} \rightarrow V_2 &= \frac{V_{CC} R_2}{(R_1 + R_2)} \\ \rightarrow I_C &= \frac{V_2 - V_{BE}}{R_E} \\ \rightarrow V_{CE} &= V_{CC} - I_C (R_C + R_E) \end{aligned}$$

$$\begin{aligned} \rightarrow I_{CSat} \text{ or } I_{Cmax} &= \frac{V_{CC}}{(R_C + R_E)} \\ \rightarrow V_{CEcut-off} \text{ or } V_{Cemax} &= V_{CC} \end{aligned} \quad \left. \begin{array}{l} \text{DC LOAD LINE} \\ \text{POINTS} \end{array} \right\}$$

PROBLEMS ON BIASING METHOD

(9)

1) Calculate the Q-point values for the circuit of collector to base circuit. Given $R_B = 100\text{k}\Omega$, $R_c = 10\text{k}\Omega$, $V_{cc} = 12\text{V}$ and $\beta_{dc} = 100$

Sol: Operating point (Q-point) for ^{Collector to}_{base} circuit is

by

$$I_c = \beta I_B \quad \text{where } I_B = \frac{V_{cc} - V_{BE}}{(\beta + 1)R_c + R_B}$$

$$V_{ce} = V_{cc} - (I_B + I_c)R_c$$

$$\therefore I_B = \frac{12 - 0.7}{[(100+1)10 \times 10^3] + 100 \times 10^3}$$

[consider Given transistor is of Silicon
 $\therefore V_{BE} = 0.7\text{V}$]

$$= \frac{11.3}{[(10)10^4] + [10^5]} = \frac{11.3}{[(10.1) \times 10^5] + [10^5]}$$

$$= \frac{11.3}{11.1 \times 10^5} = \frac{1.018}{10^5} = 10.18 \times 10^{-6}$$

$$I_B = 10.18\text{mA}$$

$$\text{Hence } I_c = (\beta)(I_B) = (100)(10.18 \times 10^{-6})$$

$$I_c = 1.018\text{mA}$$

$$V_{ce} = (12) - ((10.18 \times 10^{-6}) + (1.018 \times 10^{-3})) \times [10 \times 10^3]$$

$$= [12] - [1.02818 \times 10^{-3}] \times 10^4$$

$$= 12 - 10.28 \quad \therefore \text{operating point is } [V_{ce}, I_c]$$

$$V_{ce} = 1.72\text{V}$$

i.e. $[1.72\text{V}, 1.018\text{mA}]$

2) The voltage divider bias circuit has $V_{CC} = 15V$, $R_1 = 6.8k\Omega$, $R_2 = 3.3k\Omega$, $R_E = R_E = 900\Omega$ and $h_{FE} = 90$, $V_{BE} = 0.7V$. Find the values of V_E , I_B , I_C , V_{CE} , V_C . Draw the DC LOAD LINE and mark the Q point on that.

Sol: Given Data, $V_{CC} = 15V$, $R_1 = 6.8k\Omega$, $R_2 = 3.3k\Omega$, $R_E = 900\Omega$, $R_E = 900\Omega$, $h_{FE} = \beta = 90$, $V_{BE} = 0.7V$
 $V_E = ?$, $I_B = ?$, $I_C = ?$, $V_{CE} = ?$, $V_C = ?$

For Voltage divider bias circuit,

$$V_2 = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{15 \times 3.3 \times 10^3}{(6.8 \times 10^3) + (3.3 \times 10^3)} = \frac{49.5 \times 10^3}{10.1 \times 10^3}$$

$$\therefore V_2 = 4.9V$$

Operating point current I_C or I_{CQ} is given by,

$$I_C = I_{CQ} = \frac{V_2 - V_{BE}}{R_E} = \frac{4.9 - 0.7}{900}$$

$$\therefore I_C = 4.66mA$$

Operating point voltage V_{CE} or V_{CEQ} is given by,

$$\begin{aligned} V_{CE} &= V_{CEQ} = V_{CC} - I_C [R_C + R_E] \\ &= 15 - [4.66 \times 10^{-3} \{900 + 900\}] \\ &= 15 - 8.388 \end{aligned}$$

$$\therefore V_{CE} = 6.6V$$

$$\therefore V_E = V_C = I_C R_C = 4.66 \times 10^{-3} \times 900$$

$$\therefore V_E = V_C = 4.2V$$

$$\therefore I_B = \frac{I_C}{\beta} = \frac{4.66 \times 10^{-3}}{90}$$

$$\therefore I_B = 52 \mu A$$

(*) DC LOAD LINE

From the above calculation we found,

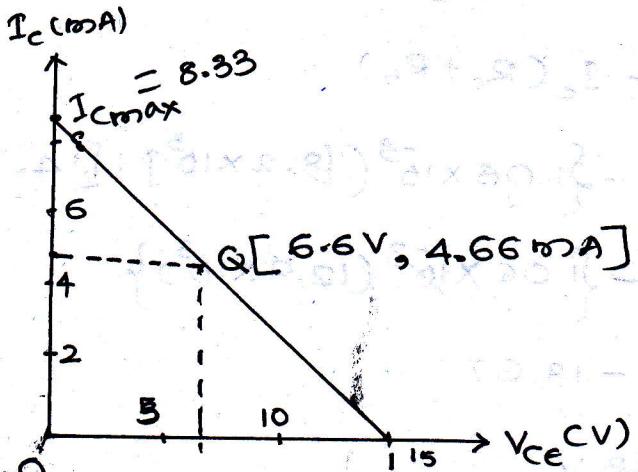
$$I_C = 4.66 \text{ mA} \quad V_{CE} = 6.6 \text{ V}$$

Now end points of Load line are,

$$I_{C\text{sat}} = I_{C\text{max}} = \frac{V_{CC}}{(R_L + R_E)} = \frac{15}{1800}$$

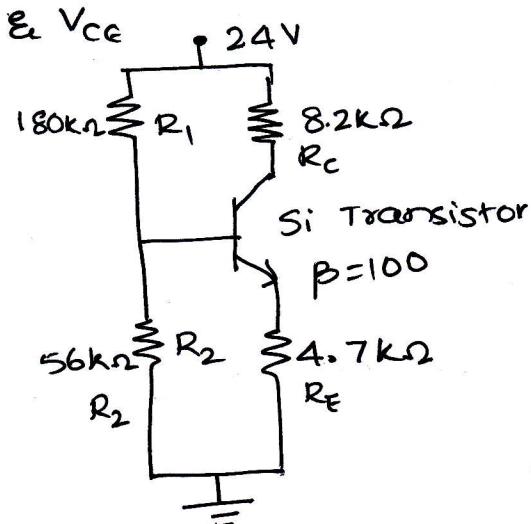
$$I_{C\text{sat}} = 8.33 \text{ mA}$$

$$V_{CE\text{max}} = V_{CE\text{cut-off}} = V_{CC} = 15 \text{ V}$$



$$V_{CE\text{max}} = 15 \text{ V}$$

3) For the circuit shown below, determine I_C , V_E , V_C



Soln: From the given circuit,

$$R_1 = 180\text{k}\Omega, R_2 = 56\text{k}\Omega,$$

$$R_c = 8.2\text{k}\Omega, R_E = 4.7\text{k}\Omega$$

$$V_{cc} = 24\text{V}, V_{BE} = 0.7\text{V}, \beta = 100$$

For the voltage Divider Bias circuit,

we have, $V_2 = \frac{V_{cc} R_2}{R_1 + R_2} = \frac{24 \times 56 \times 10^3}{(180 \times 10^3) + (56 \times 10^3)} = \frac{1344 \times 10^3}{236 \times 10^3}$

$$V_2 = 5.69\text{V}$$

•> operating point current is given by,

$$I_C = I_{CQ} = \frac{V_2 - V_{BE}}{R_E} = \frac{5.69 - 0.7}{4.7 \times 10^3}$$

$$\therefore I_C = 1.06\text{mA}$$

•> operating point voltage is given,

$$V_{CE} = V_{CEQ} = V_{cc} - I_C (R_c + R_E)$$

$$= 24 - \left\{ 1.06 \times 10^{-3} ([8.2 \times 10^3] + [4.7 \times 10^3]) \right\}$$

$$= 24 - \left\{ 1.06 \times 10^{-3} (12.9 \times 10^3) \right\}$$

$$= 24 - 13.67$$

$$V_{CE} = 10.33\text{V}$$

$$\bullet > V_E = I_E R_E = (I_c + I_b) R_E = \left(I_c + \frac{I_c}{\beta} \right) R_E = \left(1.06 \times 10^{-3} + \frac{1.06 \times 10^{-3}}{100} \right) 4.7 \times 10^3$$

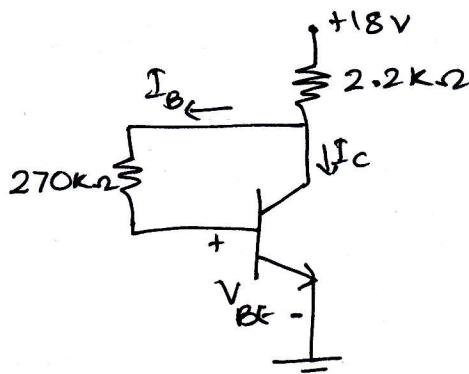
$$V_E = 5.03\text{V}$$

$$\bullet > V_C = V_{cc} - I_C R_C = 24 - (1.06 \times 10^{-3}) (8.2 \times 10^3)$$

$$V_C = 15.3\text{V}$$

4) Calculate the maximum & minimum levels of I_c & V_{CE} for the bias circuit shown in below when (13)

$\beta_{FE(\min)} = 50$ & $\beta_{FE(\max)} = 200$ Assume $V_{BE} = 0.7V$



Sol: From the given problem statement,

$$\beta_{FE(\min)} = \beta_{\min} = 50$$

$$\beta_{FE(\max)} = \beta_{\max} = 200 \quad V_{BE} = 0.7V$$

$$V_{CC} = 18V, R_B = 270k\Omega \text{ & } R_C = 2.2k\Omega$$

case i) For minimum levels of I_c & V_{CE} ($\beta = 50$)

Given circuit is Collector to Base Bias, For which,

$$I_B = \frac{V_{CC} - V_{BE}}{(\beta+1)R_C + R_B} = \frac{18 - 0.7}{[(50+1)2.2 \times 10^3] + [270 \times 10^3]} = \frac{17.3}{382.2 \times 10^3}$$

$$I_B = 45.3 \mu A$$

$$\therefore I_c = \beta I_B = 50 \times 45.3 \times 10^{-6}$$

$$I_c = 2.265 mA$$

$$\therefore V_{CE} = V_{CC} - (I_c + I_B) R_C = 18 - [(2.265 \times 10^{-3}) + (45.3 \times 10^{-6})] 2.2 \times 10^3$$

$$V_{CE} = 18.9V \quad \therefore V_{CE\min} = 18.9V, I_{c\min} = 2.265 mA$$

case ii) For maximum levels of I_c & V_{CE} when $\beta = 200$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{(\beta+1)R_C + R_B} = \frac{18 - 0.7}{[(200)2.2 \times 10^3] + [270 \times 10^3]} = \frac{17.3}{712.2 \times 10^3}$$

$$I_B = 24.29 \mu A$$

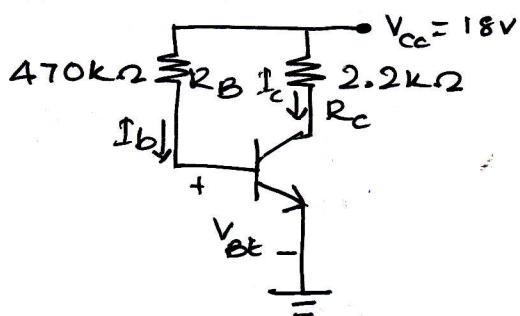
$$\therefore I_c = \beta I_B = (200)(24.29 \mu A) = 4.858 mA = I_{c(\max)}$$

$$\therefore V_{CE} = V_{CC} - [I_c + I_B] R_C = 18 - [(4.858 \times 10^{-3}) + (24.29 \times 10^{-6})] 2.2 \times 10^3$$

$$V_{CE(\max)} = 7.25V$$

5) In the circuit shown below, $B = 100$ is used.

Find I_c & V_{ce} . Draw the DC load line output characteristics & indicate Q-point. Take $V_{be} = 0.7$ Volts.



Sol2: From given problem state,

$$B = 100, V_{be} = 0.7V, V_{cc} = 18V,$$

$$R_b = 470k\Omega, R_c = 2.2k\Omega,$$

From circuit diagram it indicates biasing technique is Base Biasing method for which operating point current & voltage are given by,

$$\rightarrow I_c = B I_B \quad \text{where } I_B = \frac{V_{cc} - V_{be}}{R_b} = \frac{18 - 0.7}{270 \times 10^3}$$

$$= (100)(64.07 \mu A) \quad I_B = 64.07 \mu A$$

$$\therefore I_c = 6.407 mA$$

$$\begin{aligned} \rightarrow V_{ce} &= V_{cc} - I_c R_c \\ &= 18 - (6.4 \times 10^{-3})(2.2 \times 10^3) \\ &= 18 - 14.08 = 3.92V \end{aligned}$$

Now DC LOAD LINE

$$I_{comax} = \frac{V_{cc}}{R_c} = \frac{18}{2.2 \times 10^3} = 8.18mA$$

$$V_{cemax} = V_{cc} = 18V$$

$$Q [3.92V, 6.407mA]$$

