

#> TRANSISTOR BIASING METHODS

①

*> Need for Biasing:

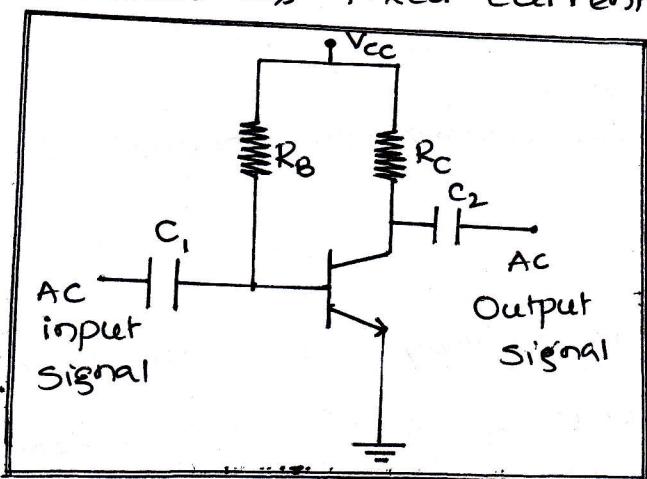
- Transistor parameters [like output voltage & output current] should be made as independent of temperature.
- Operating point must be made as independent of temperature.
- Operating point position must be maintained under Active Region

(*> Operating point of transistor varies due to change ⁱⁿ [transistor] temperature. To maintain the operating point stable by keeping I_c & V_{ce} constant so that the transistor will always work in Active region, to achieve above said parameters ^{the} following biasing techniques are designed & implemented.

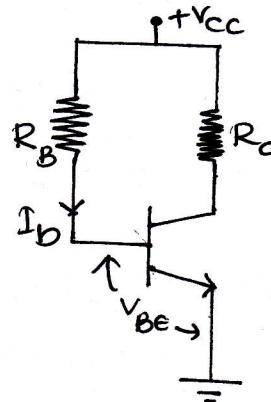
- 1> Base Bias 2> Collector to Base Bias
- 3> Voltage Divider Bias

*> BASE BIAS METHOD:

- In base bias method base current i.e. i_b current is controlled by V_{cc} & R_B . Hence this circuit is also known as fixed current bias or fixed bias circuit.



$\xrightarrow{\text{DC}}$
Equivalent



Step 1: Apply KVL to i/p section:→

In the input section V_{CC} is voltage source, E_B , R_B & V_{BE} are the voltage drops well as base to emitter [V_{BE}] are the voltage drops

i.e $V_{CC} = V_{RB} + V_{BE}$

$$V_{CC} = I_B R_B + V_{BE}$$

or $I_B = \frac{V_{CC} - V_{BE}}{R_B} \rightarrow (1)$

∴ Output Current

$$I_C = \beta I_B \rightarrow (2)$$

Step 2: Apply KVL to o/p section:→

In the output section, V_{CC} is the source voltage, voltage drops are V_{RC} & V_{CE}

$$\therefore V_{CC} = V_{RC} + V_{CE}$$

$$V_{CC} = I_C R_C + V_{CE}$$

or $V_{CE} = V_{CC} - I_C R_C \rightarrow (3)$

→ The main aim of designing the transistor biasing circuit is to determine operating point i.e combination of output voltage & output current.

Hence eqns (2) & (3) together represent operating point of base bias method.

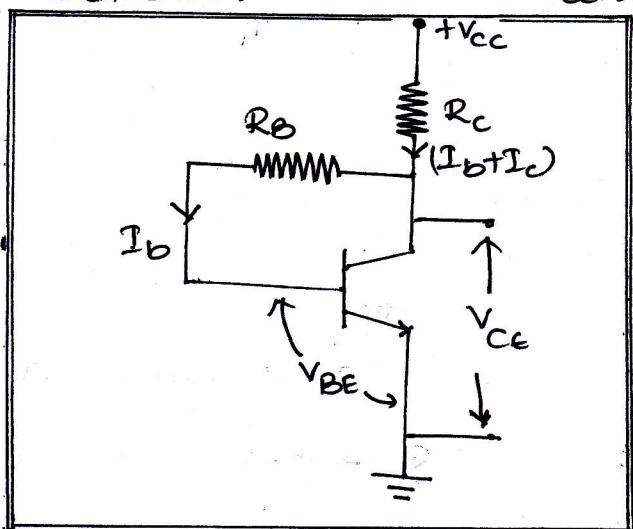
•> Eqns (2) & (3) indicates that they are independent of temperature hence operating is also independent of temperature & it can be maintained always in "Active"

*> COLLECTOR TO BASE BIAS METHOD:

(3)

→ It is an improvement of base bias method.

→ In this circuit a feedback resistor R_B is connected between collector and base region.



→ Current flowing through R_B is I_B & through R_c is $[I_B + I_C]$

→ In the i/p section, the supply & components are V_{CC} , R_c , R_B & Base to Emitter region

→ Similarly in the o/p section, the supply & components are V_{CC} , R_c & Collector to Emitter region.

Step 1: Apply KVL to i/p loop or to i/p Section.

$$\text{we get, } V_{CC} = V_{R_c} + V_{R_B} + V_{BE}$$

where $V_{R_c} \rightarrow$ Voltage drop across "R_c"

$V_{R_B} \rightarrow$ Voltage drop across resistor R_B

$$\therefore V_{CC} = (I_c + I_B) R_c + I_B R_B + V_{BE}$$

$$V_{CC} = I_c R_c + I_B R_c + I_B R_B + V_{BE} \rightarrow (1)$$

$$\text{but } I_c = (I_B) (\beta)$$

$$\therefore (1) \Rightarrow V_{CC} = (I_B \beta) R_c + I_B R_c + I_B R_B + V_{BE}$$

$$= I_B [\beta R_c + R_c + R_B] + V_{BE}$$

$$V_{CC} = I_B [\{ \beta + 1 \} R_c + R_B] + V_{BE}$$

$$\text{or } I_B = \frac{(V_{CC} - V_{BE})}{(\beta + 1) R_c + R_B} \rightarrow (2)$$

→ operating point current i.e $I_c = \beta I_B \rightarrow (3)$
[where I_B is eq 2]

step 2: Apply KVL to o/p loop or to o/p section,

we get, $V_{cc} = (I_c + I_B) R_c + V_{ce}$

or $V_{ce} = V_{cc} - [I_c + R_B] R_c \rightarrow (4)$

∴ The combination of eqs (3) & (4) is called as operating point of 'collector to base bias Technique'.

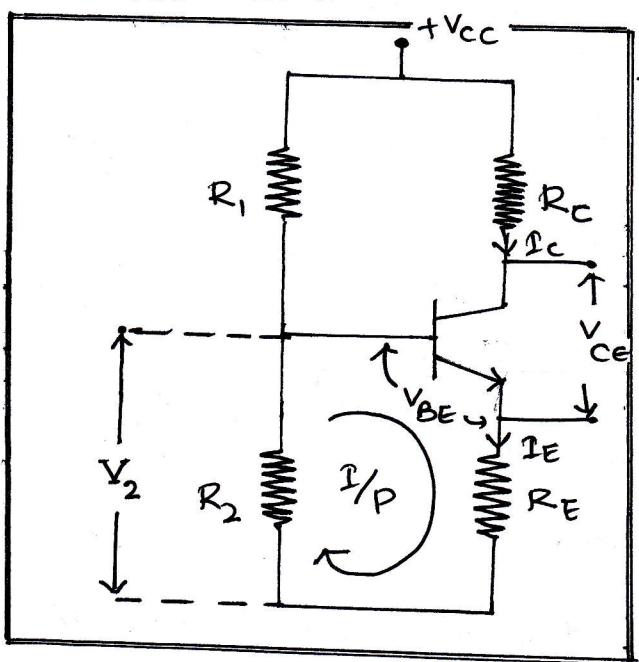
→ Equations (2), (3) & (4) indicates all parameters are independent of temperature variations hence transistor's operating point's position cannot be altered hence it is maintained in "Active region".

→ In this circuit R_B connects input section & output section of the circuit. A part of the o/p is fed back to the i/p section hence this circuit is also called as voltage feedback bias circuit.

*>> VOLTAGE DIVIDER BIAS NETWORK:

(5)

- In this network transistor's mode of operation is depending on R_1 , R_2 & R_E
- It has highest stability against temperature variations hence it is the most commonly used biasing Network.



→ where resistors R_1 & R_2 are called as voltage dividing resistors.

→ Voltage drop across resistor " R_2 " acts like Source to I/p loop.

→ And also " V_2 " [i.e. voltage drop across R_2] Switches "on" base emitter junction & remaining voltage will drop across " R_E ".

→ I_C is Current flowing through Collector as well as resistor R_E & I_E is current flowing through the resistor R_E .

→ If I_b is neglected then $I_E \approx I_C$

[VDR]

Step 1: Apply voltage divider rule across resistor " R_2 "

• resistor R_1 & R_2 are connected in series combination
→ & the source of voltage is V_{CC}

∴ Voltage divider rule = $\frac{(\text{Total Voltage})}{\text{[Sum of all resistors]}} \left[\begin{array}{l} \text{Voltage drop} \\ \text{across that} \\ \text{resistor} \end{array} \right]$

$$\text{i.e } V_x = \frac{(V_T)(R_x)}{\sum R}$$

\therefore VDR across R_2 is

$$V_{R_2} = V_2 = \frac{V_{CC} R_2}{R_1 + R_2} \rightarrow (1)$$

Step 2: Apply KVL to i/p loop

we get, $V_2 = V_{BE} + I_E R_E$

where $I_E \approx I_c$

$$\therefore V_2 = V_{BE} + I_c R_E$$

or

$$I_c = \frac{V_2 - V_{BE}}{R_E} \rightarrow (2)$$

Step 3: Apply KVL to o/p loop

in the o/p loop of voltage divider bias source is V_{CC} & components of that loop are R_C , collector to Emitter region & R_E

$$\therefore V_{CC} = V_{R_C} + V_{CE} + V_{R_E}$$

or $V_{CC} = (I_c R_C) + V_{CE} + (I_E R_E)$

where $I_E \approx I_c$

$$\therefore V_{CC} = I_c R_C + V_{CE} + I_c R_E$$

$$V_{CC} - V_{CE} = I_c (R_C + R_E)$$

or $I_c = \frac{V_{CC} - V_{CE}}{(R_C + R_E)}$ & also

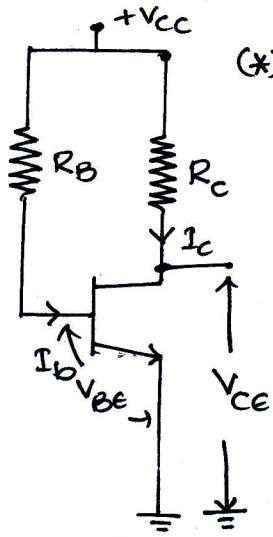
$$V_{CE} = V_{CC} - I_c [R_C + R_E] \rightarrow (3)$$

(7)

The combination of Equations (2) & (3) together represents operating point of voltage divider bias.

#> DESIGNING OF BIASING CIRCUITS

1> Base Bias circuit



(*) Design equations

$$\bullet \quad R_c = \frac{V_{cc} - V_{ce}}{I_c}$$

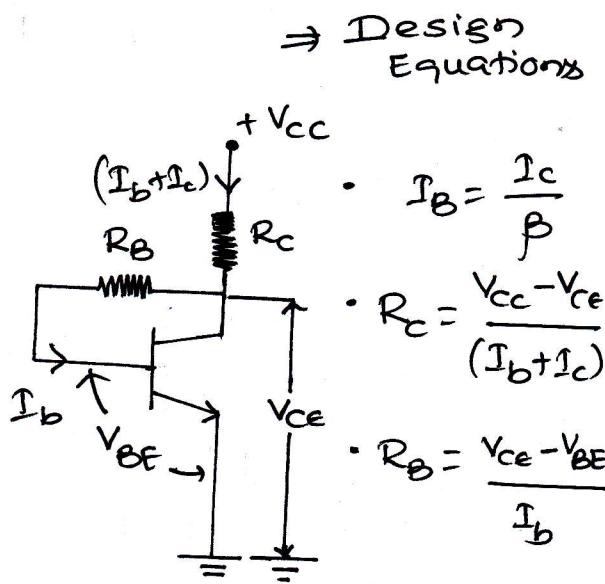
$$\bullet \quad R_b = \frac{V_{cc} - V_{be}}{I_b}$$

$$\bullet \quad I_c = \beta I_b$$

or

$$I_b = \frac{I_c}{\beta}$$

2> Collector to Base Bias



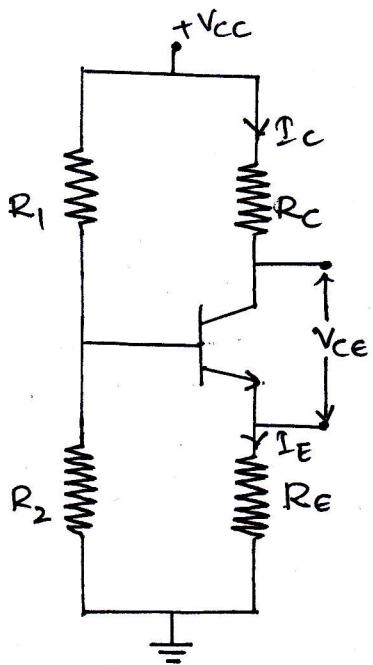
⇒ Design Equations

$$\bullet \quad I_b = \frac{I_c}{\beta}$$

$$\bullet \quad R_c = \frac{V_{cc} - V_{ce}}{(I_b + I_c)}$$

$$\bullet \quad R_b = \frac{V_{ce} - V_{be}}{I_b}$$

3> Voltage Divider Bias



$$\bullet \quad I_b = \frac{I_c}{\beta}$$

$$\bullet \quad R_c = \frac{V_{cc} - V_{ce}}{I_c} = \frac{V_{rc}}{I_c}$$

$$\bullet \quad R_e = \frac{V_{re}}{I_e} \approx \frac{V_{re}}{I_c}$$

#] LIST OF FORMULAE

1) Base Bias Method

$$\begin{aligned} \rightarrow I_B &= \frac{V_{CC} - V_{BE}}{R_B} & \rightarrow I_{Cmax} &= \frac{V_{CC}}{R_C} \\ \rightarrow I_C &= \beta I_B & \rightarrow V_{Cemax} &= V_{CC} \\ \rightarrow V_{CE} &= V_{CC} - I_C R_C & & \end{aligned} \quad \left. \begin{array}{l} \text{DC LOAD LINE} \\ \text{LINE} \end{array} \right\}$$

2) Collector to Base Bias Method

$$\begin{aligned} \rightarrow I_B &= \frac{[V_{CC} - V_{BE}]}{[(\beta+1)R_C + R_B]} & \rightarrow I_{Cmax} &= \frac{V_{CC}}{R_C} \\ \rightarrow I_C &= \beta I_B & \rightarrow V_{Cemax} &= V_{CC} \\ \rightarrow V_{CE} &= V_{CC} - (I_C + I_B) R_C & & \end{aligned} \quad \left. \begin{array}{l} \text{DC LOAD LINE} \\ \text{LINE} \end{array} \right\}$$

3) Voltage Divider Bias Method

$$\begin{aligned} \rightarrow V_2 &= \frac{V_{CC} R_2}{(R_1 + R_2)} \\ \rightarrow I_C &= \frac{V_2 - V_{BE}}{R_E} \\ \rightarrow V_{CE} &= V_{CC} - I_C (R_C + R_E) \end{aligned}$$

$$\begin{aligned} \rightarrow I_{CSat} \text{ or } I_{Cmax} &= \frac{V_{CC}}{(R_C + R_E)} \\ \rightarrow V_{CEcut-off} \text{ or } V_{Cemax} &= V_{CC} \end{aligned} \quad \left. \begin{array}{l} \text{DC LOAD LINE} \\ \text{POINTS} \end{array} \right\}$$

PROBLEMS ON BIASING METHOD

(9)

1) Calculate the Q-point values for the circuit of collector to base circuit. Given $R_B = 100\text{k}\Omega$, $R_c = 10\text{k}\Omega$, $V_{cc} = 12\text{V}$ and $\beta_{dc} = 100$

Sol: Operating point (Q-point) for ^{Collector to}_{base} circuit is

by

$$I_c = \beta I_B \quad \text{where } I_B = \frac{V_{cc} - V_{BE}}{(\beta + 1)R_c + R_B}$$

$$V_{ce} = V_{cc} - (I_B + I_c)R_c$$

$$\therefore I_B = \frac{12 - 0.7}{[(100+1)10 \times 10^3] + 100 \times 10^3}$$

[consider Given transistor is of Silicon
 $\therefore V_{BE} = 0.7\text{V}$]

$$= \frac{11.3}{[(10)10^4] + [10^5]} = \frac{11.3}{[(10.1) \times 10^5] + [10^5]}$$

$$= \frac{11.3}{11.1 \times 10^5} = \frac{1.018}{10^5} = 10.18 \times 10^{-6}$$

$$I_B = 10.18\text{mA}$$

$$\text{Hence } I_c = (\beta)(I_B) = (100)(10.18 \times 10^{-6})$$

$$I_c = 1.018\text{mA}$$

$$V_{ce} = (12) - ((10.18 \times 10^{-6}) + (1.018 \times 10^{-3})) \times [10 \times 10^3]$$

$$= [12] - [1.02818 \times 10^{-3}] \times 10^4$$

$$= 12 - 10.28 \quad \therefore \text{operating point is } [V_{ce}, I_c]$$

$$V_{ce} = 1.72\text{V}$$

i.e. $[1.72\text{V}, 1.018\text{mA}]$

2) The voltage divider bias circuit has $V_{CC} = 15V$, $R_1 = 6.8k\Omega$, $R_2 = 3.3k\Omega$, $R_E = R_E = 900\Omega$ and $h_{FE} = 90$, $V_{BE} = 0.7V$. Find the values of V_E , I_B , I_C , V_{CE} , V_C . Draw the DC LOAD LINE and mark the Q point on that.

Sol: Given Data, $V_{CC} = 15V$, $R_1 = 6.8k\Omega$, $R_2 = 3.3k\Omega$, $R_E = 900\Omega$, $R_E = 900\Omega$, $h_{FE} = \beta = 90$, $V_{BE} = 0.7V$
 $V_E = ?$, $I_B = ?$, $I_C = ?$, $V_{CE} = ?$, $V_C = ?$

For Voltage divider bias circuit,

$$V_2 = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{15 \times 3.3 \times 10^3}{(6.8 \times 10^3) + (3.3 \times 10^3)} = \frac{49.5 \times 10^3}{10.1 \times 10^3}$$

$$\therefore V_2 = 4.9V$$

Operating point current I_C or I_{CQ} is given by,

$$I_C = I_{CQ} = \frac{V_2 - V_{BE}}{R_E} = \frac{4.9 - 0.7}{900}$$

$$\therefore I_C = 4.66mA$$

Operating point voltage V_{CE} or V_{CEQ} is given by,

$$\begin{aligned} V_{CE} &= V_{CEQ} = V_{CC} - I_C [R_C + R_E] \\ &= 15 - [4.66 \times 10^{-3} \{900 + 900\}] \\ &= 15 - 8.388 \end{aligned}$$

$$\therefore V_{CE} = 6.6V$$

$$\therefore V_E = V_C = I_C R_C = 4.66 \times 10^{-3} \times 900$$

$$\therefore V_E = V_C = 4.2V$$

$$\therefore I_B = \frac{I_C}{\beta} = \frac{4.66 \times 10^{-3}}{90}$$

$$\therefore I_B = 52 \mu A$$

(*) DC LOAD LINE

From the above calculation we found,

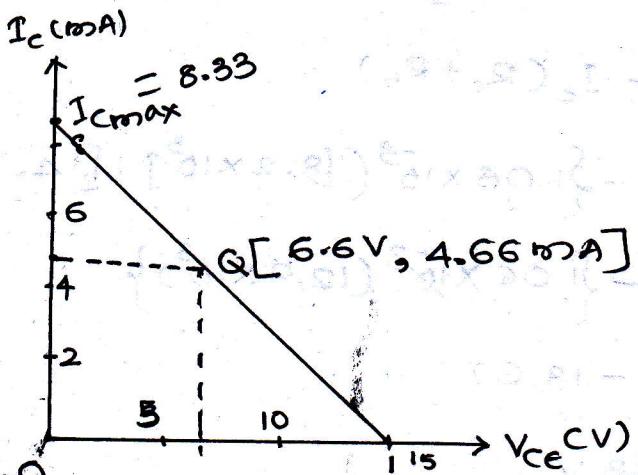
$$I_C = 4.66 \text{ mA} \quad V_{CE} = 6.6 \text{ V}$$

Now end points of Load line are,

$$I_{C\text{sat}} = I_{C\text{max}} = \frac{V_{CC}}{(R_L + R_E)} = \frac{15}{1800}$$

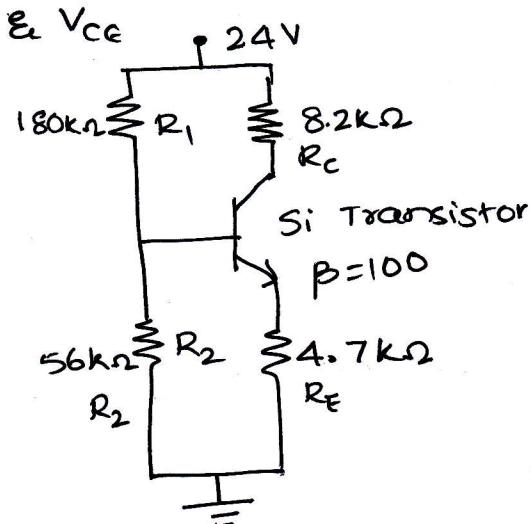
$$I_{C\text{sat}} = 8.33 \text{ mA}$$

$$V_{CE\text{max}} = V_{CE\text{cut-off}} = V_{CC} = 15 \text{ V}$$



$$V_{CE\text{max}} = 15 \text{ V}$$

3) For the circuit shown below, determine I_C , V_E , V_C



Sol: From the given circuit,

$$R_1 = 180\text{k}\Omega, R_2 = 56\text{k}\Omega,$$

$$R_c = 8.2\text{k}\Omega, R_E = 4.7\text{k}\Omega$$

$$V_{CC} = 24\text{V}, V_{BE} = 0.7\text{V}, \beta = 100$$

For the voltage Divider Bias circuit,

we have, $V_2 = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{24 \times 56 \times 10^3}{(180 \times 10^3) + (56 \times 10^3)} = \frac{1344 \times 10^3}{236 \times 10^3}$

$$V_2 = 5.69\text{V}$$

•> operating point current is given by,

$$I_C = I_{CQ} = \frac{V_2 - V_{BE}}{R_E} = \frac{5.69 - 0.7}{4.7 \times 10^3}$$

$$\therefore I_C = 1.06\text{mA}$$

•> operating point voltage is given,

$$V_{CE} = V_{CEQ} = V_{CC} - I_C (R_C + R_E)$$

$$= 24 - \left\{ 1.06 \times 10^{-3} ([8.2 \times 10^3] + [4.7 \times 10^3]) \right\}$$

$$= 24 - \left\{ 1.06 \times 10^{-3} (12.9 \times 10^3) \right\}$$

$$= 24 - 13.67$$

$$V_{CE} = 10.33\text{V}$$

$$\bullet > V_E = I_E R_E = (I_C + I_B) R_E = \left(I_C + \frac{I_C}{\beta} \right) R_E = \left(1.06 \times 10^{-3} + \frac{1.06 \times 10^{-3}}{100} \right) 4.7 \times 10^3$$

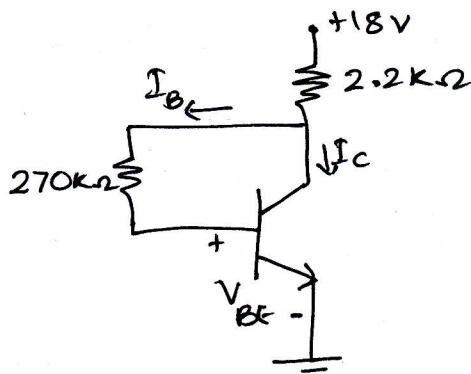
$$V_E = 5.03\text{V}$$

$$\bullet > V_C = V_{CC} - I_C R_C = 24 - (1.06 \times 10^{-3}) (8.2 \times 10^3)$$

$$V_C = 15.3\text{V}$$

4) Calculate the maximum & minimum levels of I_c & V_{ce} for the bias circuit shown in below when (13)

$\beta_{FE(\min)} = 50$ & $\beta_{FE(\max)} = 200$ Assume $V_{BE} = 0.7V$



Sol: From the given problem statement,

$$\beta_{FE(\min)} = \beta_{\min} = 50$$

$$\beta_{FE(\max)} = \beta_{\max} = 200 \quad V_{BE} = 0.7V$$

$$V_{cc} = 18V, R_B = 270k\Omega \text{ & } R_C = 2.2k\Omega$$

case i) For minimum levels of I_c & V_{ce} ($\beta = 50$)

Given circuit is Collector to Base Bias, For which,

$$I_B = \frac{V_{cc} - V_{BE}}{(\beta+1)R_C + R_B} = \frac{18 - 0.7}{[(50+1)2.2 \times 10^3] + [270 \times 10^3]} = \frac{17.3}{382.2 \times 10^3}$$

$$I_B = 45.3 \mu A$$

$$\therefore I_c = \beta I_B = 50 \times 45.3 \times 10^{-6}$$

$$I_c = 2.265 mA$$

$$\therefore V_{ce} = V_{cc} - (I_c + I_B) R_C = 18 - [(2.265 \times 10^{-3}) + (45.3 \times 10^{-6})] 2.2 \times 10^3$$

$$V_{ce} = 18.9V \quad \therefore V_{ce\min} = 18.9V, I_{c\min} = 2.265mA$$

case ii) For maximum levels of I_c & V_{ce} when $\beta = 200$

$$\therefore I_B = \frac{V_{cc} - V_{BE}}{(\beta+1)R_C + R_B} = \frac{18 - 0.7}{[(200)2.2 \times 10^3] + [270 \times 10^3]} = \frac{17.3}{712.2 \times 10^3}$$

$$I_B = 24.29 \mu A$$

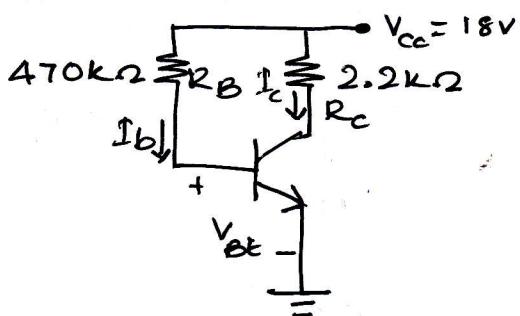
$$\therefore I_c = \beta I_B = (200)(24.29 \mu A) = 4.858mA = I_{c(\max)}$$

$$\therefore V_{ce} = V_{cc} - [I_c + I_B] R_C = 18 - [(4.858 \times 10^{-3}) + (24.29 \times 10^{-6})] 2.2 \times 10^3$$

$$V_{ce(\max)} = 7.25V$$

5) In the circuit shown below, $B = 100$ is used.

Find I_c & V_{ce} . Draw the DC load line output characteristics & indicate Q-point. Take $V_{be} = 0.7$ Volts.



Sol2: From given problem state,

$$B = 100, V_{be} = 0.7V, V_{cc} = 18V,$$

$$R_b = 470k\Omega, R_c = 2.2k\Omega,$$

From circuit diagram it indicates biasing technique is Base Biasing method for which operating point current & voltage are given by,

$$\rightarrow I_c = B I_B \quad \text{where } I_B = \frac{V_{cc} - V_{be}}{R_b} = \frac{18 - 0.7}{270 \times 10^3}$$

$$= (100)(64.07 \mu A) \quad I_B = 64.07 \mu A$$

$$\therefore I_c = 6.407 mA$$

$$\begin{aligned} \rightarrow V_{ce} &= V_{cc} - I_c R_c \\ &= 18 - (6.4 \times 10^{-3})(2.2 \times 10^3) \\ &= 18 - 14.08 = 3.92V \end{aligned}$$

Now DC LOAD LINE

$$I_{comax} = \frac{V_{cc}}{R_c} = \frac{18}{2.2 \times 10^3} = 8.18mA$$

$$V_{cemax} = V_{cc} = 18V$$

$$Q [3.92V, 6.407mA]$$

