ELECTRONIC PRINCIPLES AND DEVICES

Department of Electronics and Communication Engineering

Registers:

- A *register* is a group of flip-flops, each one of which shares a common clock and is capable of storing one bit of information.
- An *n* -bit register consists of a group of *n* flip-flops capable of storing *n* bits of binary information.
- In addition to the flip-flops, a register may have combinational gates that perform certain data-processing tasks.
- In its broadest definition, a register consists of a group of flip-flops together with gates that affect their operation.
- The flip-flops hold the binary information, and the gates determine how the information is transferred into the register.

4-bit Register:

- Various types of registers are available commercially.
- The simplest register is one that consists of only flip-flops, without any gates.
- Following Figure (next slide) shows such a register constructed with four *D* -type flip-flops to form a four-bit data storage register.
- The common clock input triggers all flip-flops on the positive edge of each pulse, and the binary data available at the four inputs are transferred into the register.
- The four outputs can be sampled at any time to obtain the binary information stored in the register.
- The input Clear goes to the active-low R (reset) input of all four flip-flops. When this input goes to 0, all flip-flops are reset asynchronously.
- The R inputs must be maintained at logic 1 (i.e., de-asserted) during normal clocked operation.

4-bit Register:

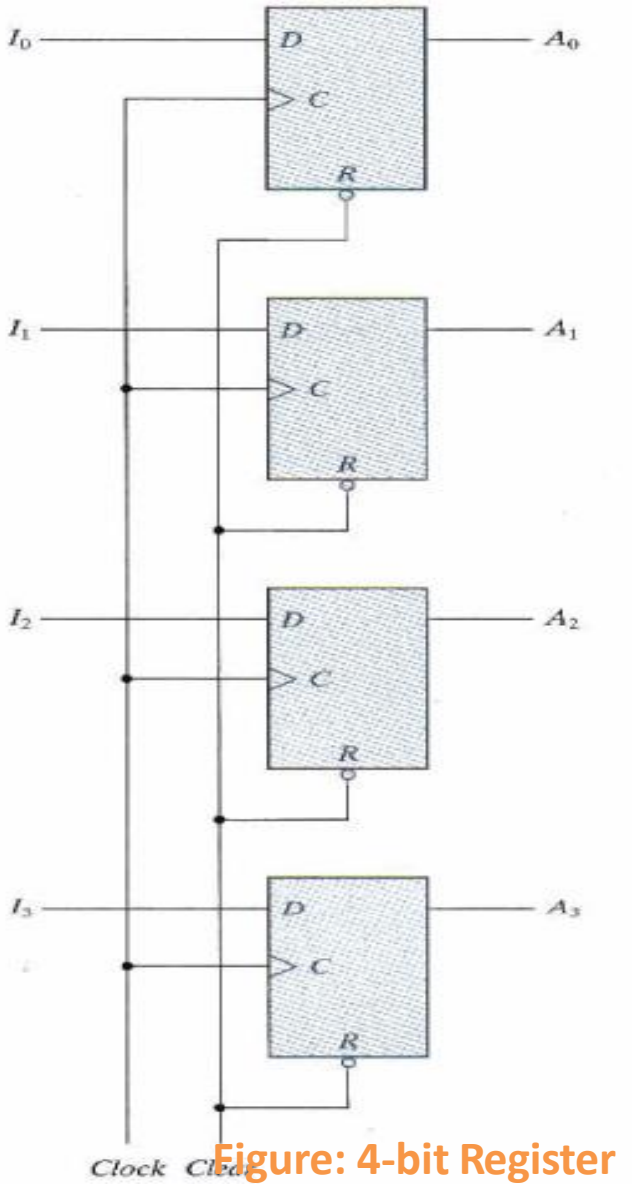


Figure: 4-bit Register

- The transfer of new information into a register is referred to as *loading* or *updating* the register.
- If all the bits of the register are loaded simultaneously with a common clock pulse, we say that the loading is done *in parallel* .
- A clock edge applied to the *C* inputs of the register of Figure, will load all four inputs in parallel.
- In this configuration, if the contents of the register must be left unchanged, the inputs must be held constant or the clock must be inhibited from the circuit.

SHIFT REGISTERS (SISO)

- A register capable of shifting the binary information held in each cell to its neighboring cell, in a selected direction, is called a *shift register*.
- The logical configuration of a shift register consists of a chain of flip-flops in cascade, with the output of one flip-flop connected to the input of the next flip-flop.
- All flip-flops receive common clock pulses, which activate the shift of data from one stage to the next.
- There are four different types of shift registers:
  - Serial In Serial Out (SISO)
  - Serial In Parallel Out (SIPO)
  - Parallel In Serial Out (PISO)
  - Parallel In Parallel Out (PIPO)

REGISTERS (SISO)

- The simplest possible shift register (SISO) is one that uses only flip-flops, as shown in the following Figure .
- The output of a given flip-flop is connected to the *D* input of the flip-flop at its right.
- This shift register is unidirectional (left-to-right).
- Each clock pulse shifts the contents of the register one bit position to the right.

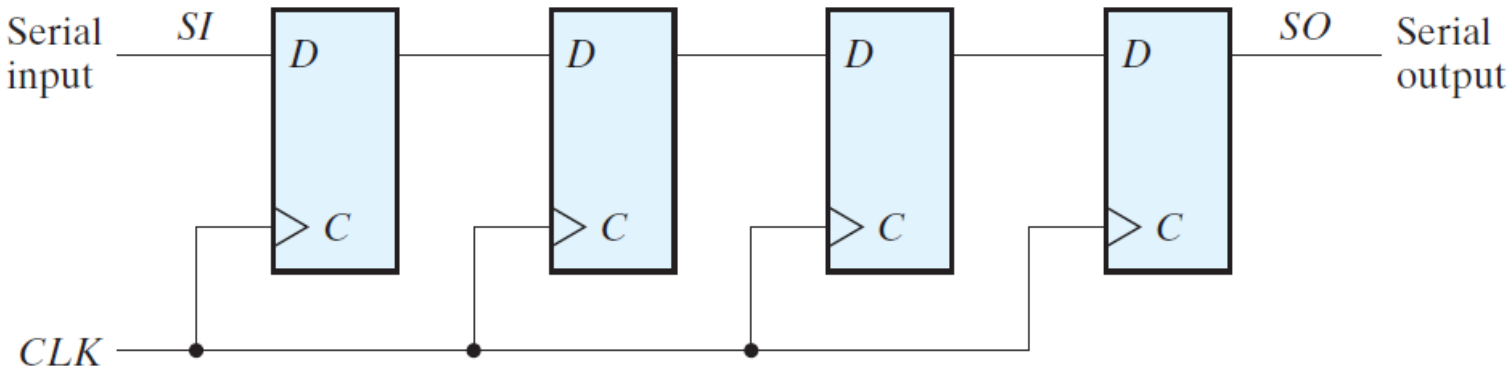
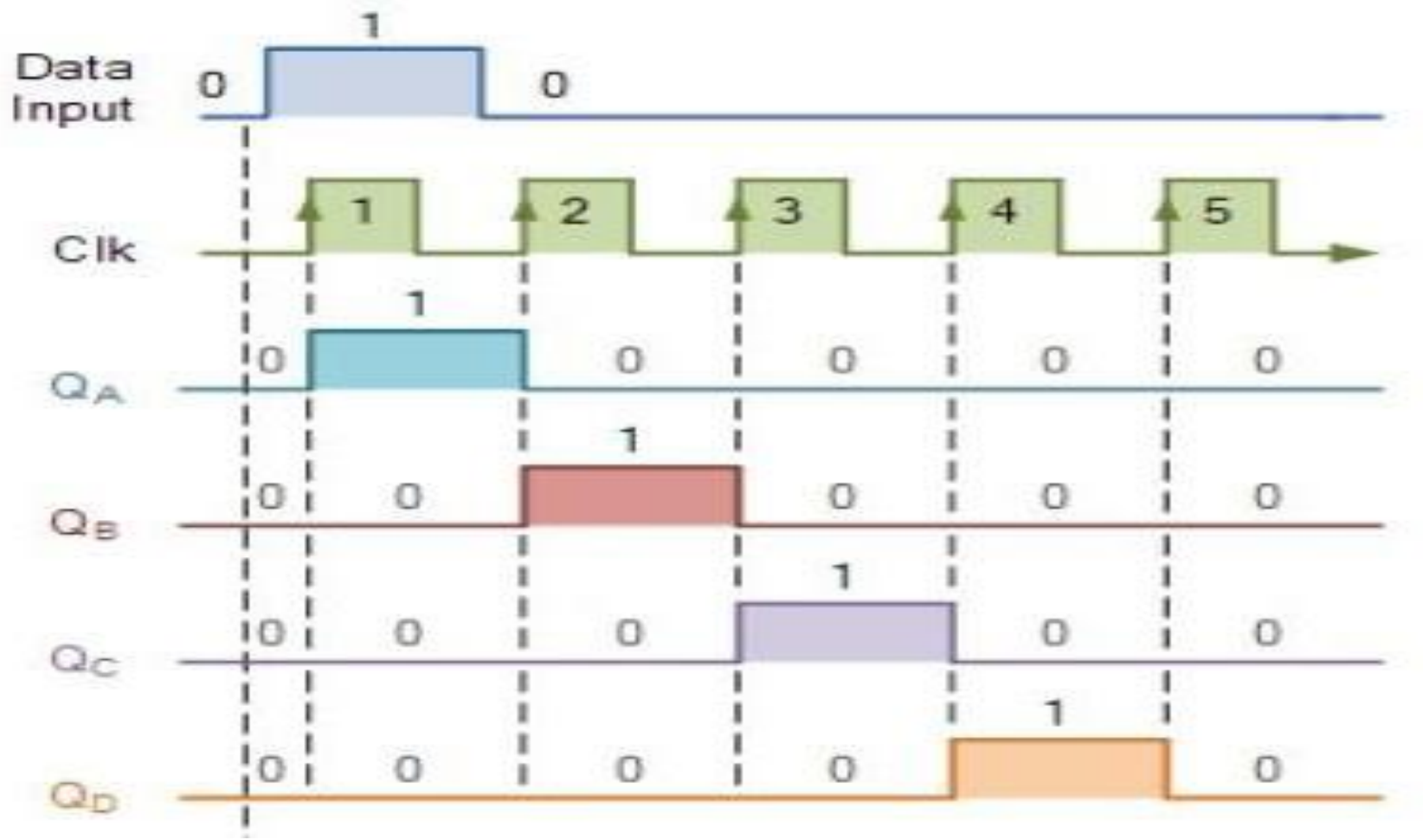


FIGURE: Four-bit shift register

REGISTERS (SISO)



Timing Diagram for SISO register

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4-bit Serial Input Serial Output (SISO) register:

Clock Pulse No	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	0	0	0	0

Data movement through a shift register

4-bit Serial Input Serial Output (SISO) register:

Example:

The register is shifted six times to the right with the serial input being 0110. What is the content of the register after each shift?

Answer:

0110; 0011; 1001; 1100; 0110; 0011.

4-bit Serial Input Serial Output (SISO) register:

Example:

The contents of a four-bit register is initially 0110. The register is shifted six times to the right with the serial input being 1011100. What is the content of the register after each shift?

Answer:

0110; 0011; 0001; 1000; 1100; 1110; 0111; 1011

	Data	QA	QB	QC	QD
	initial	0	1	1	0
1st	0	0	0	1	1
2nd	0	0	0	0	1
3rd	1	1	0	0	0
4th	1	1	1	0	0
5th	1	1	1	1	0
6th	0	0	1	1	1
7th	1	1	0	1	1

Electronic Principles and Devices

Synchronous and Asynchronous counters (Introduction):

- A register (group of flip-flops) that goes through a prescribed sequence of states upon the application of input pulses is called a *counter* .
- The input pulses may be clock pulses, or they may originate from some external source and may occur at a fixed interval of time or at random.
- The sequence of states may follow the binary number sequence or any other sequence of states.
- A counter that follows the binary number sequence is called a *binary counter* .
- An n -bit binary counter consists of n flip-flops and can count in binary from 0 through $2^n - 1$.

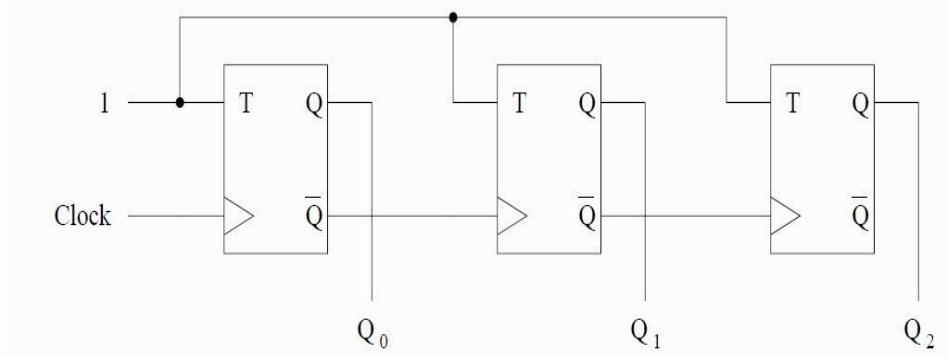
Electronic Principles and Devices

Synchronous and Asynchronous counters (Introduction):

- Counters are available in two categories: ripple (or asynchronous) counters and synchronous counters.
- In a ripple counter, a flip-flop output transition serves as a source for triggering other flip-flops.
- In other words, the *C* input of some or all flip-flops are triggered, not by the common clock pulses, but rather by the transition that occurs in other flip-flop outputs.
- In a synchronous counter, the *C* inputs of all flip-flops receive the common clock.

Electronic Principles and Devices

3 bit Asynchronous up- counter:



Circuit diagram

Truth Table

Number of clock pulses	Q_2 (MSB)	Q_1	Q_0 (LSB)
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Timing Diagram

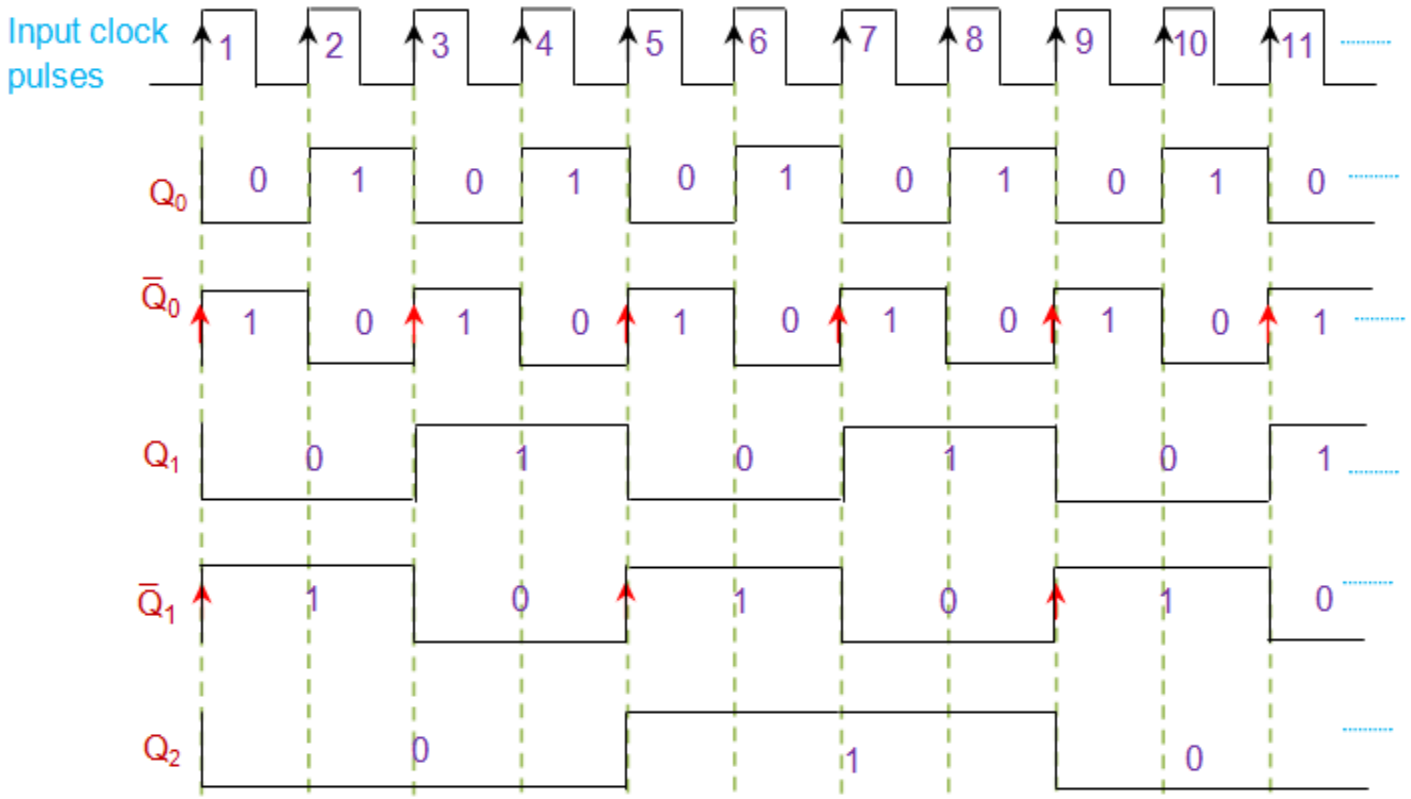


Figure 4 Timing diagram for 3-bit asynchronous positive edge triggered up-counter

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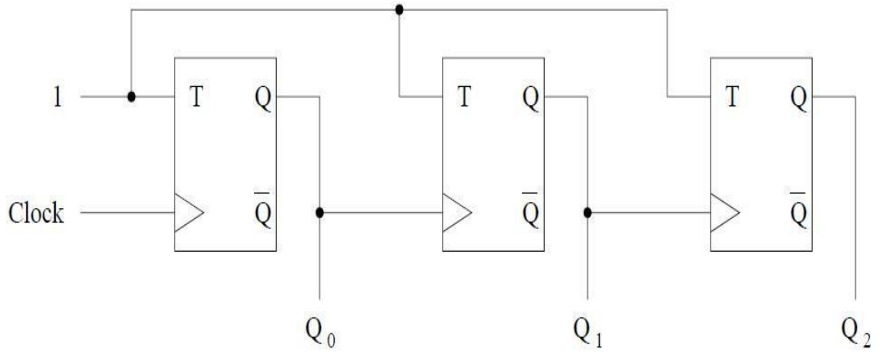
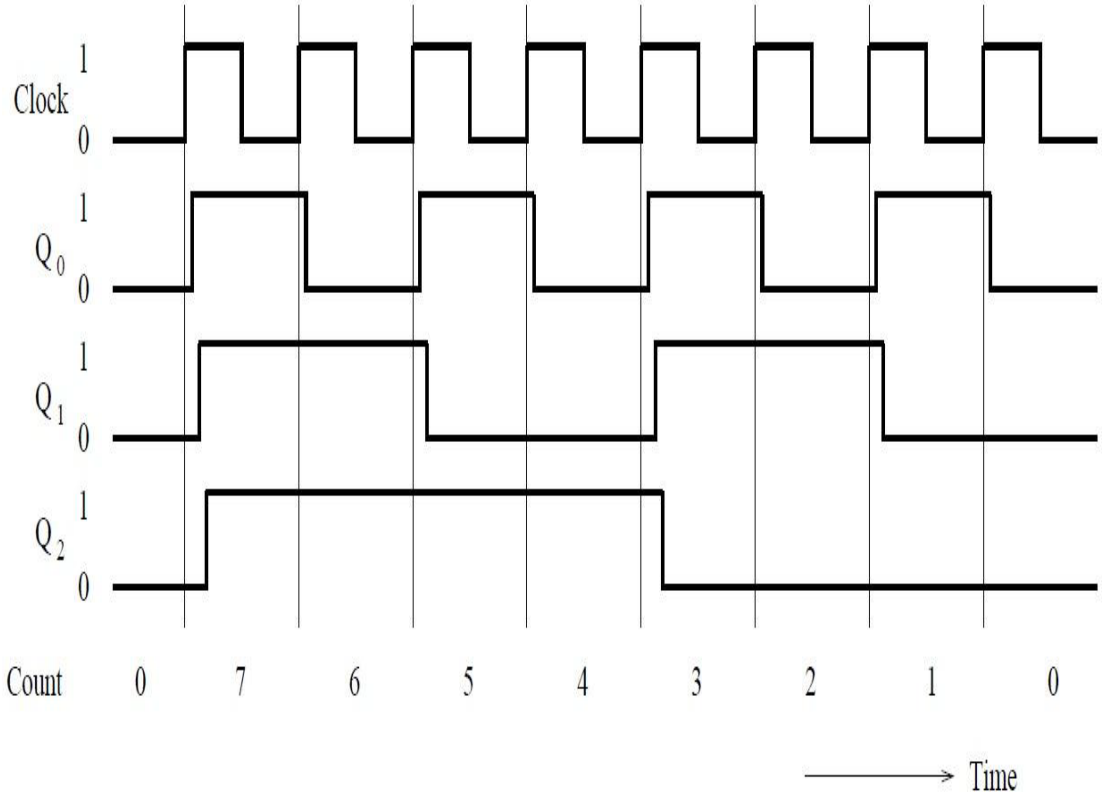
3 bit Asynchronous down - counter:



Circuit diagram

Timing Diagram



Truth Table

Number of clock pulses	Q_2 (MSB)	Q_1	Q_0 (LSB)
0	0	0	0
1	1	1	1
2	1	1	0
3	1	0	1
4	1	0	0
5	0	1	1
6	0	1	0
7	0	0	1

Concluding Remarks :

- **Registers, 4-bit registers**
- **4-bit SISO register** using D – flip flop, a synchronous sequential circuit which shifts the data value by one bit to the right.
- Counters
- **3 bit Asynchronous up- counter**, using T flip-flop.
- **3 bit Asynchronous down- counter**, using T flip-flop.

THANK YOU

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