

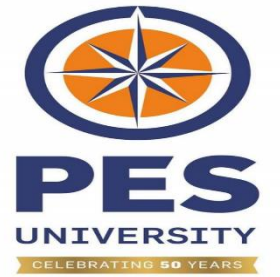


ELECTRONIC PRINCIPLES AND DEVICES

Dr. Ananda M

Department of Electronics and Communication.

ELECTRONIC PRINCIPLES AND DEVICES



Unit-3 Digital Electronics

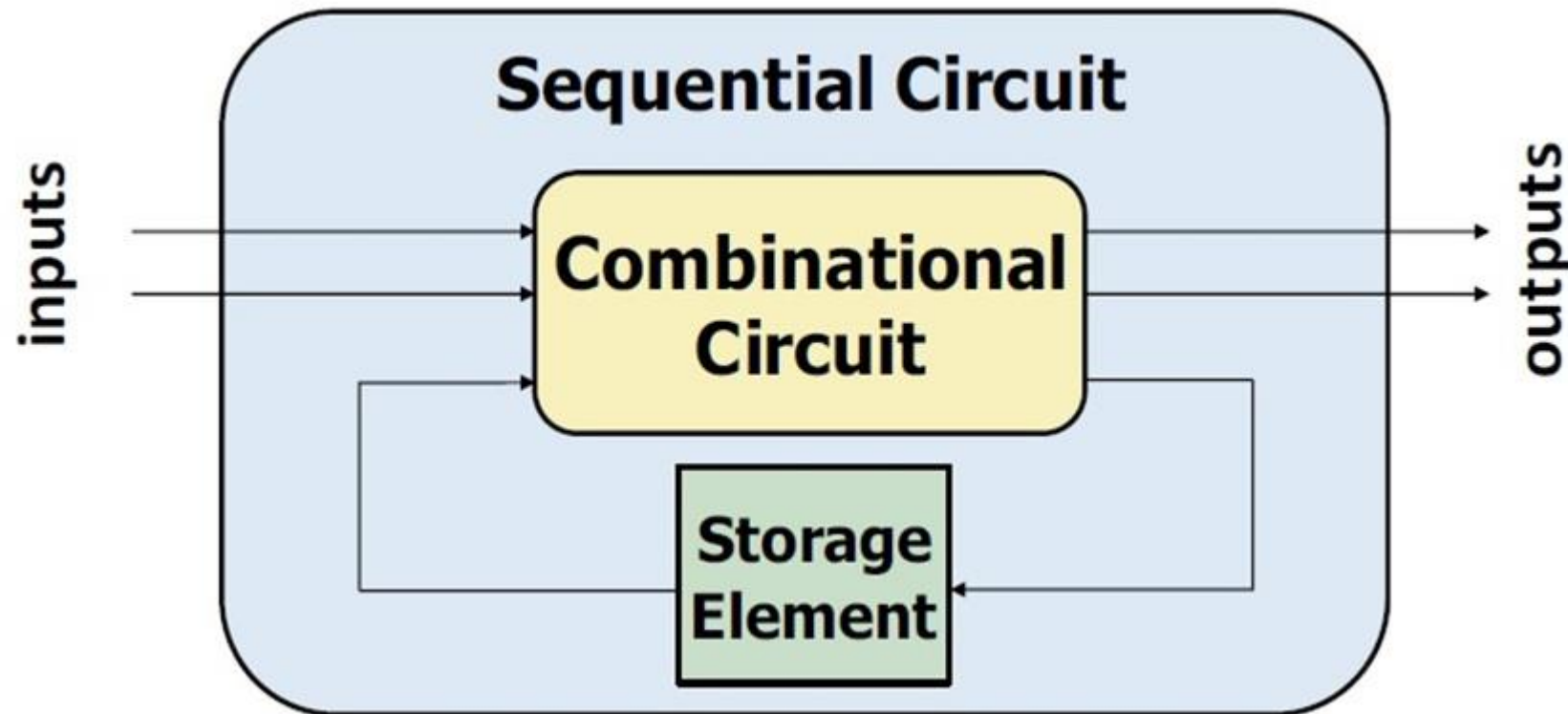
Introduction: Sequential Circuits : RS FF

Dr. Ananda M

Department of Electronics and Communication.

- Introduction to sequential circuits
- Types of sequential circuits
- R-S latch
- Problems in R-S latch
- R- S Flip Flop: Characteristic Table
- Conclusion Remarks

- Combinational Circuit output depend **only** on **present** input.
- We want circuits that produce the output depending on the **current** and **past** input values - Circuits with **memory**.
- How do we design such a circuit that **stores information**?



- Sequential Circuits are of **two** types

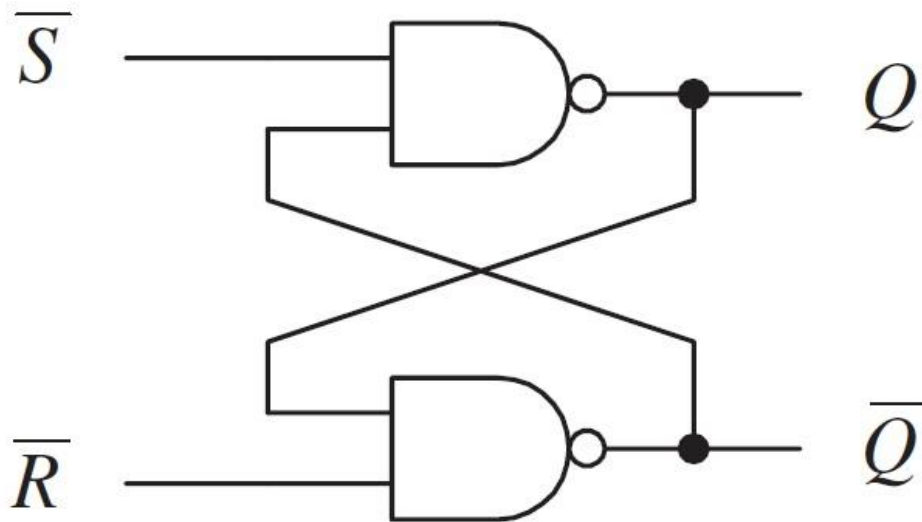
1. Synchronous Circuits:

- ☐ In synchronous sequential circuits, the state of the device changes only at discrete times in response to a **clock pulse**.

2. Asynchronous Circuits:

- ☐ Asynchronous circuit is **not synchronized** by a clock signal; the outputs of the circuit change directly in response to the change in the inputs.

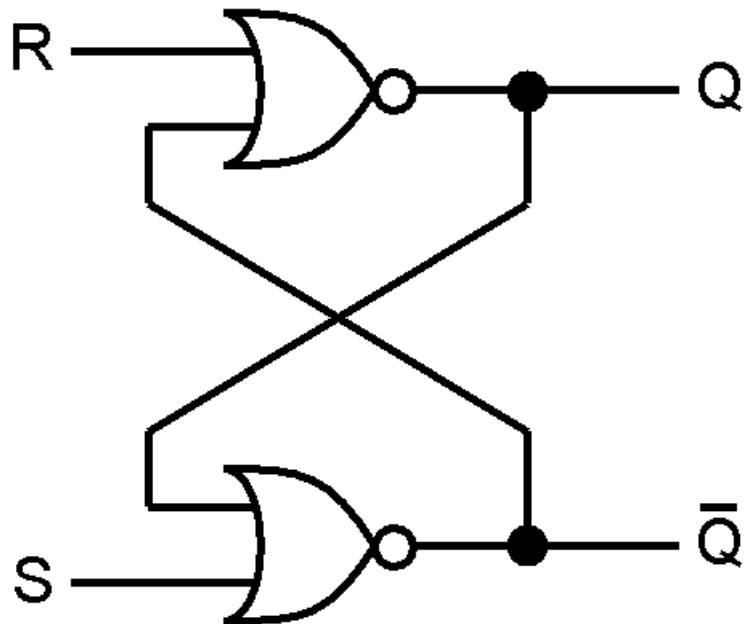
Circuit Diagram



Function Table

INPUTS		OUTPUTS		Status of S'R' Latch
S'	R'	Q	Q'	
0	0	1	1	FORBIDDEN
0	1	1	0	SET
1	0	0	1	RESET
1	1	Q_1	Q'_{-1}	PREVIOUS STATE

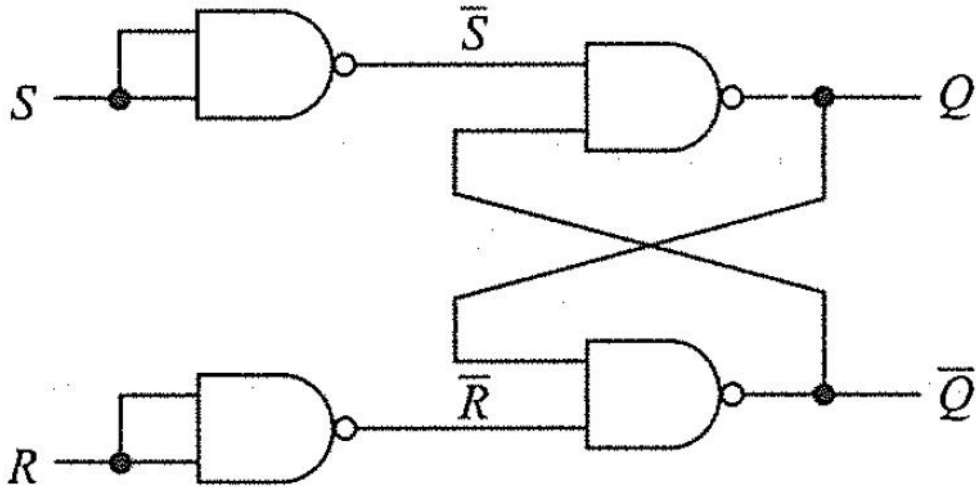
Circuit Diagram



Function Table

INPUTS		OUTPUTS		Status of RS Latch
R	S	Q	Q'	
0	0	Q_{-1}	Q'_{-1}	PREVIOUS STATE
0	1	1	0	SET
1	0	0	1	RESET
1	1	0	0	FORBIDDEN

Circuit Diagram



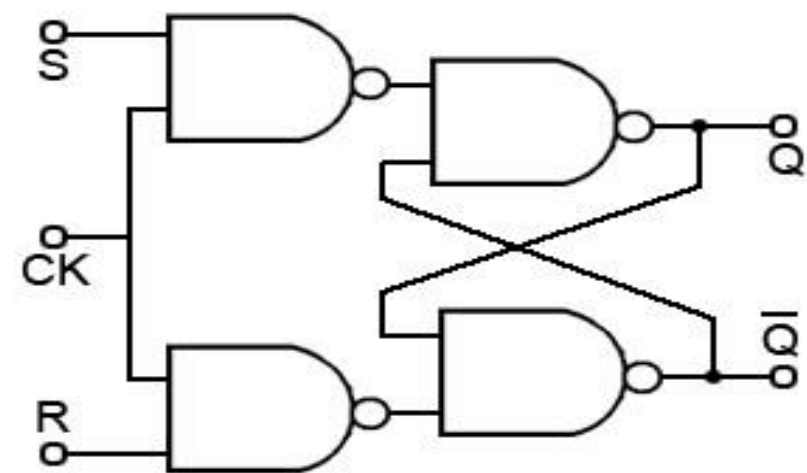
Function Table

INPUTS		OUTPUTS		Status of SR Latch
S	R	Q	Q'	
0	0	Q_1	Q'_{-1}	PREVIOUS STATE
0	1	0	1	RESET
1	0	1	0	SET
1	1	1	1	FORBIDDEN

Electronic Principles and Devices

The S-R (Set - Reset) Flip – Flop / Gated R-S latch

Logic Diagram



Function Table

INPUTS			OUTPUTS		Status of SR Flip-Flop
CK	S	R	Q	Q'	
0	X	X	Q_1	Q'_{-1}	PREVIOUS STATE
1	0	0	Q_1	Q'_{-1}	PREVIOUS STATE
1	0	1	0	1	RESET
1	1	0	1	0	SET
1	1	1	1	1	FORBIDDEN

1. Flip – flops are the **building blocks** of sequential circuits.
But these are built from **latches**.
2. Flip- flops **continuously checks** its inputs and changes its outputs correspondingly only at time instant determined by the **clock signal**.
3. Flip – flops is **sensitive** to signal change. They transfer data only at single time instant and data can't be changed till next signal change.
➤ Therefore they are used as **registers**.
4. It is an edge triggered circuit, means that the output and the next state input changes, when there's a change in the clock pulse whether it can may be **POSITIVE (+ve)** or **NEGATIVE (-ve)** clock pulse.

Comparison between Flip-flop and Latch

Flip-Flop	Latch
Flip-flop utilizes an edge triggering approach.	Latch follows a level triggering approach.
The clock signal is present.	The clock signal is absent.
You can design it using Latches along with a clock.	You can design it using Logic gates.
Flip-flop is sensitive to the applied input and the clock signal.	Latches are sensitive to the applied input signal- only when enabled.
It has a slow operating speed.	It has comparatively fast operating speed.
You can classify a flip-flop into a synchronous or asynchronous flip-flop.	A user cannot classify the Latch this way.
A flip-flop checks the inputs. It only changes the output at times defined by any control signal like the clock signal.	The latch responds to the changes in inputs continuously as soon as it checks the inputs.
A flip-flop is synchronous. It works based on the clock signal.	A latch is asynchronous. It does not work based on the time signal.



THANK YOU

Dr. Ananda M
Department of Electronics and Communication
anandam@pes.edu