

DIGITAL LOGIC

Gate :

- ✓ It is the basic building block of digital circuits
- ✓ which can take logical decisions & generate output either HIGH [5v or binary 1] or Low[0v or binary 0]
- ✓ Gate has one or more inputs but has only one output variable.

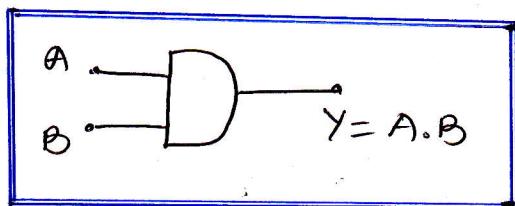
Types of Gates

- ✓ BASIC GATES
 - ✓ UNIVERSAL GATES
 - ✓ EXCLUSIVE GATES
- | | | |
|------------|-------------|--------------|
| • AND Gate | • NAND Gate | • X-OR Gate |
| • OR Gate | • NOR Gate | • X-NOR Gate |
| • NOT Gate | | |

1) AND Gate : It belongs to the category of basic Gates

(*) Defn: which has two or more inputs but has only one output terminal. When any one of the input is at low state output is also low, when all the applied inputs are at high state only then o/p is high.

(*) Symbol of AND Gate



(*) Truth Table

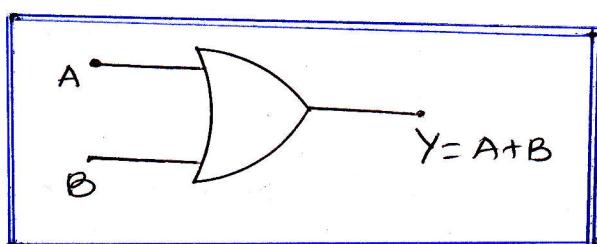
I/P VARIABLES		O/P VARIABLES
A	B	$Y = A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1

✓ AND gate performs logical multiplication i.e $(A) \cdot (A) = (A)$

(HIGH) (HIGH) = HIGH

2) OR Gate: It is also a basic Gate.

(*) Symbol



(*) Truth Table

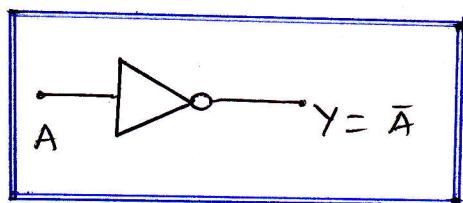
I/P VARIABLE		O/P VARIABLE
A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

(*) Defn: Which has two or more inputs but has only one input variable.

- If any one of the i/p is at high state then o/p is also high. If all the applied i/p are at low state only then o/p is low.
- OR Gate does logical Addition operation
ie HIGH + HIGH = HIGH \textcircled{O} $A + A = A$

3) NOT GATE: NOT gate is also a basic Gate

(*) Symbol



(*) Truth Table

I/p variable	O/p variable
A	$Y = \bar{A}$
0	1
1	0

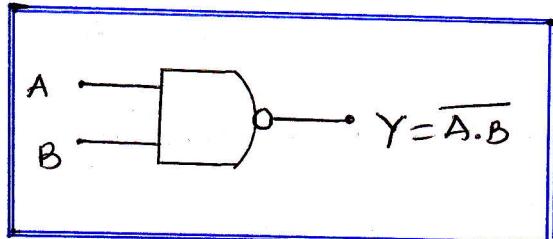
(*) Defn: Which only one i/p & only one o/p variable.

- O/p is complement or inverted part of the applied i/p
i.e. If input is high then o/p will be low
If input is low then o/p will be high.

4) NAND Gate: It is an Universal Gate

- NAND Gate is derived from AND gate & NOT Gate
- AND gate output is followed by NOT Gate hence NAND gate originates.

(*) Symbol



(*) Truth Table

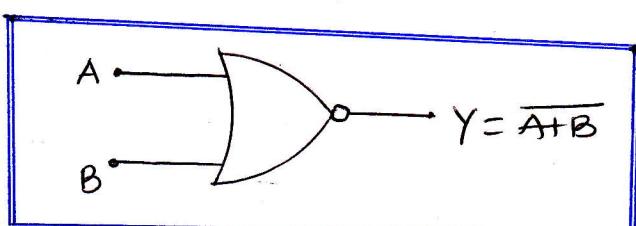
I/p variables		O/p variable $Y = \overline{A \cdot B}$
A	B	
0	0	1
0	1	1
1	0	1
1	1	0

(*) Defn: If any one of the input is at low state output is high. If all the applied inputs are at high state only then output is low.

5) NOR Gate: It is also an Universal Gate

- NOR Gate is derived from OR Gate & NOT Gate
- OR Gate output is followed by NOT gate hence NOR gate originates

(*) Symbol



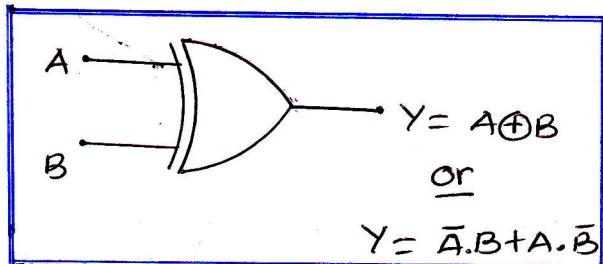
(*) Truth Table

I/p variables		O/p variable $Y = \overline{A+B}$
A	B	
0	0	1
0	1	0
1	0	0
1	1	0

(*) Defn: If any of the input is at high state then o/p is low, If all the applied inputs are at low only then o/p is HIGH.

6) X-OR Gate: It is a special purpose Gate

(*) Symbol



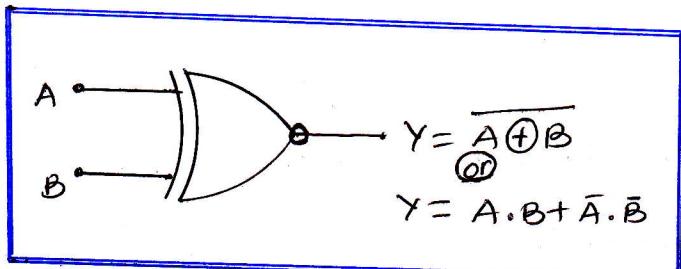
(*) Truth Table

I/p variables		O/p variable
A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

(*) Defn: When both the applied inputs are dissimilar then output is high, otherwise low.

7) X-NOR Gate: It is also a special purpose Gate

(*) Symbol



(*) Truth Table

I/p variables		O/p variable
A	B	$Y = \overline{A \oplus B}$
0	0	1
0	1	0
1	0	0
1	1	1

(*) Defn: When both the applied inputs are similar then output is high, otherwise low.

(#) Boolean ALGEBRA

(x) LAWS

\Rightarrow AND LAWS

$$\checkmark A \cdot 0 = 0$$

$$\checkmark A \cdot 1 = A$$

$$\checkmark A \cdot A = A$$

$$\checkmark A \cdot \bar{A} = 0$$

\Rightarrow OR LAWS

$$\checkmark A + 0 = A$$

$$\checkmark A + 1 = 1$$

$$\checkmark A + A = A$$

$$\checkmark A + \bar{A} = 1$$

\Rightarrow NOT LAW

$$\bar{\bar{A}} = A$$

\Rightarrow COMMUTATIVE LAW

$$\checkmark A + B = B + A$$

$$\checkmark A \cdot B = B \cdot A$$

\Rightarrow ASSOCIATIVE LAW

$$\checkmark (A + B) + C = A + (B + C)$$

$$\checkmark (A \cdot B) \cdot C = A \cdot (B \cdot C)$$

\Rightarrow DISTRIBUTIVE LAW

$$\checkmark A \cdot (B + C) = (A \cdot B) + (A \cdot C)$$

$$\checkmark (A + (B \cdot C)) = (A + B) \cdot (A + C)$$

Proof : Consider R.H.S i.e $(A + B) \cdot (A + C)$

$$\Rightarrow A[A + C] + B[A + C]$$

$$\Rightarrow \underbrace{A \cdot A}_A + A \cdot C + B \cdot A + B \cdot C$$

$$\Rightarrow \underbrace{A + A \cdot C}_1 + A \cdot B + B \cdot C$$

$$\Rightarrow A[\cancel{1 + C}] + A \cdot B + B \cdot C$$

$$\Rightarrow \underbrace{A + A \cdot B}_1 + B \cdot C$$

$$\Rightarrow A[\cancel{(1 + B)}] + B \cdot C$$

$$\Rightarrow A + (B \cdot C)$$

Hence L.H.S

#> DE-MORGAN'S THEOREM

i> First Law: Complement of Logical sum is equals to Logical product of individual complements,

$$\text{i.e } \overline{(A+B)} = (\bar{A}) \cdot (\bar{B})$$

ii> Second Law: Complement of Logical product is equals to Logical sum of individual complements.

$$\text{i.e } \overline{(A \cdot B)} = (\bar{A}) + (\bar{B})$$

[Hint: Split the complement & change the signs]

Proof:

I/p VARIABLES		$(A+B)$	$\bar{A} \cdot \bar{B}$	$\overline{(A \cdot B)}$	$(\bar{A}) + (\bar{B})$
A	B				
0	0	1	1	1	1
0	1	0	0	1	1
1	0	0	0	1	1
1	1	0	0	0	0

#] SIMPLIFICATION OF BOOLEAN EXPRESSION

Simplify the following boolean expressions by using laws of boolean algebra

$$\text{i> } M = \overline{\overline{x}\overline{y}\overline{z}} + \overline{\overline{x}\overline{y}\overline{z}} + \overline{x}\overline{y} + x\overline{y}$$



$$= \overline{\overline{x}\overline{y}\overline{z}} + \overline{x}\overline{y} + x\overline{y}$$

$$\therefore ABC + ABC = ABC$$

$$= \overline{x}\overline{y}[\overline{z}+1] + \overline{x}\overline{y}$$

$$\therefore [\overline{z}+1] = 1$$

$$= \overline{y}[\overline{x+x}]^1$$

$$\therefore M = \boxed{\overline{y}}$$

ii) Simplify $Y = \underline{ABC + AB} + A$

$$\begin{aligned}
 &= AB[\underline{C+1}] + A \\
 &= AB + A \\
 &= A[B+1] \\
 \therefore Y &= A
 \end{aligned}$$

iii) $Y = A\bar{B} + ABC + A[\underline{-B+A\bar{B}}]$

$$\begin{aligned}
 &= A\bar{B} + \underline{ABC} + \underline{AB} + \underline{A \cdot A\bar{B}} \\
 &= A\bar{B} + AB[C+1] \\
 &= A\bar{B} + AB \\
 &= A[\cancel{\bar{B}+B}]^1 \\
 \therefore Y &= A
 \end{aligned}$$

iv) $Y = AB + \bar{AC} + A\bar{B}C[AB+c]$

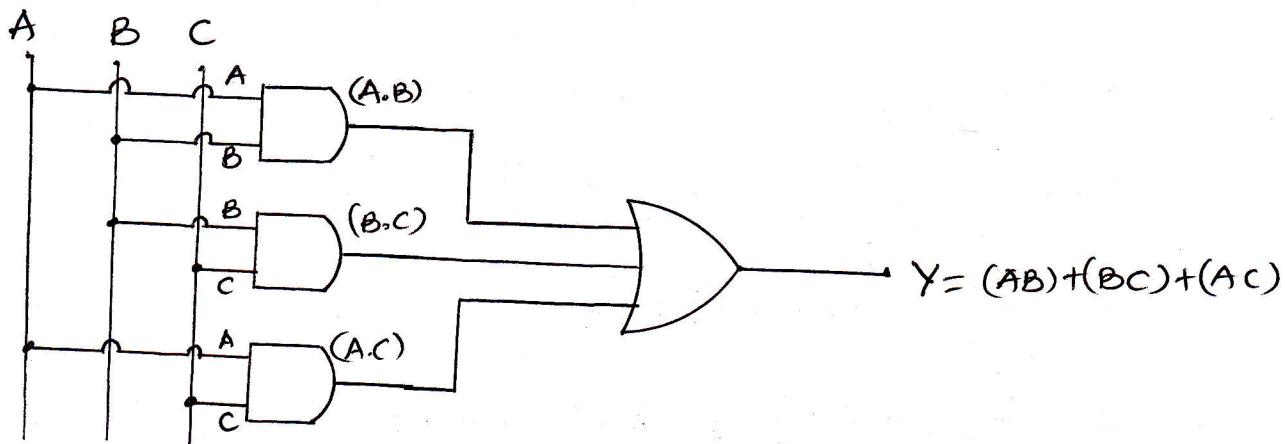
$$\begin{aligned}
 &= AB + [\bar{A} + \bar{c}] + (\cancel{A\bar{B}C} \cdot \cancel{AB}) + [\bar{A}\bar{B}C \cdot c] \\
 &= \underline{AB + \bar{A}} + \bar{C} + A\bar{B}C \\
 &= \bar{A} + B + \underline{\bar{C} + A\bar{B}C} \\
 &= \bar{A} + B + [(\bar{C} + A)(\bar{C} + \bar{B})(\cancel{\bar{C} + C}^1)] \\
 &= \bar{A} + B + [\bar{C}\bar{C} + \bar{C}\bar{B} + A\bar{C} + A\bar{B}] \\
 &= \bar{A} + B + [\bar{C} + \bar{C}\bar{B} + A\bar{C} + A\bar{B}] \\
 &= \bar{A} + B + [\bar{C}[1 + \cancel{\bar{B} + A}^1] + A\bar{B}] \\
 &= \bar{A} + B + [\bar{C} + A\bar{B}] = \bar{A} + B + \underline{A\bar{B} + \bar{C}} \\
 &= \bar{A} + B + \underline{A + \bar{C}} = (\cancel{\bar{A} + A}^1) + B + \bar{C} \\
 Y &= \underline{\underline{1}}
 \end{aligned}$$

v> Simplify & realize using only basic Gates

$$\begin{aligned}
 Y &= (A + \bar{B} + C) (\bar{A} + B + C) (\bar{A} + B) \\
 &= (A + \bar{B} + C) [A(\bar{A} + B + C) + B(\bar{A} + B + C)] \\
 &= [A + \bar{B} + C] [(A \cdot \cancel{\bar{A}})^0 + (AB) + (AC) + (\bar{A}B) + (\cancel{B} \cdot \cancel{B})^1 + (B \cdot C)] \\
 &= [A + \bar{B} + C] [0 + AB + AC + \cancel{\bar{A}B} + B + BC] \\
 &= [A + \bar{B} + C] [B[A + \bar{A} + 1 + C] + AC] \\
 &= [A + \bar{B} + C] [B + AC] \\
 &= A(B + AC) + \bar{B}(B + AC) + C(B + AC) \\
 &= BA + A \cdot AC + \cancel{\bar{B} \cdot B}^0 + \bar{B}AC + BC + AC \cdot C \\
 &= AB + \underline{AC} + A\bar{B}C + BC + \underline{AC} \\
 &= AB + \underline{AC} + BC + \underline{A\bar{B}C} \\
 &= AB + BC + AC[1 + \bar{B}]
 \end{aligned}$$

$$Y = AB + BC + CA$$

Implementation simplified expression using basic Gates,



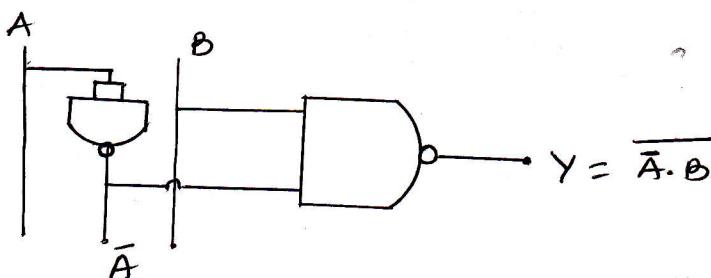
vii) Simplify the given boolean expression & implement using only NAND gates.

$$\begin{aligned}
 Y &= [A + \bar{B} + \bar{C}] [A + \bar{B} + C] \\
 &= A[A + \bar{B} + C] + \bar{B}[A + \bar{B} + C] + \bar{C}[A + \bar{B} + C] \\
 &= \underbrace{A \cdot A}_A + A\bar{B} + AC + \bar{B}A + \underbrace{\bar{B} \cdot \bar{B}}_{\bar{B}} + \bar{B}C + \bar{C}A + \bar{C}\bar{B} + \cancel{\bar{C}C}^0 \\
 &= \underbrace{A + A\bar{B} + AC + A\bar{B}}_A + \underbrace{\bar{B} + \bar{B}C}_0 + \underbrace{AC + \bar{C}\bar{B}}_0 \\
 &= A[\cancel{1 + \bar{B} + C + \bar{B} + C}]^1 + \bar{B}[\cancel{1 + C + \bar{C}}]^1 \\
 \therefore Y &= A + \bar{B}
 \end{aligned}$$

Implementation using only NAND gates.

$$\begin{aligned}
 Y &= \overline{(A + \bar{B})} = \overline{(A + \bar{B})} = \overline{(A \cdot \bar{B})}
 \end{aligned}$$

$$\Rightarrow Y = \overline{(A \cdot B)}$$



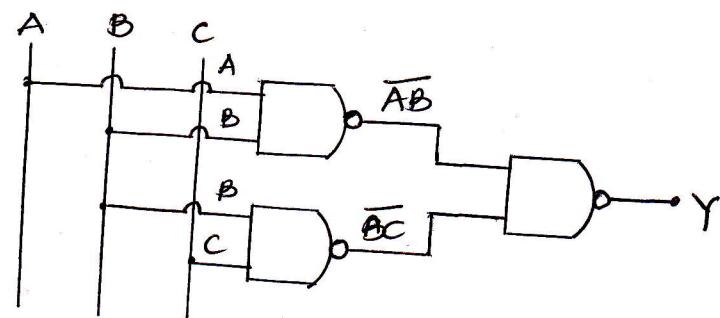
$$vii) Y = \underline{ABC} + A\bar{B}C + \underline{ABC}$$

$$\begin{aligned}
 &= AB[C + \bar{C}] + A\bar{B}C = AB + A\bar{B}C = A[B + \bar{B}C] \\
 &= A[(B + \cancel{\bar{B}})^1(B + C)] = A[B + C]
 \end{aligned}$$

$$Y = AB + BC$$

Implementation using only NAND gates.

$$Y = \overline{(AB + BC)} = \overline{(AB)} \cdot \overline{(BC)}$$

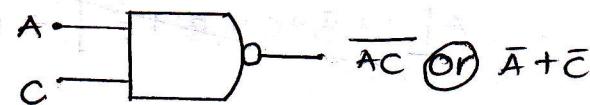


$$\begin{aligned}
 \text{viii) } Y &= \underbrace{A\bar{B}\bar{C}}_{\downarrow} + \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B} + \underline{\bar{A}C} \\
 &= \bar{B}\bar{C}[A+\bar{A}] + \bar{A}\bar{B} + \bar{A} + \bar{C} \\
 &= \bar{B}\bar{C} + \underline{\bar{A}\bar{B} + \bar{A} + \bar{C}} \\
 &= \bar{B}[\bar{B}+1] + \bar{A}[\bar{B}+1]
 \end{aligned}$$

$$Y = \bar{C} + \bar{A}$$

Implement using only NAND gates,

$$\begin{aligned}
 \therefore Y &= \overline{(\bar{C} + \bar{A})} = \overline{(\bar{C} \cdot \bar{A})} \\
 Y &= \overline{(C \cdot A)}
 \end{aligned}$$



$$\begin{aligned}
 \text{ix) } M &= \overline{[(XY + X\bar{Y}Z)]} + \overline{[X[Y + X\bar{Y}]]} \\
 &= \overline{[(XY + X\bar{Y}Z)]} + \overline{[XY + \underline{X \cdot X\bar{Y}}]} \\
 &= [XY + X\bar{Y}Z] + \overline{[XY + X\bar{Y}]} \\
 &= XY[1+Z] + \overline{[X[Y + \bar{Y}]]} \\
 &= [XY] \cdot [\bar{X}] \\
 &= XY \cdot \bar{X}
 \end{aligned}$$

$$\underline{\underline{M=0}}$$

Follows $\Rightarrow M=0$ \Rightarrow $M=0$

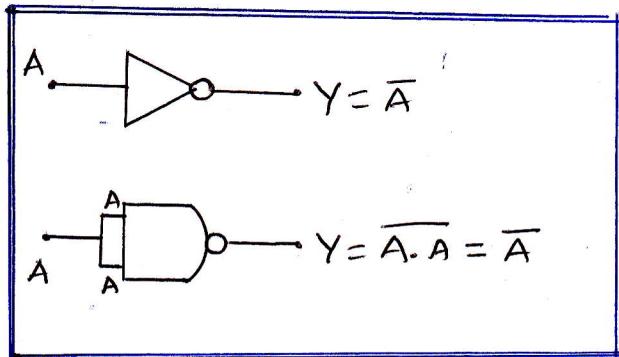


#> NAND as UNIVERSAL GATE:

→ NAND gate can act or mimic like all the basic gates, NOR Gate & as well as exclusive gates hence it is called as Universal Gate.

1> NAND as NOT Gate:

(*) Symbol of NOT Gate

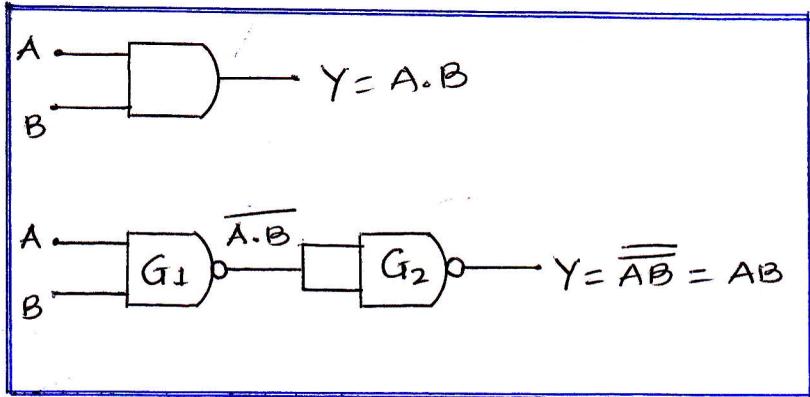


(*) Truth Table of NOT Gate

I/P VARIABLE	O/P VARIABLE
A	$Y = \bar{A}$
0	1
1	0

2> NAND as AND Gate:

(*) Symbol of AND Gate

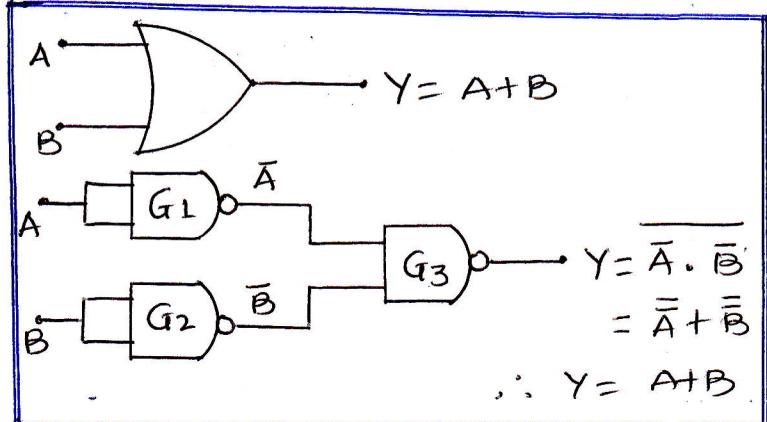


(*) Truth Table of AND Gate

I/P VARIABLES		O/P VARIABLE
A	B	$Y = A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1

3> NAND as OR Gate:

(*) Symbol of OR Gate

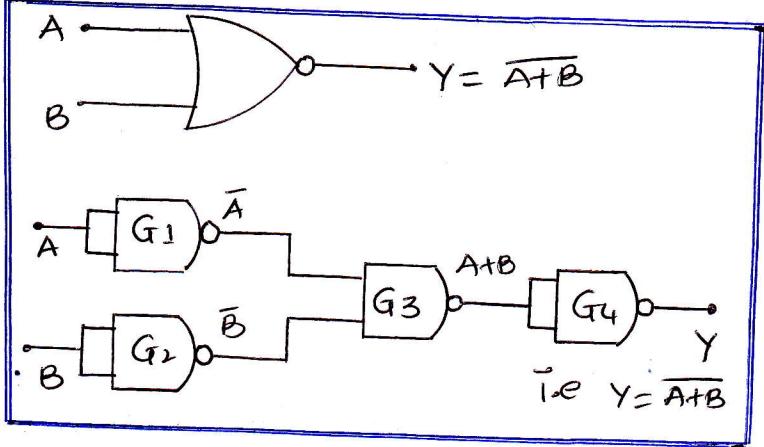


(*) T.T of OR Gate

I/P VARIABLEX		O/P VARIABLE
A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

4) NAND as NOR Gate:

(*) Symbol of NOR Gate

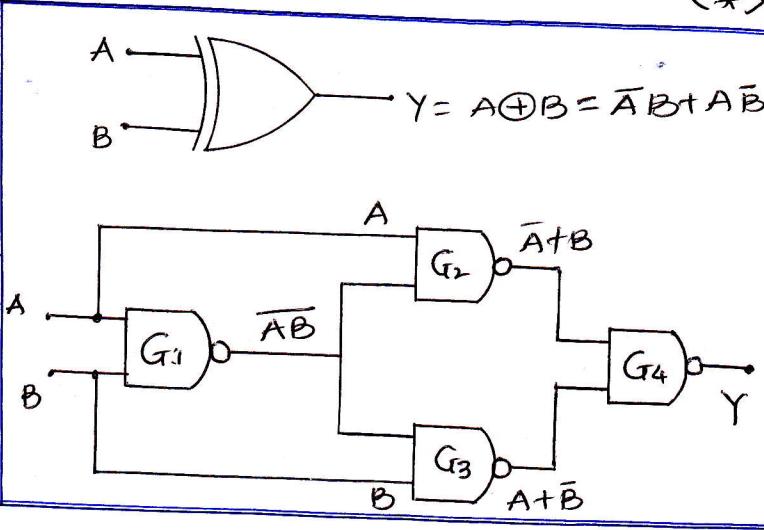


(*) Truth Table of NOR Gate

I/P VARIABLES		O/P VARIABLE
A	B	Y = A + B
0	0	1
0	1	0
1	0	0
1	1	0

5) NAND as X-OR Gate:

(*) Symbol of X-OR Gate

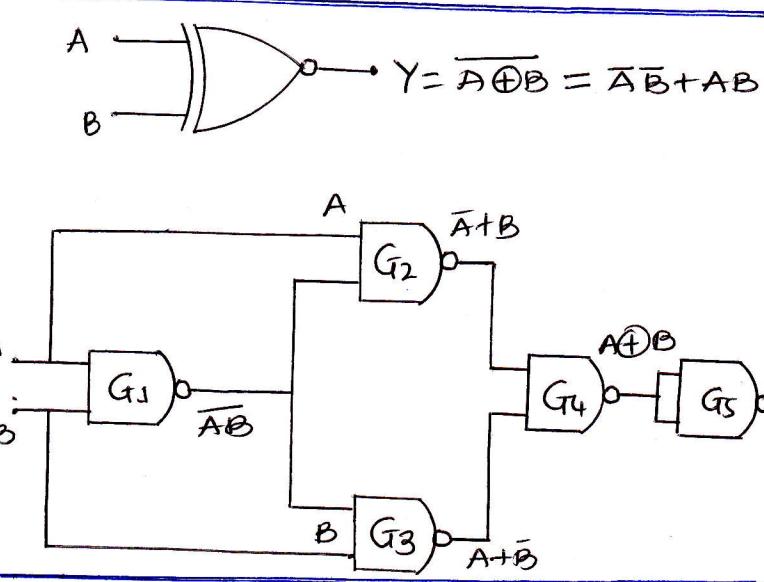


(*) Truth Table of X-OR Gate

I/P VARIABLES		O/P VARIABLE
A	B	Y = A ⊕ B
0	0	0
0	1	1
1	0	1
1	1	0

6) NAND as X-NOR Gate:

(*) Symbol of X-NOR Gate



(*) Truth Table of X-NOR Gate

I/P VARIABLES		O/P VARIABLE
A	B	Y = A ⊕ B
0	0	1
0	1	0
1	0	0
1	1	1

(*) Simplification of NAND & X-OR & X-NOR Gates

From the case(5) & case(6)

• Output of Gate 1 is, $\overline{A \cdot B}$

• Output of Gate 2 is $\overline{(\overline{A \cdot B}) \cdot A}$

$$\therefore \overline{\overline{(A \cdot B)}} + \overline{A}$$

$$= AB + \overline{A} = (\overline{A} + A)^1 \cdot (\overline{A} + B)$$

$$= \overline{A} + B$$

• Output of Gate 3 is $\overline{(\overline{A \oplus B}) \cdot B}$

$$\therefore \overline{\overline{A \oplus B}} + \overline{B}$$

$$= AB + \overline{B} = (A + \overline{B}) \cdot (\overline{B} + \overline{B})^1$$

$$= A + \overline{B}$$

• Output of Gate 4 is $\overline{(\overline{A} + B) \cdot (A + \overline{B})}$

$$= \overline{(\overline{A} + B)} + \overline{(A + \overline{B})}$$

$$= (\overline{\overline{A}} \cdot \overline{B}) + (\overline{A} \cdot \overline{\overline{B}}) = (A \overline{B} + \overline{A} \cdot B)$$

$$= \overline{A}B + A\overline{B} \quad \text{or}$$

• Output of Gate 5 [for X-NOR Gate] is,

$$\overline{(A \cdot B) + (A \cdot \overline{B})}$$

$$= \overline{(A \cdot B)} \cdot \overline{(A \cdot \overline{B})} = (\overline{\overline{A}} + \overline{B}) \cdot (\overline{A} + \overline{\overline{B}})$$

$$= (A + \overline{B})(\overline{A} + B) = A[\overline{A} + B] + \overline{B}[\overline{A} + B]$$

$$= A\cancel{\overline{A}}^0 + A\overline{B} + \overline{B}\cancel{\overline{A}}^0 + \overline{B}B^0$$

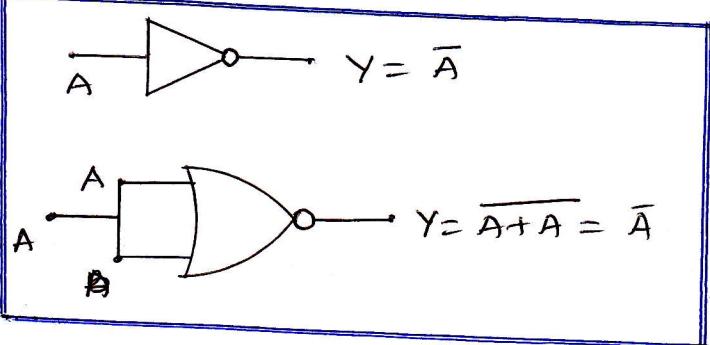
$$\therefore = \overline{A}\overline{B} + AB$$

NOR GATE as UNIVERSAL GATE

→ All the basic gates, NAND gates & exclusive gates can be realized by using NOR Gate, hence it is also called as an "Universal Gate".

1) NOR as NOT Gate :

(*) Symbol of NOT Gate

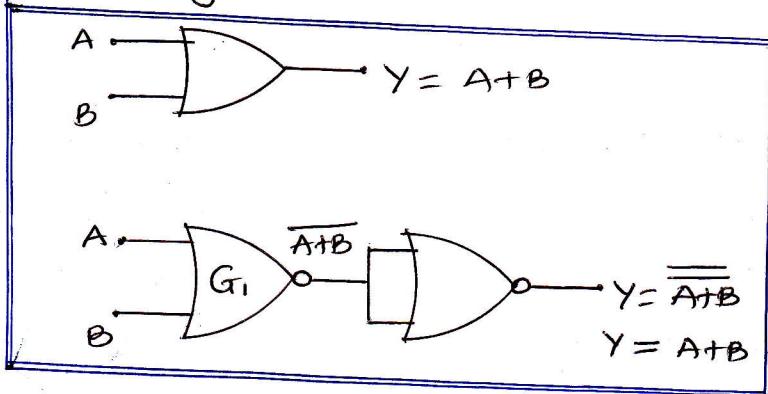


(*) Truth Table of NOT Gate

I/p variable	O/p variable
A	$Y = \bar{A}$
0	1
1	0

2) NOR as OR Gate :

(*) Symbol of OR Gate

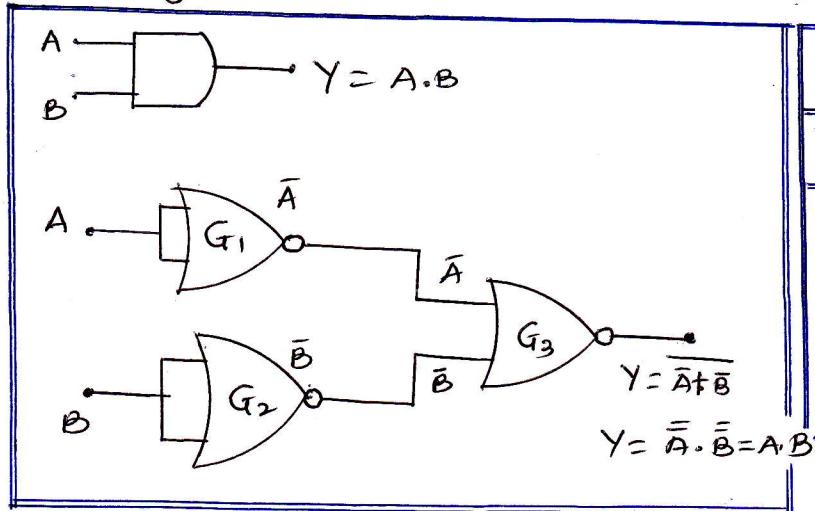


(*) Truth Table of OR Gate

I/p variables		O/p variable
A	B	$Y = (A+B)$
0	0	0
0	1	1
1	0	1
1	1	1

3) NOR as AND Gate :

(*) Symbol of AND Gate



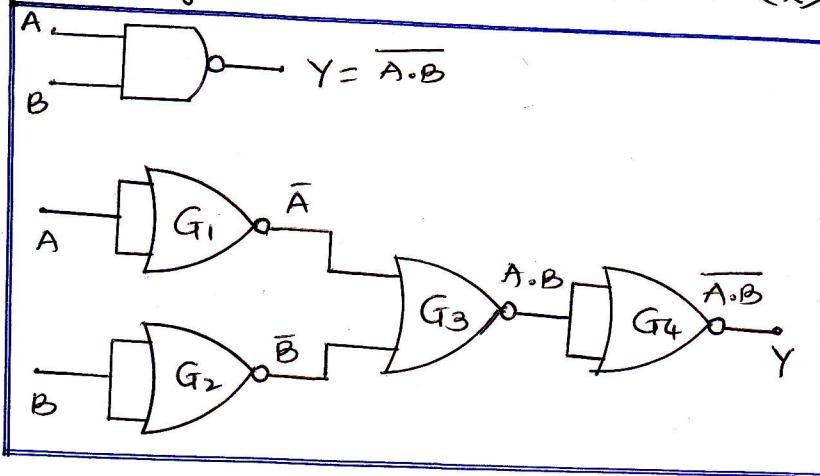
(*) Truth Table of AND Gate

I/p variables		O/p variable
A	B	$Y = (A \cdot B)$
0	0	0
0	1	0
1	0	0
1	1	1

<*> 4) NOR Gate as NAND Gate:

(*) Symbol of NAND Gate

(*) Truth Table of NAND Gate

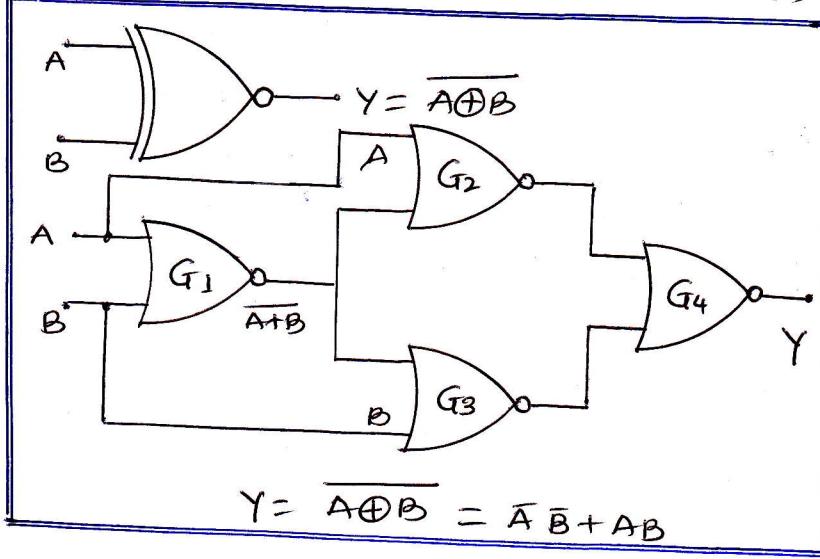


I/P VARIABLES		O/P Variable
A	B	$Y = \overline{A+B}$
0	0	1
0	1	1
1	0	1
1	1	0

<*> 5) NOR Gate as X-NOR Gate:

(*) Symbol of X-NOR Gate

(*) Truth Table of X-NOR Gate

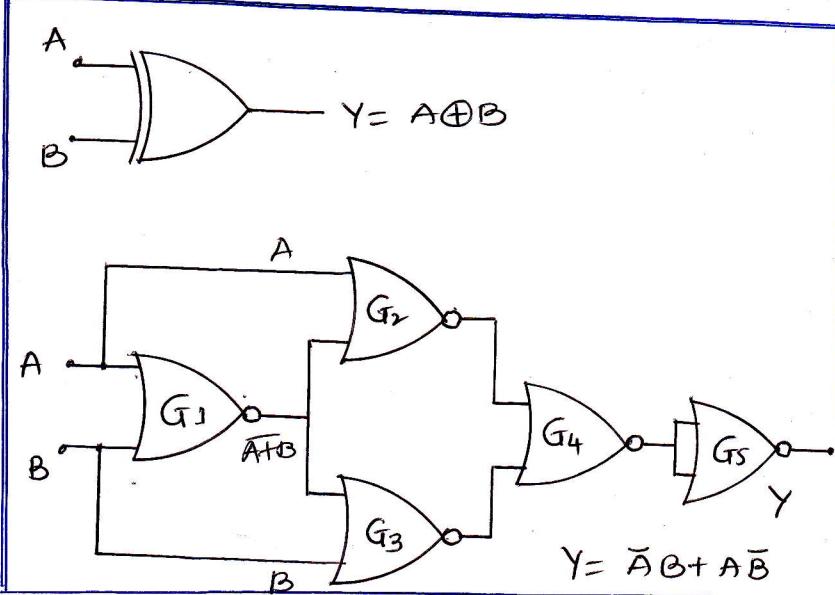


I/P variables		O/P variable
A	B	$Y = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	1

<*> 6) NOR Gate as X-OR Gate:

(*) Symbol of X-OR Gate

(*) Truth Table of X-OR Gate



I/P variables		O/P variable
A	B	$Y = \overline{A+B}$
0	0	0
0	1	1
1	0	1
1	1	0

<*> Simplification of NOR & X-OR & X-NOR Gates

From the Case(5) & Case(6)

- Output of Gate 1 is $\overline{A+B}$

- Output of Gate 2 is $\overline{(A)} + \overline{\overline{A+B}}$

$$\Rightarrow (\bar{A}) \cdot (\overline{\overline{A+B}})$$

$$\Rightarrow (\bar{A}) \cdot (A+B) = (\cancel{\bar{A} \cdot A})^0 + \bar{A} \cdot B$$

$$\Rightarrow \bar{A} \cdot B$$

- Output of Gate 3 is $\overline{(B)} + \overline{\overline{A+B}}$

$$\Rightarrow (\bar{B}) \cdot (\overline{\overline{A+B}})$$

$$\Rightarrow (\bar{B}) \cdot (A+B) = (\bar{B} \cdot \bar{A}) + (\bar{B} \cdot B)^0$$

$$\Rightarrow A \cdot \bar{B}$$

- Output of Gate 4 is $\overline{(\bar{A} \cdot B) + (A \cdot \bar{B})}$

$$\therefore \overline{A \oplus B}$$

$$[\because (\bar{A} \cdot B) + (A \cdot \bar{B}) = A \oplus B]$$

hence X-NOR Gate

- Output of Gate 5 is $\overline{\overline{A \oplus B}}$

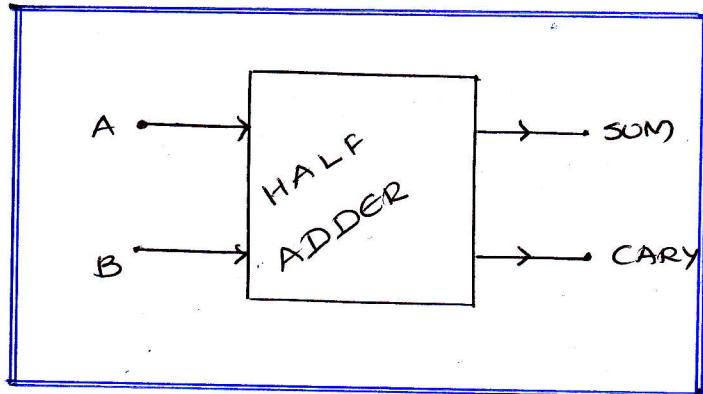
$$\therefore A \oplus B = \bar{A}B + A\bar{B}$$

Hence the X-OR Gate

<#> HALF ADDER

(*) Defn: A logic circuit which can add two bits at a time & generates sum & carry as output variable.

(*) Block Diagram



(*) Truth Table

I/P VARIABLES		O/P VARIABLES	
A	B	CARRY	SUM
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

✓ SUM Column is the output status of X-OR Gate, hence boolean expression for SUM is,

$$\text{SUM} = (\bar{A}B + A\bar{B})$$

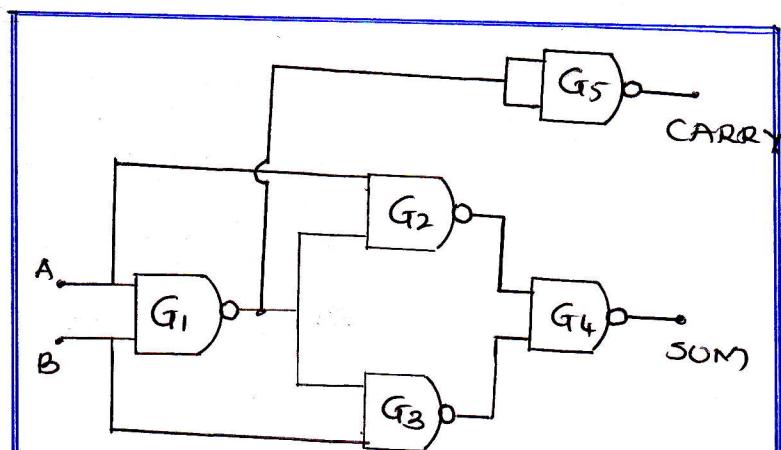
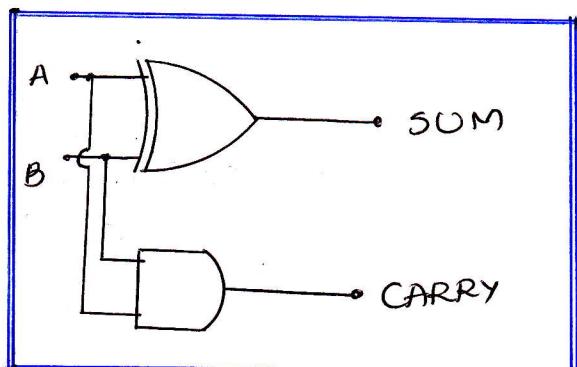
✓ CARRY Column is the output status of AND Gate, hence boolean expression for CARRY is,

$$\text{CARRY} = (A \cdot B)$$

(*) Realization of HALF ADDER Using Gates

(i) Using basic Gates & (ii) Using only NAND Gates

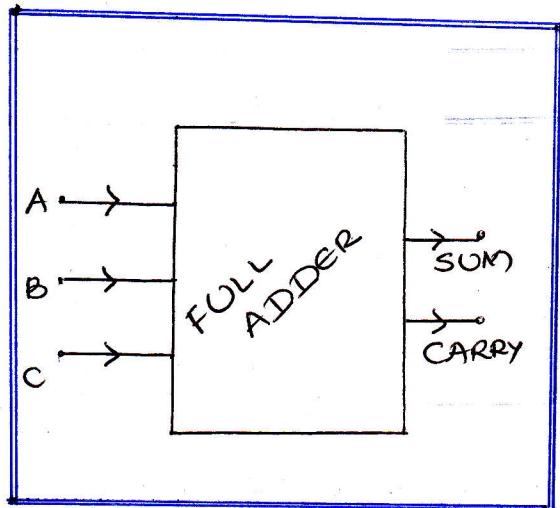
X-OR



(#) FULL ADDER

(*Defn: A logic circuit which can add three bits at a time & generates SUM & CARRY as output variables.

(* BLOCK DIAGRAM)



(* Truth Table)

I/P VARIABLES			O/P VARIABLES	
A	B	C	CARRY	SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	1
1	1	1	1	0

$$\cdot \text{SUM} = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC \quad \underline{\text{or}} \quad A \oplus B \oplus C$$

$$\cdot \text{CARRY} = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

Simplification of CARRY Expression

$$\text{CARRY} = \bar{A}BC + A\bar{B}C + \underline{AB\bar{C}} + ABC$$

$$= \bar{A}BC + A\bar{B}C + AB[\bar{C} + C]$$

$$= \bar{A}BC + \underline{A\bar{B}C + AB}$$

$$= \bar{A}BC + A[\bar{B}C + B]$$

$$= \bar{A}BC + A[B + C]$$

$$= \underline{\bar{A}BC + AB} + AC$$

$$= B[\bar{A}C + A] + AC$$

$$= B[A + C] + AC$$

$$[\because \bar{B}C + B = (\bar{B} + B)(C + B)]$$

$$[\bar{A}C + A = (\bar{A} + A)(C + B)]$$

$$\text{CARRY} = AB + BC + AC$$

$$\checkmark \text{ SUM} \Rightarrow \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC = [A \oplus B] \oplus C$$

Consider R.H.S $[A \oplus B] \oplus C$

$$\Rightarrow [\bar{A}B + A\bar{B}] \oplus C$$

$$\text{Let } (\bar{A}B + A\bar{B}) = m$$

$$\therefore m \oplus C = \bar{m}C + \bar{C}m \text{ now substitute "m" value}$$

$$\Rightarrow \overline{(\bar{A}B + A\bar{B})} \cdot C + \bar{C} \cdot (\bar{A}B + A\bar{B})$$

$$\Rightarrow (\bar{A}\bar{B} + AB) \cdot C + \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C}$$

$$\Rightarrow \bar{A}\bar{B}C + ABC + \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C}$$

Hence the L.H.S

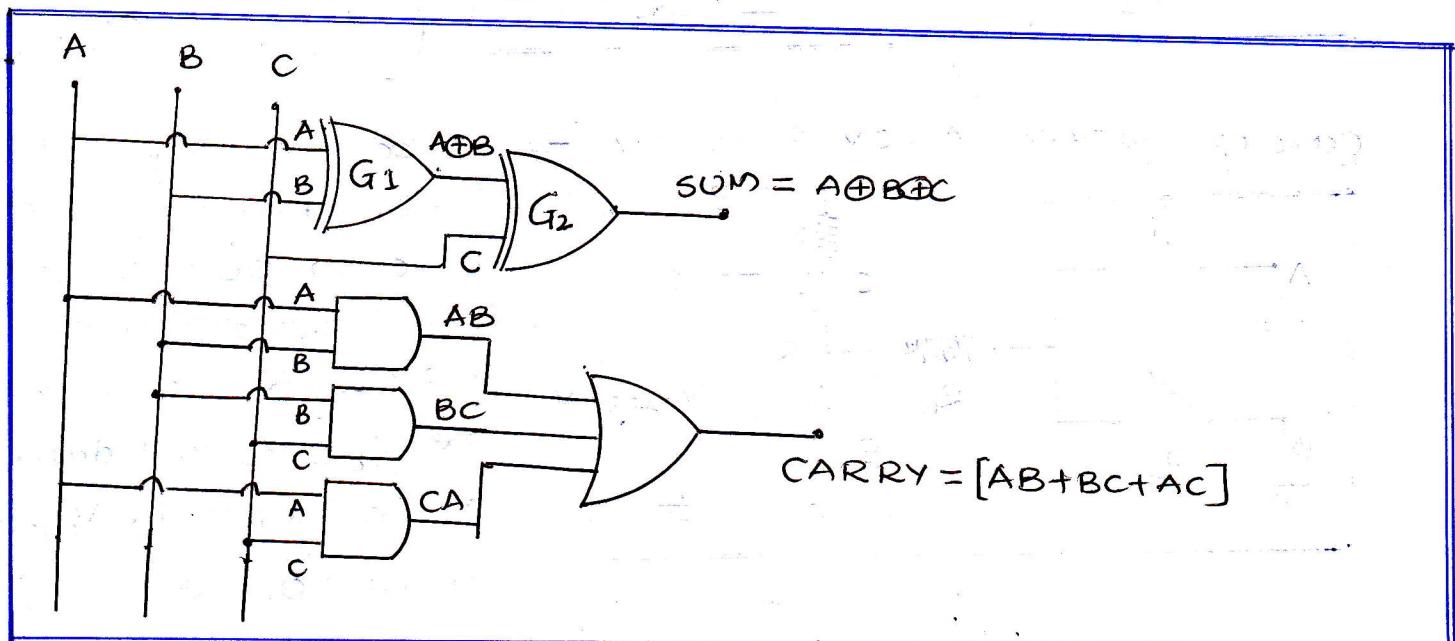
\therefore Simplified SUM & CARRY expressions are,

$$\checkmark \text{ SUM} = (A \oplus B) \oplus C$$

$$\checkmark \text{ CARRY} = AB + BC + AC$$

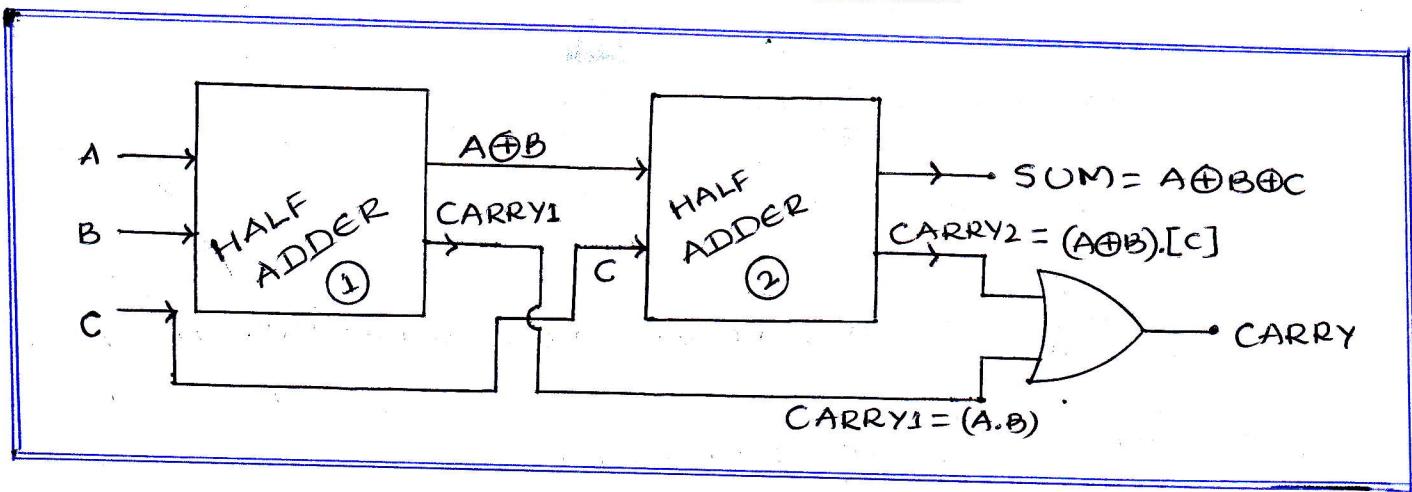
*> Implementation of FULL ADDER USING BASIC GATES

Eg X-OR Gates



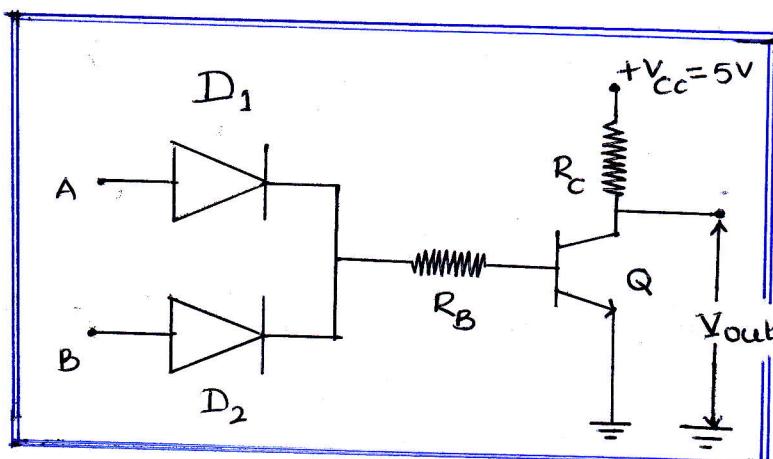
#> IMPLEMENTATION OF FULL ADDER USING BLOCK DIAGRAM

OF TWO HALF ADDERS



#> DTL NOR GATE :

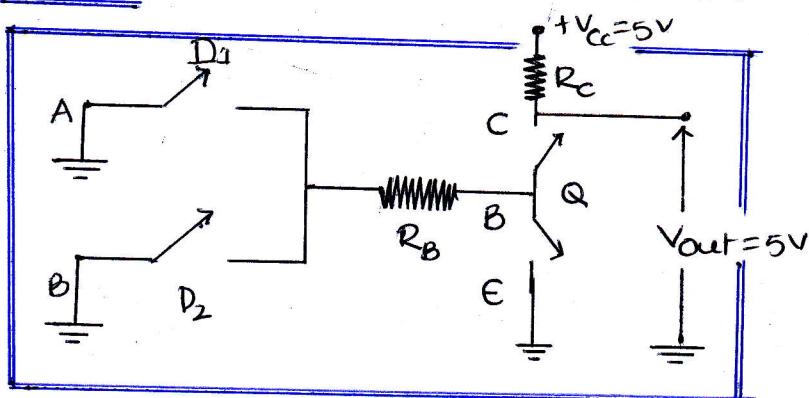
⇒ Constructing a digital device NOR Gate by analog components like Diodes & Transistor hence it is called as Diode-Transistor-Logic [DTL].



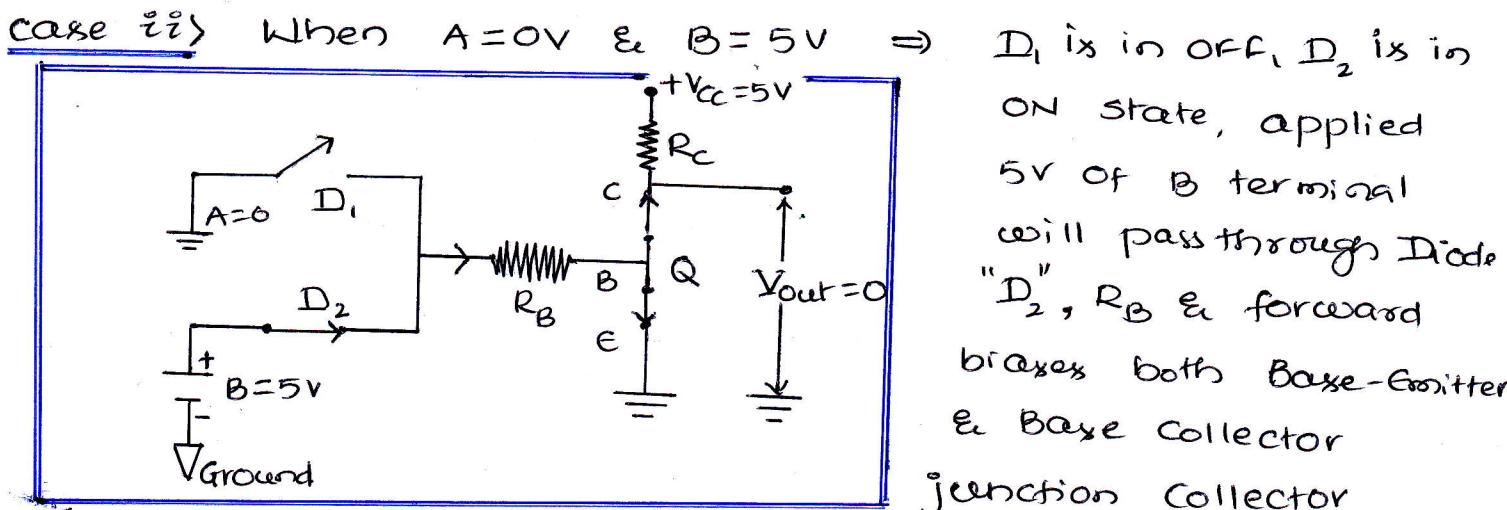
(*> T.T for NOR Gate

I/P VARIABLES		O/P VARIABLE
A	B	$Y = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

Case i> When A=0V & B=0V ⇒ Diodes D₁ & D₂ are

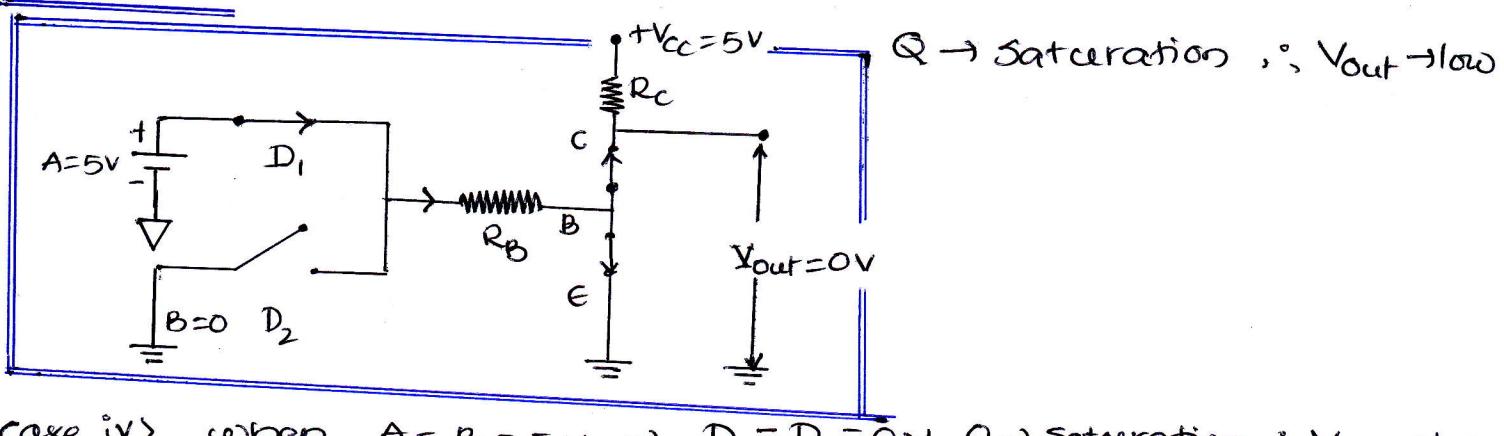


in OFF state hence acts like open switch. Therefore transistor is driven into cut-off. Thus all the V_{cc} [5V] will drop across output i.e V_{out} = 5V
∴ HIGH → Output.

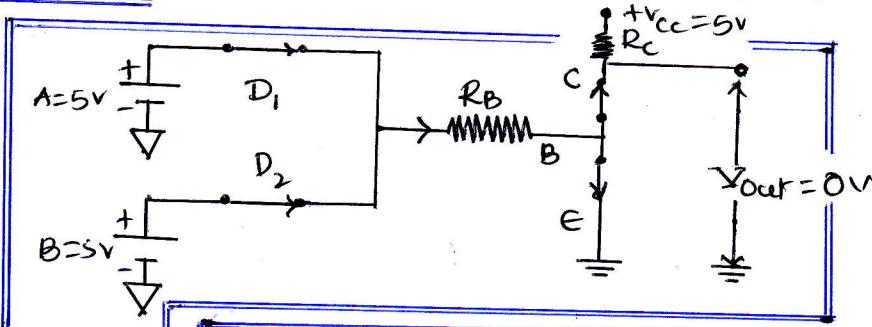


[∴ when transistor is operated under saturation region collector is connected to emitter through base region but emitter terminal is connected to ground hence $V_{out} \rightarrow 0$]

case iii) when $A=5V$ & $B=0V \Rightarrow D_1=ON, D_2=OFF$



case iv) when $A=B=5V \Rightarrow D_1=D_2=ON, Q \rightarrow$ Saturation $\therefore V_{out} \rightarrow low$



I/P VARIABLES		DIODE CONDITION		TRANSISTOR CONDITION		V _{out}
A	B	D ₁	D ₂	Q		
0	0	OFF	OFF	CUT-OFF		HIGH
0	5	OFF	ON	SATURATION		LOW
5	0	ON	OFF	SATURATION		LOW
5	5	ON	ON	SATURATION		LOW