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Unit-3 Digital Electronics

Other Logical Operation, Digital Logic gates (XOR and XNOR)

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Other Logical Operation, Digital Logic gates (XOR and XNOR)

- * XOR Gate is a digital logic Gate which has two or more inputs and only one output that performs Exclusive OR operation. Hence it is also called as Ex-OR or XOR
- For two input XOR gate output is **logic-1** only when one of its input is logic-1 (unequal input i.e..A = 0 and B = 1 or A = 1 and B = 0).
- ❖ Output of XOR gate is logic-0 if both inputs are same (i.e., A = 0 and B = 0 or A = 1 and B = 1)
- Truth Table of XOR Gate:

| Input A | Input B | Output Y |
|---------|---------|----------|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |



$$\begin{array}{c} A \\ B \end{array} \begin{array}{c} \\ \end{array} \end{array} \begin{array}{c} \\ \end{array} \end{array} \begin{array}{c} \\ \end{array} \end{array} \begin{array}{c} \\ \end{array} \begin{array}{c} \\ \end{array}$$

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* XOR gate performs modulo sum operation without including carry. i.e., 0+0=0, 0+1=1, 1+0=1, 1+1=0 (carry 1)

❖ Truth Table

| Α | В | Υ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

$$Y = A'.B + A.B'$$

$$Y = A XOR B$$

$$Y = A \oplus B$$

$$A.B' + A'.B = A \oplus B$$

LHS =
$$A.B' + A'.B$$

Case1: If
$$A = 0$$
 and $B = 0$
 $0.0' + 0'.0 = 0.1 + 1.0 = 0$

Case2: If
$$A = 0$$
 and $B = 1$
0.1' + 0'.1 = 0.0 + 1.1 = 1

Case3: If
$$A = 1$$
 and $B = 0$
1.0' + 1'.0 = 1.1 + 0.0 = 1

Case4: If
$$A = 1$$
 and $B = 1$
1.1' + 1'.1 = 1.0 + 0.1 = 0

Hence
$$Y = A \oplus B = A.B' + A'.B$$

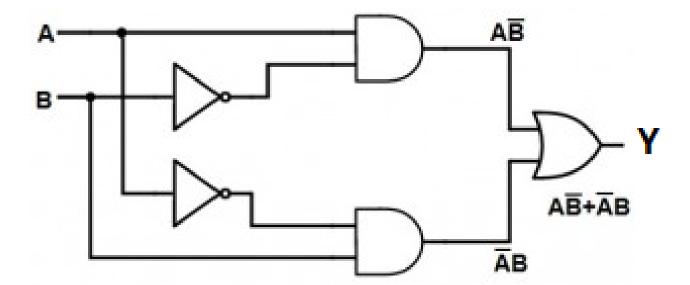
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Implementation of XOR Gate using basic gates:

$$Y = A \oplus B = A.B' + A'.B$$

Logic Diagram







Reference: "Digital Design with an Introduction to Verilog HDL" M Morris Mano, Michale D Ciletti

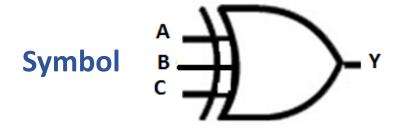
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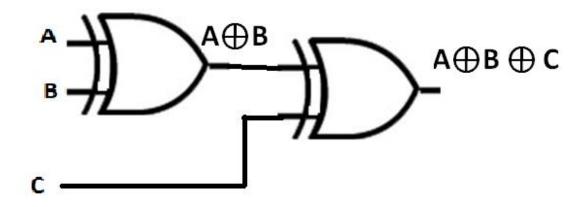


❖ 3 - Input XOR Gate: $Y = A \oplus B \oplus C$

Truth Table

| Α | В | С | А⊕В | A⊕B⊕C |
|---|---|---|-----|--------------|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 |





Associative Law: $(A \oplus B) \oplus C = A \oplus (B \oplus C)$

Even or odd Parity Bits

Other Logical Operation, Digital Logic gates (XOR and XNOR)



- **XNOR Gate**: Logical Complement of XOR Gate
- For two input XNOR Gate if both inputs are same i.e., A = 0 and B = 0 or A = 1 and B = 1. Then output of logic gate is logic-1 (High). Output of XNOR is logic-0 if inputs are unequal.
- Equality detector

Truth Table

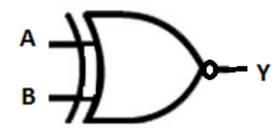
| Input A | Input B | Output Y |
|---------|---------|----------|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

***** Boolean Expression

$$Y = A.B + A'.B'$$

$$Y = A \odot B$$

❖ Symbol



Other Logical Operation, Digital Logic gates (XOR and XNOR)



XNOR Gate:

$$Y = (A \bigoplus B)'$$

$$Y = (A.B' + A'. B)'$$

De Morgan's Theorem

$$Y = (A.B')'.(A'.B)'$$

$$Y = (A'+B) \cdot (A + B')$$

$$Y = A'. A + A'.B' + A.B + B.B'$$

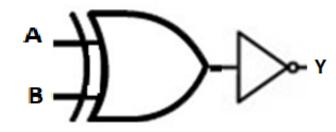
$$Y = 0 + A'.B' + A.B + 0$$

$$Y = A'.B' + A.B$$

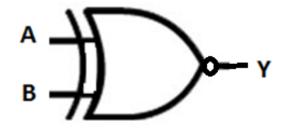
$$Y = (A \oplus B)' = A \odot B$$

 $Y = (A XOR B)' = (A XNOR B)$

Logic Diagram:



❖ Symbol:



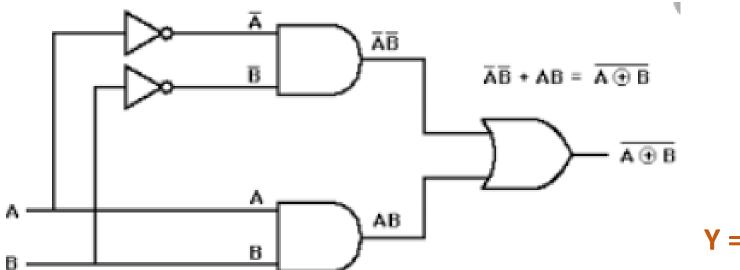
Other Logical Operation, Digital Logic gates (XOR and XNOR)



❖ Implement the XNOR Gate using basic gates:

$$Y = A'.B' + A.B$$

Logic Diagram:



$$Y = (A \oplus B)' = A \odot B$$

Other Logical Operation, Digital Logic gates (XOR and XNOR)



Properties of XOR Gate:

- \triangleright Identity element: A \bigoplus 0 = A
- ➤ A ⊕ 1 = A'
- \rightarrow A \bigoplus A = 0
- \triangleright Commutative Law: A \bigoplus B = B \bigoplus A
- \triangleright Associative Law : A \oplus (B \oplus C) = (A \oplus B) \oplus C

| A 47 | |
|------------------------|--|
| B = 1 | |

| Input A | Input B | Output Y |
|---------|---------|----------|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Other Logical Operation, Digital Logic gates (XOR and XNOR)



Applications of XOR and XNOR

- > XOR gate is used in processor's Arithmetic Logic Unit (ALU) for binary addition.
- > XOR logic gate is used to generate pseudorandom numbers in hardware.
- > To generate parity bits and error detection
- > Equality detector



THANK YOU

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