ELECTRONIC PRINCIPLES AND DEVICES

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ELECTRONIC PRINCIPLES AND DEVICES

Unit-3 Digital Electronics

Combinational Logic Circuits: Half Adder and Full adder

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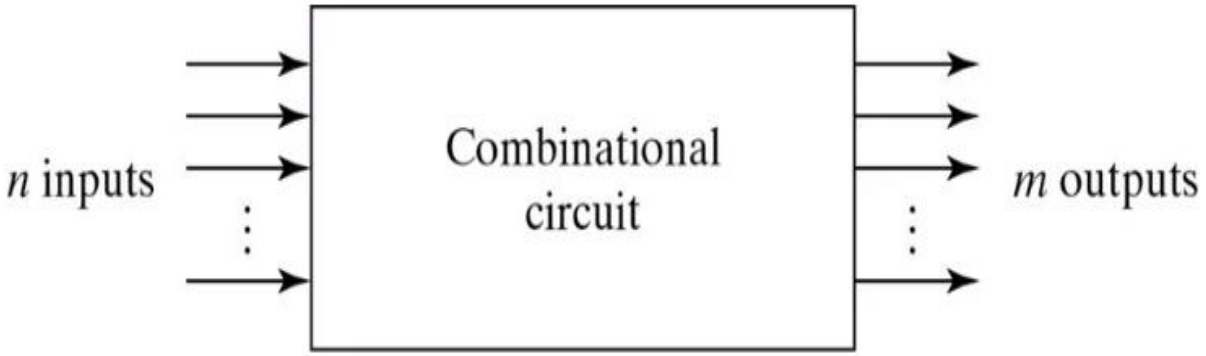
Combinational Logic Circuits: Half Adder and Full adder

❖ **Combinational circuits** are constructed by interconnection of logic gates.
whose outputs at any time are determined from only the present combination of inputs



❖ A combinational circuit performs an operation that can be specified logically by a set of **Boolean functions**

❖ Examples: Binary Adders, Multiplexers, etc.

Combinational Logic Circuits: Half Adder and Full adder

❖ Half Adder

- ➢ x and y are the two binary inputs
- ➢ Sum (s) and Carry (c) are the two binary outputs

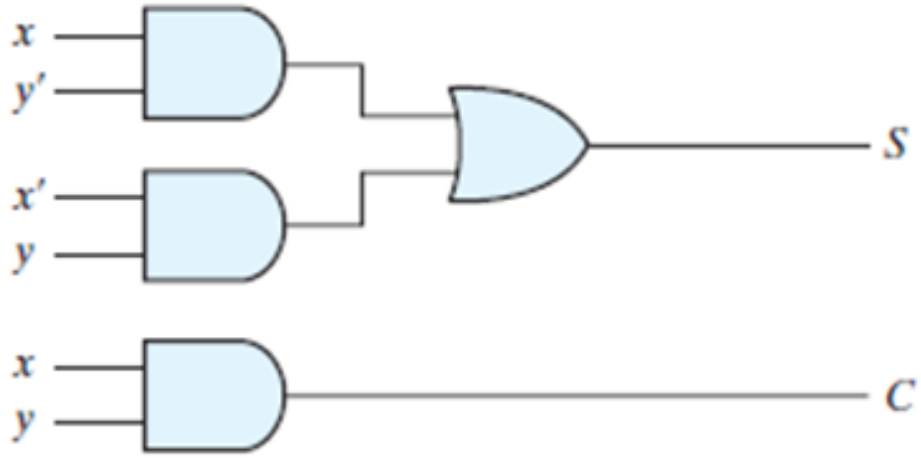
Boolean Expression:

$s = x'.y + x.y'$

$c = x.y$

Truth Table

x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



Logic Diagram

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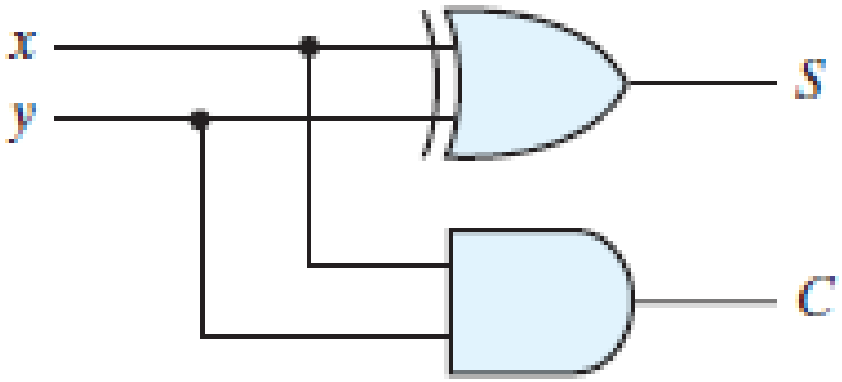
Combinational Logic Circuits: Half Adder and Full adder

❖ **Half Adder:** $s = x \oplus y$

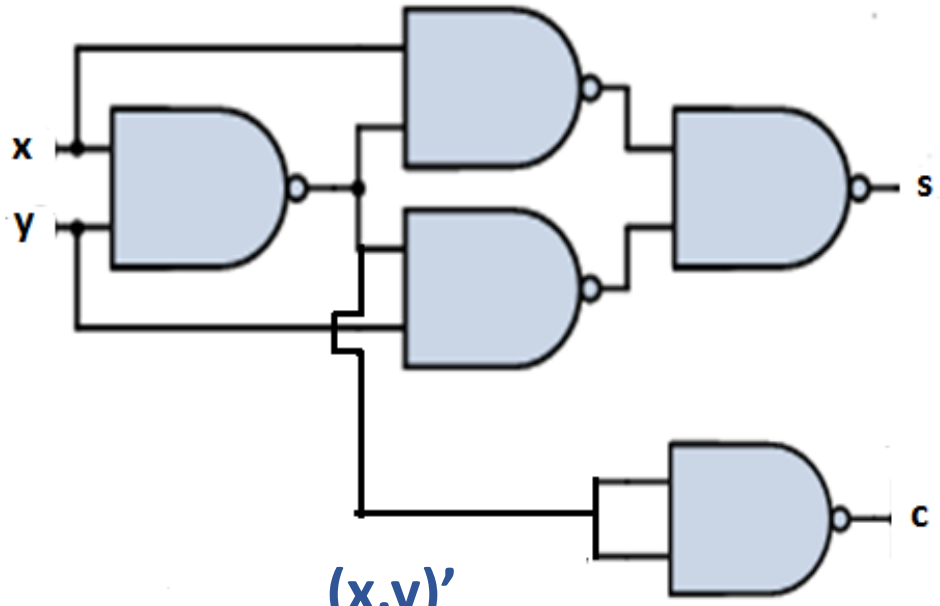
$c = x.y$

Sum expression: $s = x'.y + x.y'$

❖ **Half Adder using Logic Gates**



❖ **Half Adder using NAND Gates only**



(x.y)'

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Combinational Logic Circuits: Half Adder and Full adder

❖ Full Adder:

- x, y and z are three binary inputs.
- S is sum and C is carry outputs

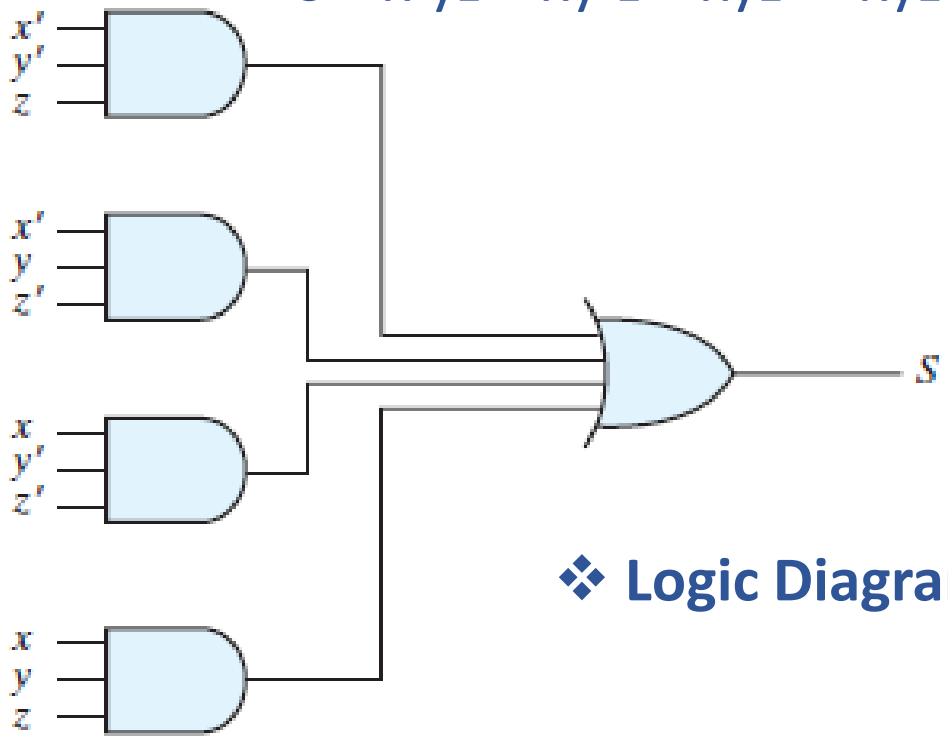
❖ Truth Table:

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

❖ Boolean Expression:

$S = x'y'z + x'yz' + xy'z' + xyz$

$C = x'yz + xy'z + xyz' + xyz$



❖ **Logic Diagram**

Reference: "Digital Design with an Introduction to Verilog HDL" M Morris Mano, Michale D Ciletti

Combinational Logic Circuits: Half Adder and Full adder

❖ Full Adder:

➢ **Carry Expression**:

C = x'yz + xy'z + xyz' + xyz

C = x'yz + xy'z + xy (z'+z)

C = x'yz + xy'z + xy

C = x'yz + x(y'z + y) Absorption Law

C = x'yz + x(z + y)

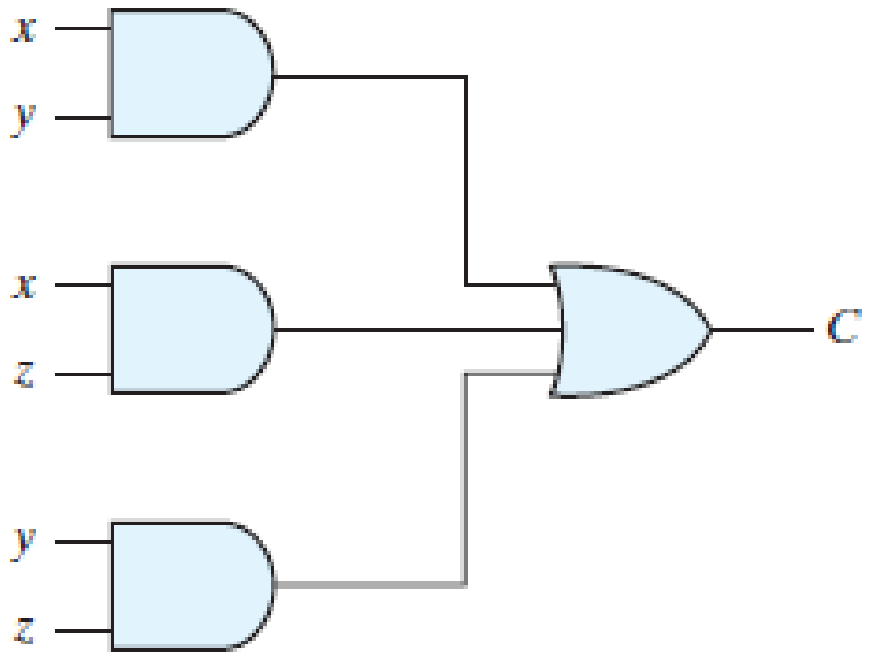
C = x'yz + xz + xy

C = z(x'y + x) + xy

C = z(y + x) + xy

C = yz + xz + xy

❖ **Logic Diagram**



Reference: "Digital Design with an Introduction to Verilog HDL" M Morris Mano, Michale D Ciletti

Combinational Logic Circuits: Half Adder and Full adder

- **Boolean Expression for Sum:**

$S = x'y'z + x'yz' + xy'z' + xyz$

$S = x' (y'z + yz') + x (y'z' + yz)$

$S = x' (y \oplus z) + x ((y \oplus z)')$

$\mathbf{S = x \oplus (y \oplus z)}$

- **Boolean Expression for Carry:**

$C = x'yz + xy'z + xyz' + xyz$

$C = z. (x'y + xy') + xy (z' + z)$

$C = z. (x \oplus y) + xy .(1)$

$\mathbf{C = (x \oplus y).z + xy}$

Reference: "Digital Design with an Introduction to Verilog HDL" M Morris Mano, Michale D Ciletti

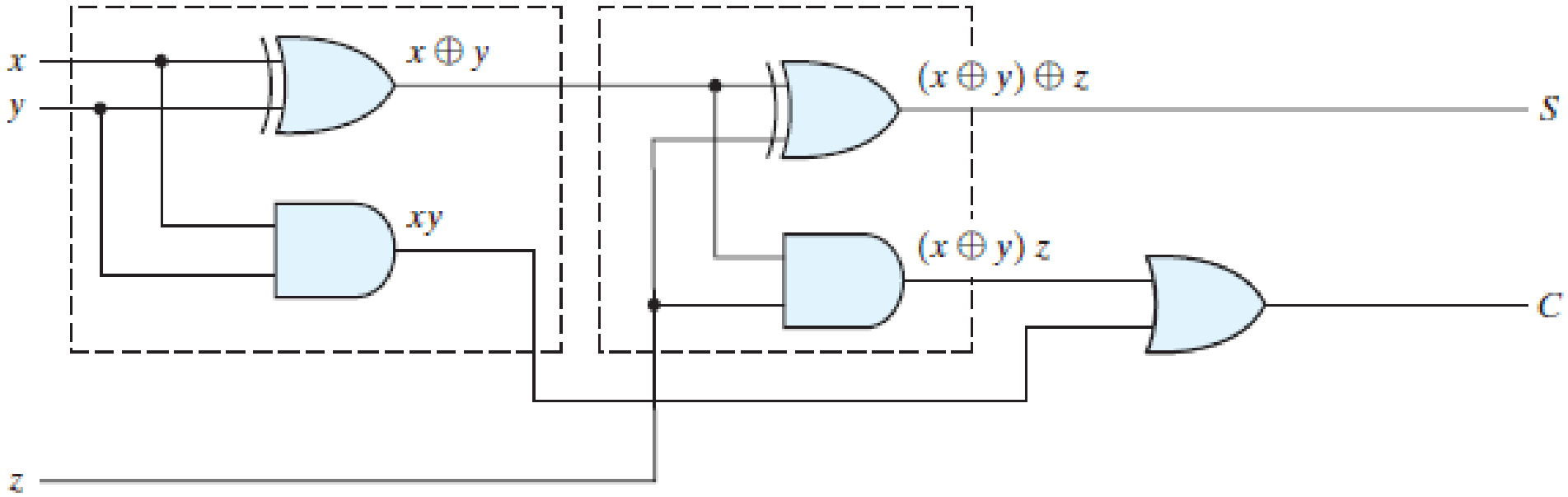
Combinational Logic Circuits: Half Adder and Full adder

- Full Adder Boolean Expression:

$$S = (x \oplus y) \oplus z$$

$$C = (x \oplus y).z + x.y$$

- Implementation of full adder with two half adders and an OR gate



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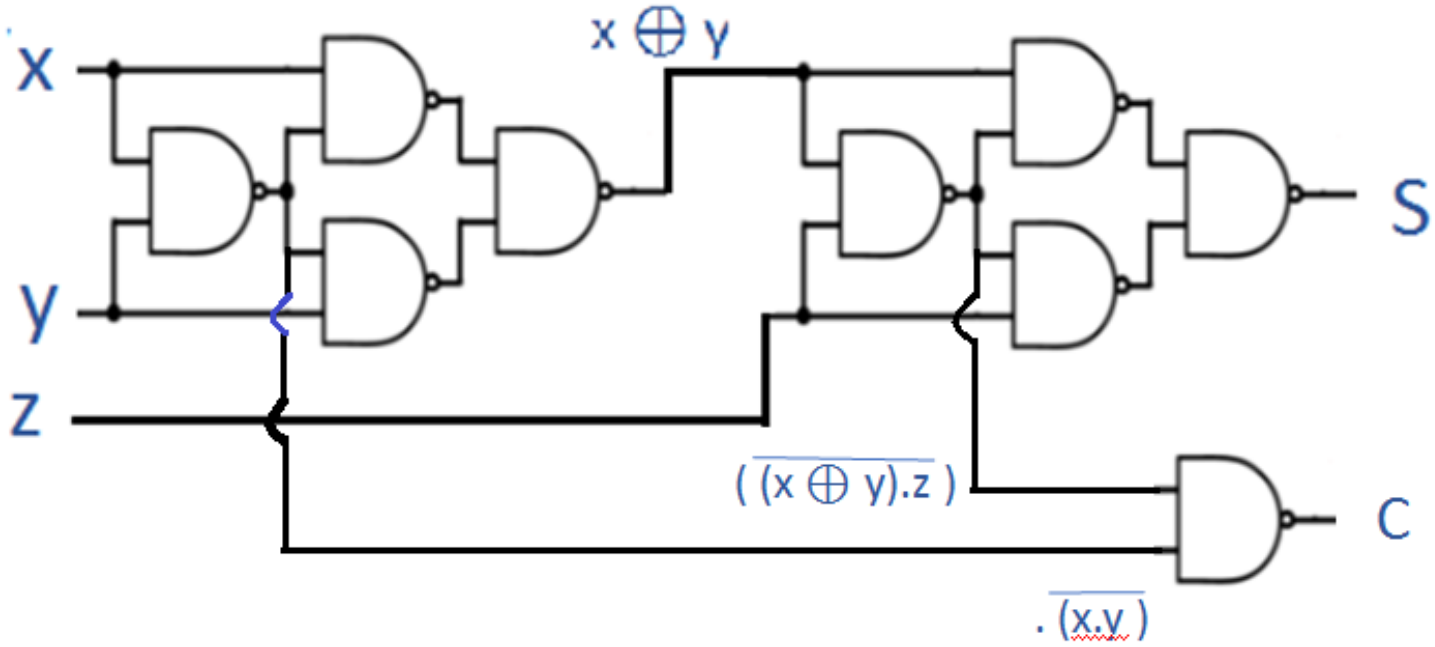
Combinational Logic Circuits: Half Adder and Full adder

- Boolean Expression: $S = (x \oplus y) \oplus z$

  $C = (x \oplus y).z + x.y$

- Full adder circuit using NAND Gates



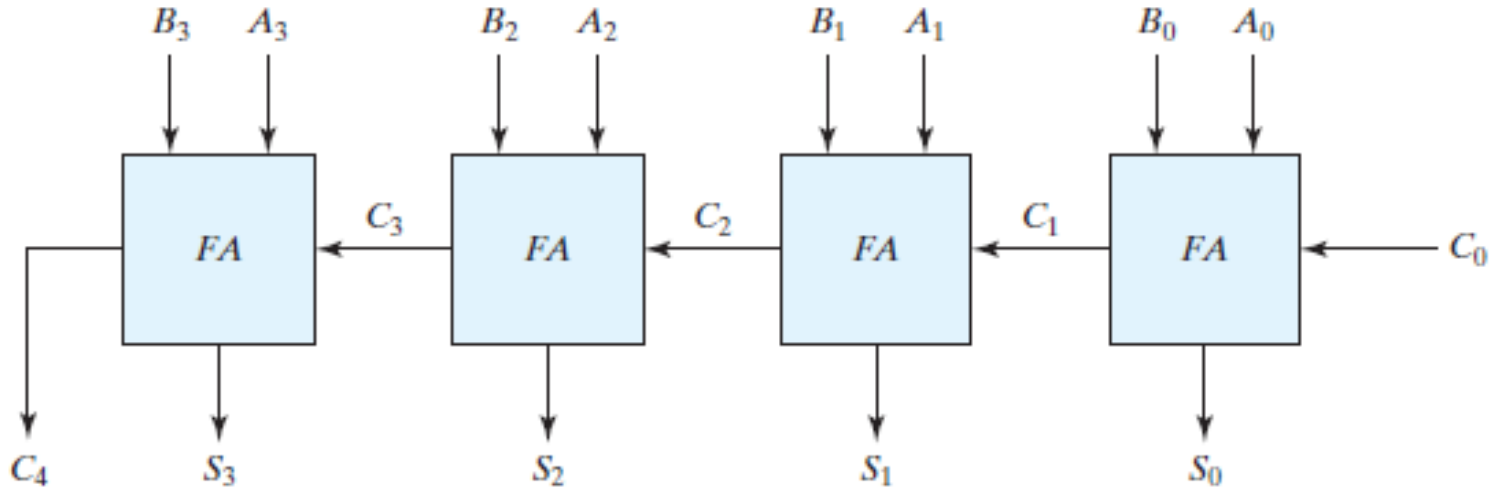
$C = \overline{((x \oplus y).z + x.y)}$

$C = \overline{\overline{(x \oplus y).z} \; . \; \overline{x.y}}$

Combinational Logic Circuits: Half Adder and Full adder

❖ Four-bit adder

Using four Full adder Ripple adder circuit is constructed.



❖ Example

```
      1110
A =   1101
+ B = 0111
      -----
      10100
```

Reference: "Digital Design with an Introduction to Verilog HDL" M Morris Mano, Michale D Ciletti

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Combinational Logic Circuits: Half Adder and Full adder

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Summary:

- Half Adder Circuits: (i) Using Basic Gates
  (ii) Using NAND Gates

- Full Adder Circuits: (i) Using Basic Gates
  (ii) Using NAND Gates

THANK YOU

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