



ELECTRONIC PRINCIPLES AND DEVICES

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Department of Electronics and Communication Engineering

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Digital Electronics

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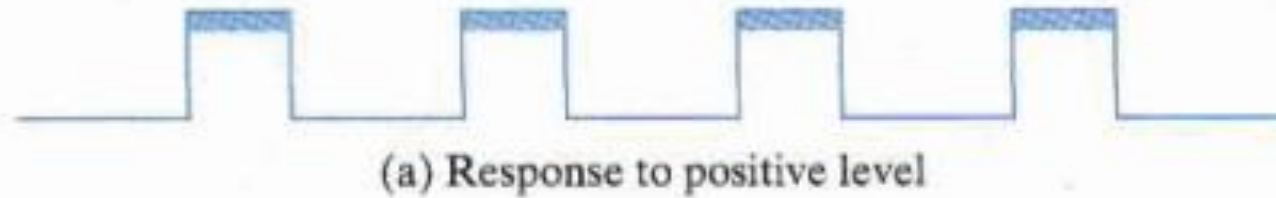
Recap

- D Flip-Flop: Working, Function Table
- JK Flip-Flop: Working, Function Table
- T Flip-Flop: Working, Function Table
- Conclusion Remarks

Electronic Principles and Devices

Recap:

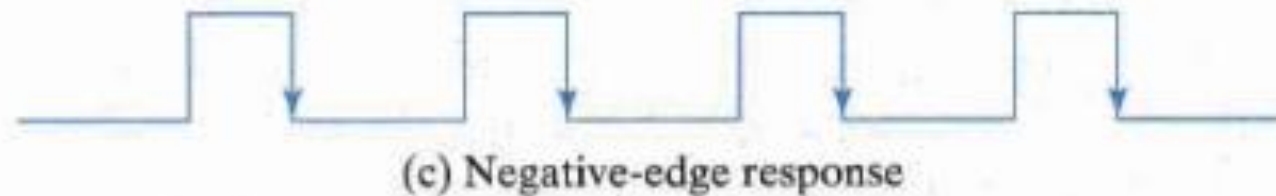
1. Flip – flops are the **building blocks** of sequential circuits.
But these are built from **latches**.
2. Flip- flops **continuously checks** its inputs and changes its outputs correspondingly only at time instant determined by the **clock signal**.
3. Flip – flops is **sensitive** to signal change. They transfer data only at single time instance and data can't be changed till next signal change.
➤ Therefore they are used as **registers**.
4. It is an edge triggered circuit, means that the output and the next state input changes, when there's a change in the clock pulse whether it can may be **POSITIVE (+ve)** or **NEGATIVE (-ve) clock pulse**.



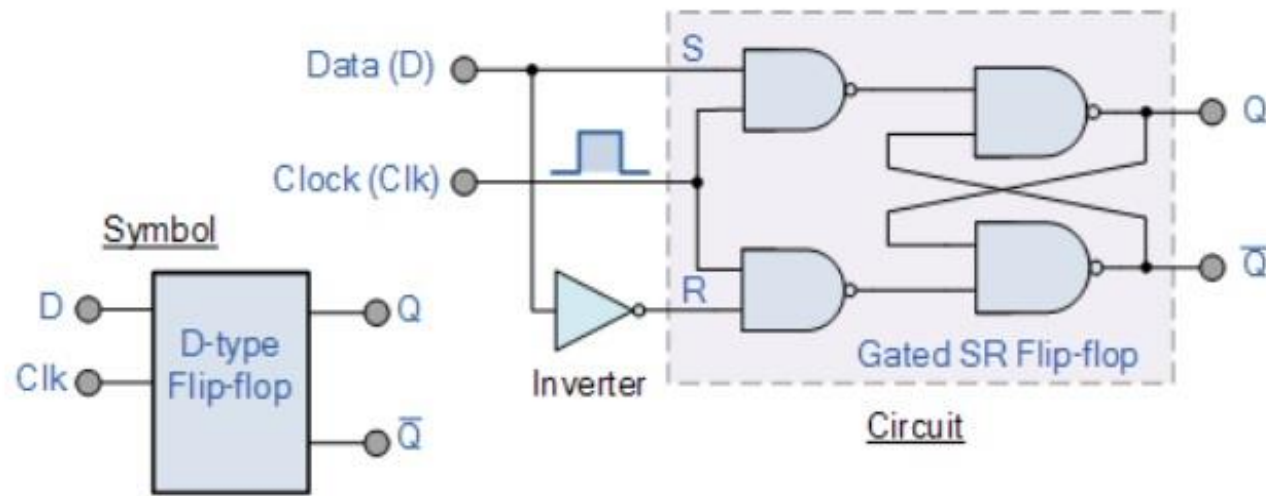
Flip-Flops will change the Output when the clock remains as logic 1 as shown in figure (a)



Flip-Flops will change the Output when the clock changes from logic 0 to Logic 1 as shown in figure (b)



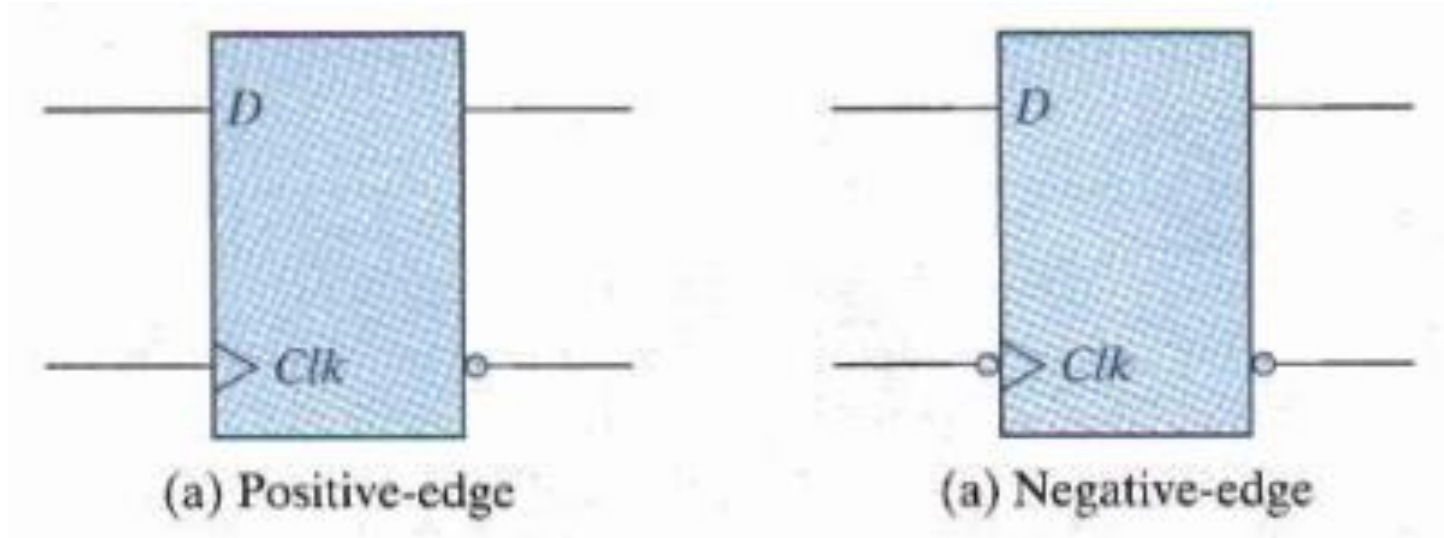
Flip-Flops will change the Output when the clock changes from logic 1 to Logic 0 as shown in figure (c)



- ❑ The **D Flip Flop** is by far the most important of the clocked flip-flops as it ensures that inputs **S** and **R** are **never equal** to one at the same time.
- ❑ The **D Flip Flop** are constructed from a SR flip-flop with an **inverter** added between the **S** and the **R** inputs to allow for a single D (Data) input.

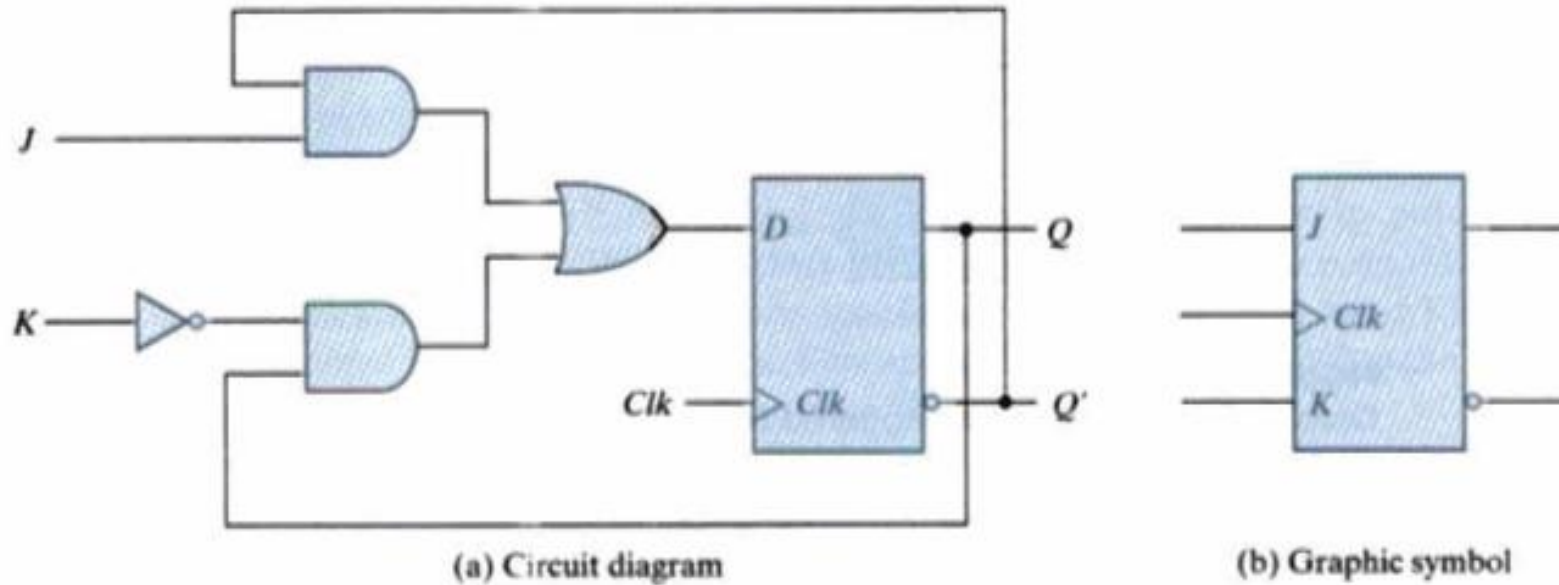
INPUTS		OUTPUTS		Status of D Flip-Flop
CLK	D	Q	Q'	
0	X	Q_1	Q'_{-1}	PREVIOUS STATE
1	0	0	1	RESET
1	1	1	0	SET

- ❑ The D Flip-flop will store and output whatever logic level is applied to its **DATA** input.
- ❑ Once the clock input goes LOW the “set” and “reset” inputs of the flip-flop are both held at logic level “1”, so it will not change its state.
- ❑ ↓ and ↑ indicates direction of clock pulse as it is assumed D-type flip flops are edge triggered.



In D Flip-Flops, **Absence of the bubble in front of the Clk indicates Positive edge triggered as shown in figure (a)**

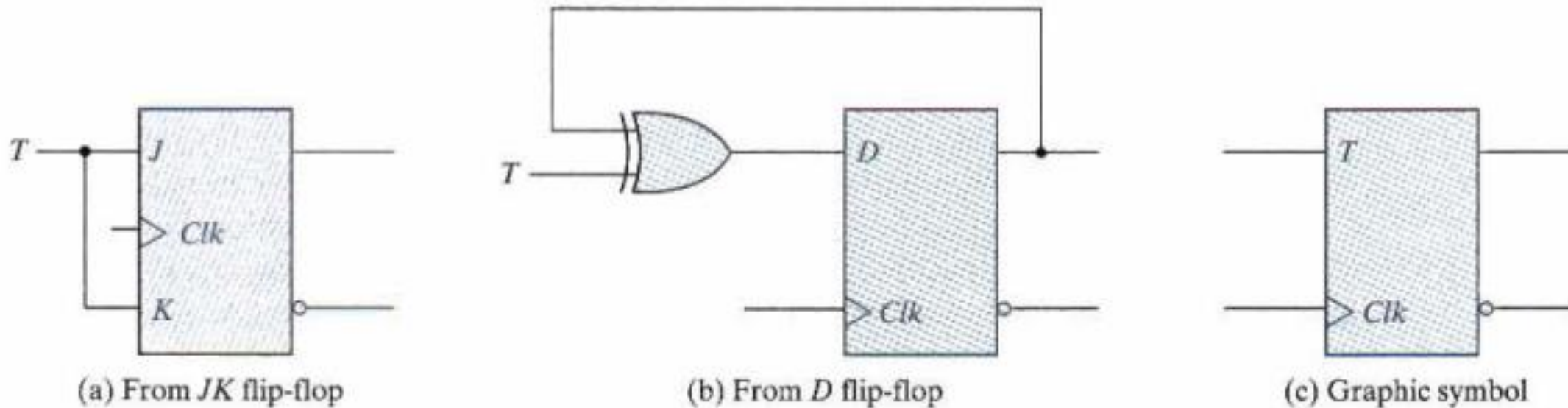
In D Flip-Flops, **Presence of the bubble in front of the Clk indicates Positive edge triggered as shown in figure (b)**



- ❑ The Inputs are **J-K** along with the Clk
 - J-K inputs comes after its inventors **Jack Kilby**.

Function Table

INPUTS			OUTPUTS		Status of JK Flip-Flop
CLK	J	K	Q	Q'	
0	X	X	Q_{-1}	Q'_{-1}	PREVIOUS STATE
1	0	0	Q_{-1}	Q'_{-1}	PREVIOUS STATE
1	0	1	0	1	RESET
1	1	0	1	0	SET
1	1	1	Q'_{-1}	Q_{-1}	TOGGLE



T Flip-Flop using JK Flip-Flop & D Flip-Flop

□ T Flip-Flop is a **synchronous** device, where high to low or low to high transitions is passed through **clock signal** which **changes** the output state of Flip-Flop.

INPUTS		OUTPUTS		Status of T Flip-Flop
CLK	T	Q	Q'	
0	X	Q_{-1}	Q'_{-1}	PREVIOUS STATE
1	0	Q_{-1}	Q'_{-1}	PREVIOUS STATE
1	1	Q'_{-1}	Q_{-1}	TOGGLE

Advantages of T flip-flop:

- These Flip-Flops has a **toggle input** and a **clock**.
When a clock is triggered it **inverts** the value of Flip-Flops.
- They are used for designing the **counters**.

- **JK flip-flop** is a sequential circuit, whose state transitions are **synchronized** with the **clock pulse** (+ve / -ve) edge triggered.
- In **JK flip-flop** all the rows are a valid state in the characteristic table, also when $J=K=1$, the output toggles, **Toggle state**.
- **D flip-flop** is a sequential circuit, whose output is same as the input and hence also called as **transparent flip-flop**.
- **T flip-flop** is a synchronous sequential circuit, whose state transitions are **synchronized** with the **clock pulse**.
- **T flip-flop** finds its application in counters, **Toggle state** is used.



THANK YOU

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