Countbcd

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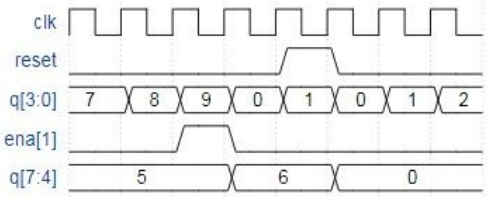
Build a 4-digit BCD (binary-coded decimal) counter. Each decimal digit is encoded using 4 bits: q[3:0] is the ones digit, q[7:4] is the tens digit, etc. For digits [3:1], also output an enable signal indicating when each of the upper three digits should be incremented.

You may want to instantiate or modify some one-digit decade counters.




```
module top_module (
    input clk,
    input reset,    // Synchronous active-high reset
    output [3:1] ena,
    output [15:0] q);

    always@(posedge clk) begin
        if(reset)begin
            q[3:0]<=4'd0;
        end
        else begin
            q[3:0]<=(q[3:0]==4'd9)?4'd0:(q[3:0]+4'd1);
        end
    end
    assign ena[1]=(q[3:0]==4'd9);

    always@(posedge clk) begin
        if(reset)begin
            q[7:4]<=4'd0;
        end
        else if(ena[1]) begin
            q[7:4]<=(q[7:4]==4'd9)?4'd0:(q[7:4]+4'd1);
        end
    end
    assign ena[2]=(q[3:0]==4'd9)&(q[7:4]==4'd9);

    always@(posedge clk) begin
        if(reset)begin
            q[11:8]<=4'd0;
        end
        else if(ena[2]) begin
            q[11:8]<=(q[11:8]==4'd9)?4'd0:(q[11:8]+4'd1);
        end
    end

    assign ena[3]=(q[3:0]==4'd9)&(q[7:4]==4'd9)&(q[11:8]==4'd9);
    always@(posedge clk) begin
```

```
        if(reset)begin
            q[15:12]<=4'd0;
        end
        else if(ena[3]) begin
            q[15:12]<=(q[15:12]==4'd9)?4'd0:(q[15:12]+4'd1);
        end
    end


endmodule
```