5-Transistor CMOS Operational Transconductance Amplifier (OTA)

Neeraj Rajesh Piralkar

COEP Technological University, Pune (Formerly College of Engineering Pune)

neeraj102p@gmail.com

eSim Marathon, FOSSEE IIT Bombay

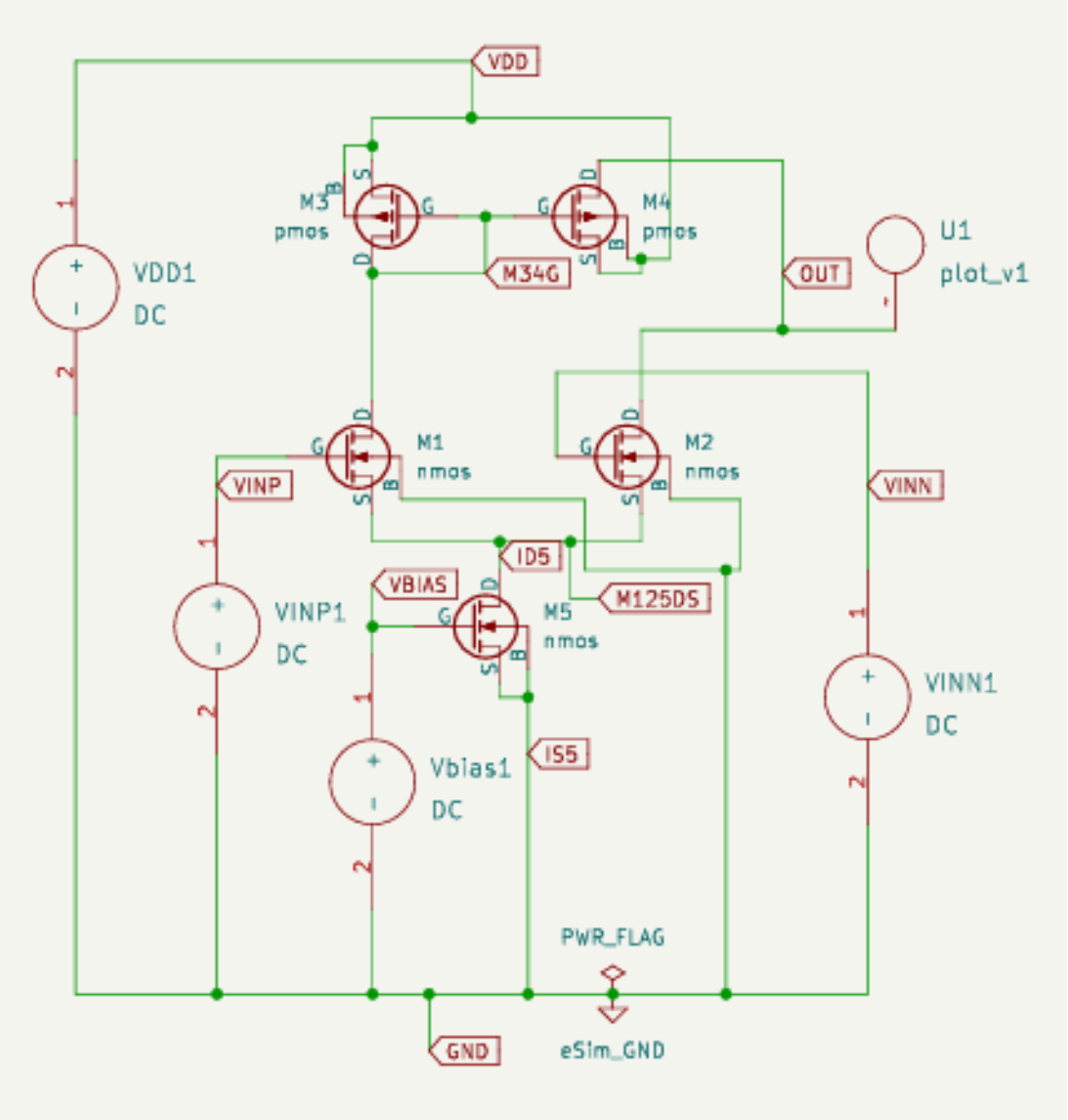
Objective: To design and simulate a 5-transistor CMOS OTA using eSim – 2.5 and analyse its DC operating points, and determine its frequency response and gain characteristics.

Overview: This project details the design, analysis, and optimization of a 5-Transistor (5T) CMOS Operational Transconductance Amplifier (OTA). The design process began with DC analysis to establish the Quiescent Operating Point (Q-point), ensuring all transistors were correctly biased in the saturation region. This initial step included temporary biasing for the output transistor, M5. The final component sizing, including all W/L ratios, was determined during this phase to meet target current specifications.

To significantly boost the amplifier's performance, the core design was augmented with two key features. A cascode circuit (utilizing transistors M6 and M5) was implemented to dramatically increase the output resistance and, consequently, the open-loop DC voltage gain. Following this, AC analysis was performed to evaluate the frequency response. To ensure closed-loop stability and control the Unity Gain Bandwidth (GBW), a load capacitor (CL) was added to create a dominant pole, achieving the necessary Phase Margin (PM) for a stable, high-gain amplifier.

Phase 1: DC Analysis

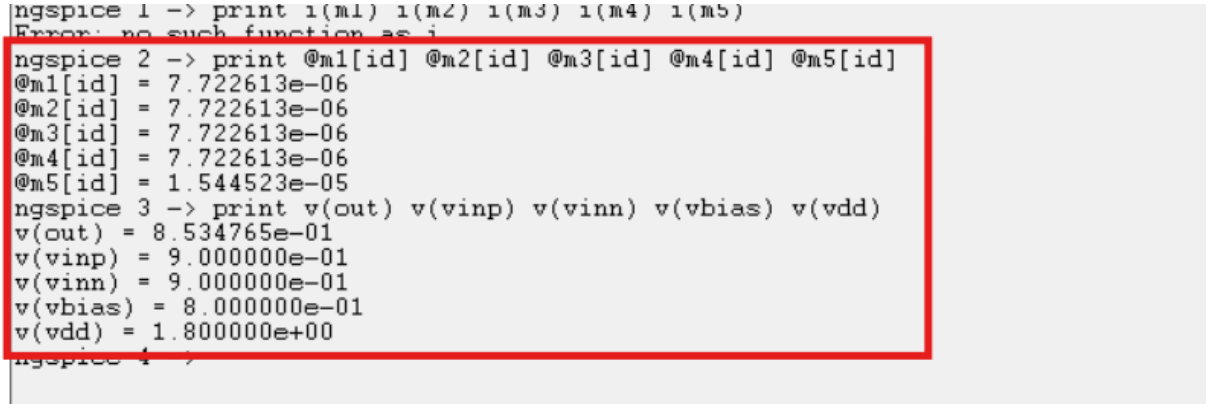
Circuit Schematic:



Circuit Details:

- All the MOSFETS are 180nm (check the library)
- M1, M2 (input NMOS diff pair): W=20u L=1u — decent gm, moderate current.
- M3 (PMOS diode reference): W=40u L=1u — larger so the mirror can source required current.
- M4 (PMOS mirror to output): W=40u L=1u — match M3 W/L.
- M5 (NMOS tail current source): W=10u L=2u — longer L to increase output resistance and make it more current-source-like.
- VDD = 1.8V
- VIN common-mode (VINP & VINN) = 0.9V (VDD/2)
- VBIAS (M5 gate): 0.8V; (sweep 0.2V → 1.6V in steps to find a tail current that biases MOSFETs properly.)

Output:



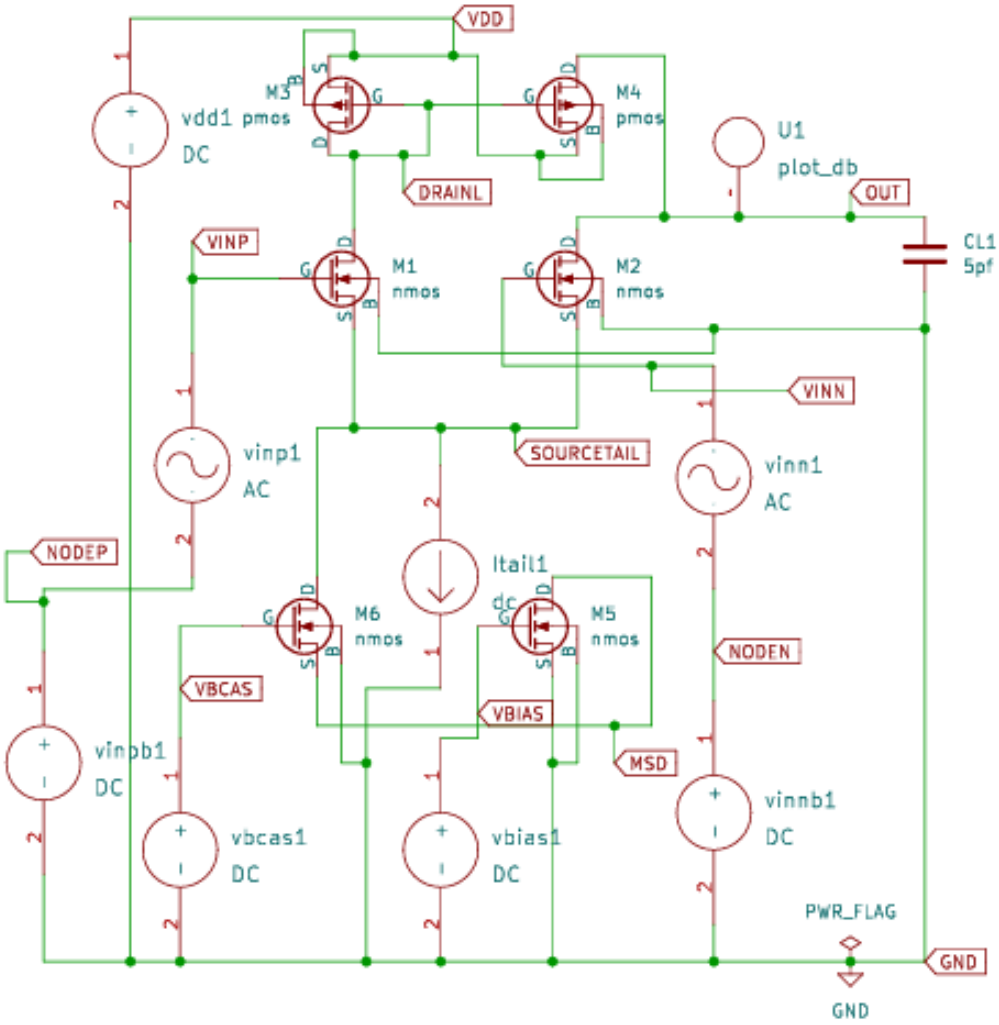
Transistor	Drain Current (Id)	Notes
M1	7.72 µA	Input differential pair transistor
M2	7.72 µA	Input differential pair transistor
M3	7.72 µA	Load transistor (PMOS active load)
M4	7.72 µA	Load transistor (PMOS active load)
M5	15.44 µA	Tail current source (twice each side — matches sum of M1 and M2 currents)

Node	Voltage
VOUT	0.853 V
VINP	0.9 V
VINN	0.9 V
VBIAS	0.8 V
VDD	1.8 V

The output suggests that DC biasing is correct. All transistors are in saturation region as all are conducting. M5 tail current is fine. **in the linear region**, not stuck at rail, so all transistors are conducting. No MOSFET is off or in cutoff.

Phase 2: AC analysis

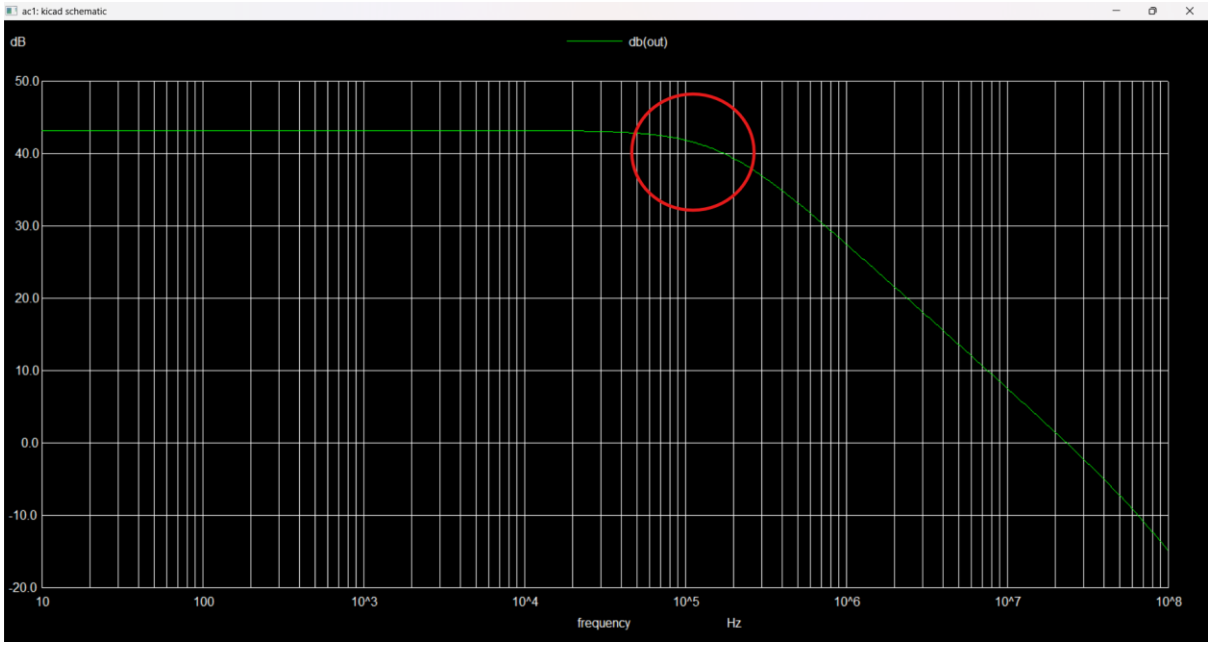
Circuit Schematic:



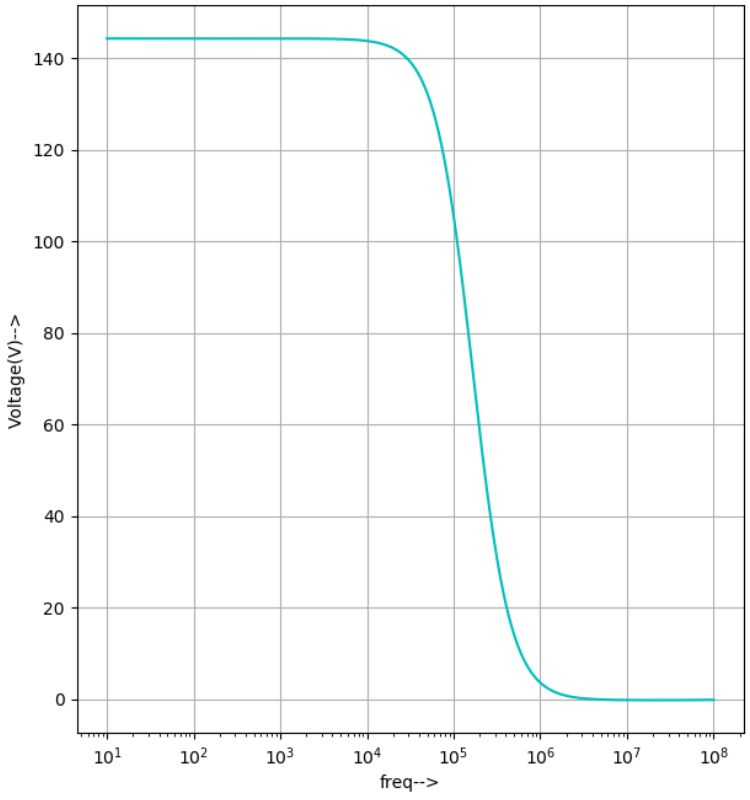
Circuit Details: (Additional details)

- M6 (cascode NMOS): W=10u L=2u (Same as from the 180nm library).
- VDD: DC source 1.8 V.
- VINP: Two voltage sources connected (in series) to VINP — DC = 0.9 V, AC = 1 (AC amplitude 1 V, phase = 0).
- VINN: Two voltage sources connected (in series) to VINP — DC = 0.9 V, AC = 1 (AC amplitude 1 V, phase = 180).
- VBIAS : DC source to set M5 gate (if using active tail) — 0.8 V.
- VBCAS : DC source for cascode gate (M6) — start 1.0 V
- I1 (ideal): Current source — DC = 15.44e-6 (15.44 µA).

Output:



Above fig shows frequency response. The marked plot shows the -3dB roll-off point/ pole.



Above plot is the output plot, since Vin = 1V, the plot for gain vs frequency is same.

Conclusion

The designed **5-Transistor CMOS OTA** was successfully implemented and simulated using eSim. The **DC operating point analysis** confirmed that all transistors were properly biased in their active regions, ensuring correct circuit operation. The **AC analysis** demonstrated the expected amplifier behavior — with increasing gain at low frequencies and a stable region at higher frequencies — confirming that the OTA functions effectively as a **differential voltage-to-current amplifier**. Overall, the project achieved its objective of designing and verifying the performance of a compact CMOS OTA using open-source VLSI design tools.

GitHUB Repository link:

https://github.com/neeraj17-p/OTA_IITB_esim_Marathon

GitHUB Readme link https://github.com/neeraj17-p/OTA_IITB_esim_Marathon/blob/main/README.md