for all notes click below

github

Introduction to Digital Systems

Unit III Question Bank

1. What are the classifications of sequential circuits?

Sequential circuits:
Now, these are types and classifications of Sequential circuits.
Types of Sequential circuits:
The sequential circuits can be event driven, clock driven and pulse driven. There are two main types of sequential circuits: (a) Synchronous and (b) Asynchronous.

- **(a).** Asynchronous Sequential circuits **–**
  Asynchronous circuits do not synchronize with positive edge or negative edge of the clock signal, that means, the outputs of asynchronous sequential circuits do not change or affect at the same time and change their state immediately when there is a change in the input signal. So, these circuits are faster and independent of the internal clock pulses. But these circuits have uncertainty in the outputs and are difficult to design.

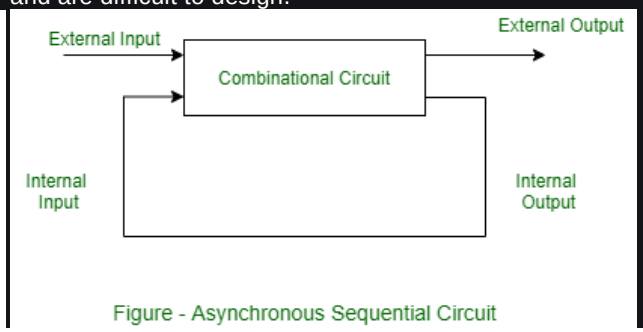

Figure - Asynchronous Sequential Circuit

- **(b).** Synchronous Sequential circuits **–**
  Synchronous circuits synchronize with either positive edge or negative edge of the clock signal, that means, the outputs of synchronous sequential circuits change or affect at the same time. These circuits use clock signal and level input (or pulsed with restrictions on pulse width and circuit propagation). Since they wait for the next clock pulse to arrive to perform the next operation, so these circuits are a bit slower compared to asynchronous. Level output changes state at the start of an input pulse and remains in that until the next input or clock pulse. The synchronous sequential circuit can be locked or unlocked (or pulsed).

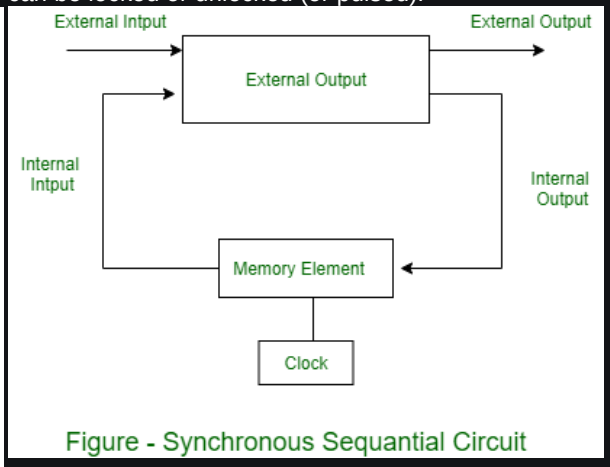

Figure - Synchronous Sequantial Circuit

Counters, Flip-Flops, and design of Mealy-Moore machines are examples of Synchronous sequential circuits.

2. What is the operation of D flip-flop?

What is D Flip Flop?

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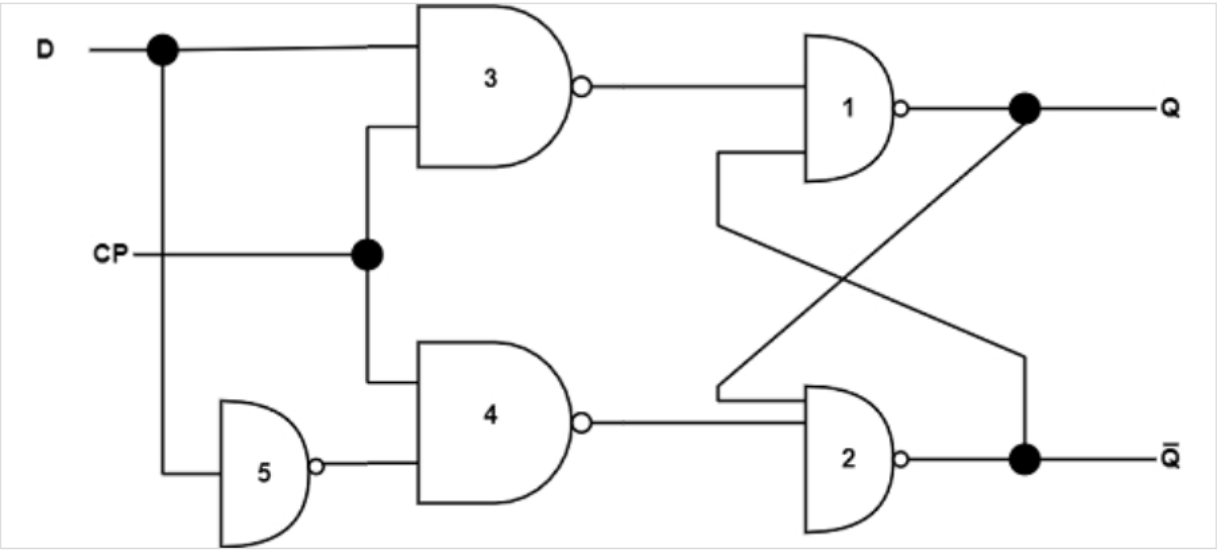
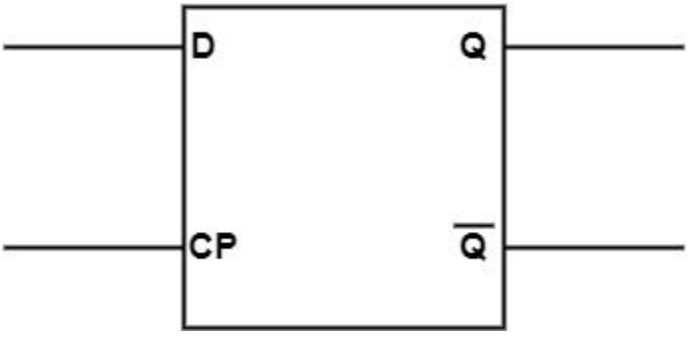
The D flip-flop is a clocked flip-flop with a single digital input 'D'. Each time a D flip-flop is clocked, its output follows the state of 'D'. The D Flip Flop has only two inputs D and CP. The D inputs go precisely to the S input and its complement is used to the R input.

Considering the pulse input is at 0, the outputs of gates 3 and 4 are at the 1 level and the circuit cannot convert state regardless of the value of D. The D input is sampled when CP = 1. If D is 1, the Q output goes to 1, locating the circuit in the set state. If D is 0, output Q goes to 0, and the circuit switches to a clear state.



The truth table for D flip-flop is as shown in the table.

S	D	Q_{N+1}
0	0	0
0	1	1
1	0	0
1	1	1



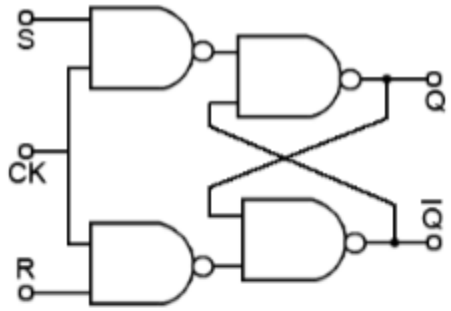
3. What is flip-flop

Flip-flop is a circuit that maintains a state until directed by input to change the state. A basic flip-flop can be constructed using four-NAND or four-NOR gates. **Types of flip-flops:**

1. RS Flip Flop
2. JK Flip Flop
3. D Flip Flop
4. T Flip Flop

Logic diagrams and truth tables of the different types of flip-flops are as follows:

S-R Flip Flop :

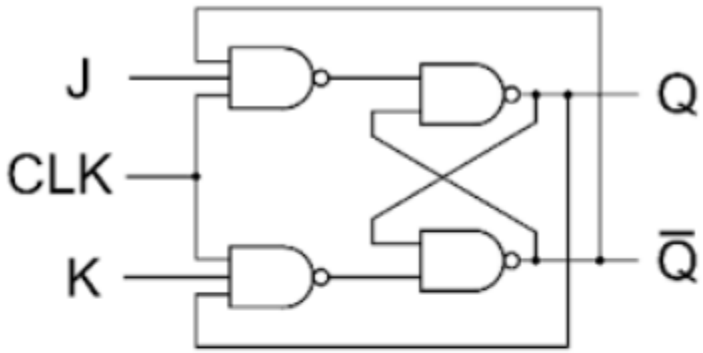


TRUTH TABLE

S	R	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	-
1	1	1	-

Characteristics Equation for SR Flip Flop: $Q_{N+1} = Q_N R' + SR'$

J-K Flip Flop:

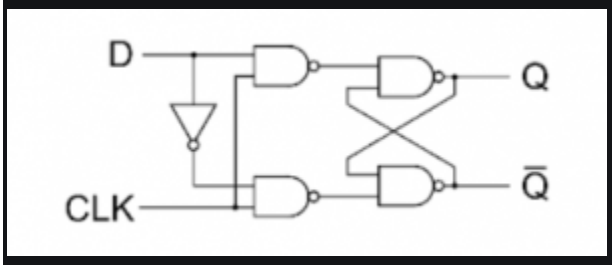


TRUTH TABLE

J	K	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Characteristics Equation for JK Flip Flop: $Q_{N+1} = JQ'_N + K'Q_N$

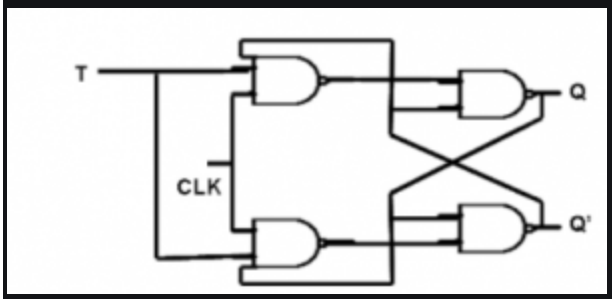
D Flip Flop:



Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

Characteristics Equation for D Flip Flop: $Q_{N+1} = D$

T Flip Flop:



T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

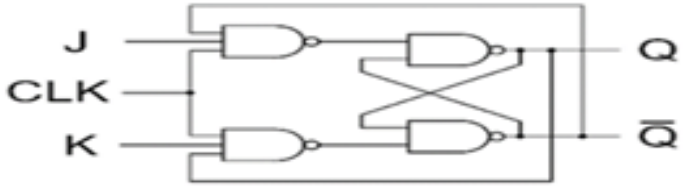
Characteristics Equation for T Flip Flop: $Q_{N+1} = Q'_N T + Q_N T' = Q_N$ XOR T

5. Define Race Around Condition

Race around condition occurs in JK Flip Flop when both its inputs J=K=1 and also the clock =1 for a long period.

J-K Flip Flop

The truth table is shown below with its circuit diagram.



TRUTH TABLE

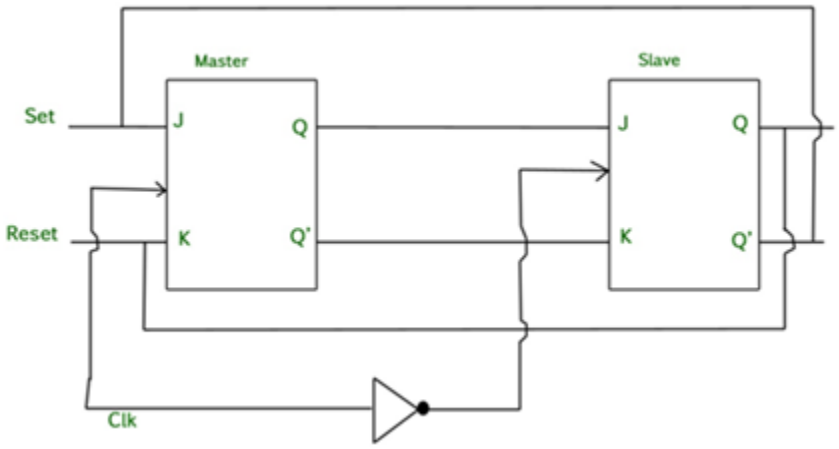
J	K	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Race Around Condition in JK Flip-flop

- For J-K flip-flop, if J=K=1, and if clk=1 for a long period of time, then output Q will toggle as long as CLK remains high which makes the output unstable or uncertain.
- This is called a race around condition in J-K flip-flop.
- We can overcome this problem by making the clock =1 for very less duration.
- The circuit used to overcome race around conditions is called the Master **Slave JK** flip flop.

Master Slave JK flip flop

- Here two JK flip flops are connected in series.
- The first JK flip flop is called the **"master"** and the other is a **"slave"**.
- The output from the master is connected to the two inputs of the slave whose output is fed back to inputs of the master.
- The circuit also has an inverter other than the two flip flops.
- The Clock Pulse and inverter are connected because of which the flip flops get an inverted clock pulse.
- In other words, if CP=0 for a master flip-flop, then CP=1 for a slave flip-flop and vice versa.

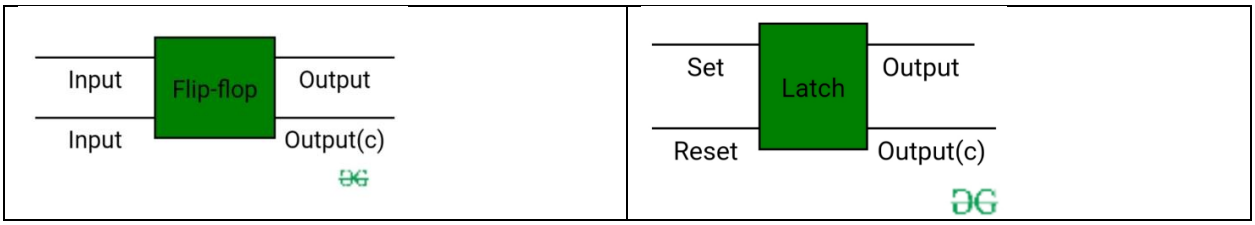


Working of a Master Slave flip flop

- When the clock pulse goes high, the slave is isolated; J and K inputs can affect the state of the system. The slave flip-flop is isolated when the CP goes low.
- When the CP goes back to 0, information is transmitted from the master flip-flop to the slave flip-flop and output is obtained.
- As the master flip flop is positive triggered it responds first and the slave later (it is negative edge triggered).
- The master goes to the K input of the slave when both inputs J=0 and K=1, and also Q' = 1. In this case the slave copies the master as the clock forces the slave to reset.
- The master goes to the J input of the slave when both J=1 and K=0, Q = 1. The clock is set due to the negative transition of the clock.
- There is a state of toggle when both J=1 and K=1. On the negative transition of clock slave toggles and the master toggles on the positive transition of the clock.
- Both the flip flops are disabled when both J=0 and K=0 and Q is unchanged.

6. Difference between latch and flip-flop

	Flip-flop	Latch
1	Flip-flop is a bistable device i.e., it has two stable states that are represented as 0 and 1.	Latch is also a bistable device whose states are also represented as 0 and 1.
2	It checks the inputs but changes the output only at times defined by the clock signal or any other control signal.	It checks the inputs continuously and responds to the changes in inputs immediately.
3	It is a edge triggered device.	It is a level triggered device.
4	Gates like NOR, NOT, AND, NAND are building blocks of flip flops.	These are also made up of gates.
5	They are classified into asynchronous or synchronous flipflops.	There is no such classification in latches.
6	It forms the building blocks of many sequential circuits like counters.	These can be used for the designing of sequential circuits but are not generally preferred.
7	a, Flip-flop always have a clock signal	latche doesn't have a clock signal
8	Flip-flop can be build from Latches	Latches can be build from gates
9	ex:D Flip-flop, JK Flip-flop	ex:SR Latch, D Latch



6. Define Propagation Delay

The time required to change the output from one logic state to another logic state after input is applied, is called the propagation delay of logic circuit. Its unit is nanoseconds. It is denoted by t_p.

7. What is Master Slave Flip-flop

refer to ans 5

8. Explain Shift Registers

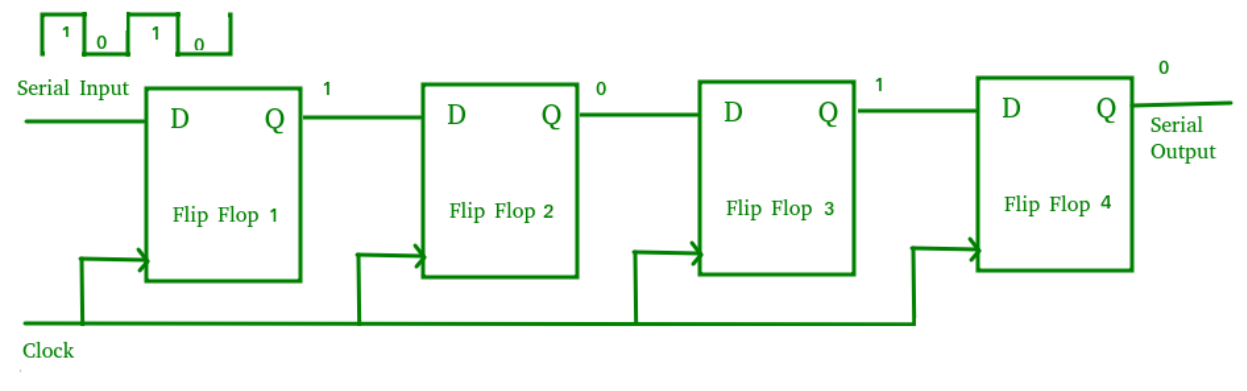
Flip flops can be used to store a single bit of binary data (1or 0). However, in order to store multiple bits of data, we need multiple flip flops. N flip flops are to be connected in an order to store n bits of data. A **Register** is a device which is used to store such information. It is a group of flip flops connected in series used to store multiple bits of data.
The information stored within these registers can be transferred with the help of **shift registers**. Shift Register is a group of flip flops used to store multiple bits of data. The bits stored in such registers can be made to move within the registers and in/out of the registers by applying clock pulses. An n-bit shift register can be formed by connecting n flip-flops where each flip flop stores a single bit of data.
The registers which will shift the bits to left are called “Shift left registers”.
The registers which will shift the bits to right are called “Shift right registers”.
Shift registers are basically of 4 types. These are:

a-Serial In Serial Out shift register
b-Serial In parallel Out shift register
c-Parallel In Serial Out shift register
d-Parallel In parallel Out shift register

Serial-In Serial-Out Shift Register (SISO) –

The shift register, which allows serial input (one bit after the other through a single data line) and produces a serial output is known as Serial-In Serial-Out shift register. Since there is only one output, the data leaves the shift register one bit at a time in a serial pattern, thus the name Serial-In Serial-Out Shift Register.

The logic circuit given below shows a serial-in serial-out shift register. The circuit consists of four D flip-flops which are connected in a serial manner. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip flop.

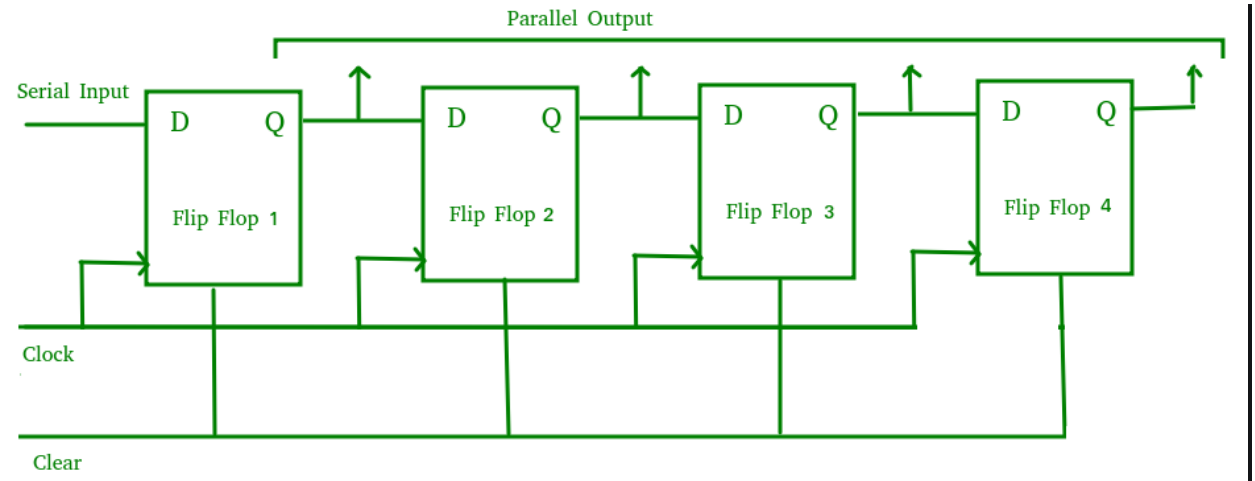


The above circuit is an example of shift right register, taking the serial data input from the left side of the flip flop. The main use of a SISO is to act as a delay element.

Serial-In Parallel-Out shift Register (SIPO) –

The shift register, which allows serial input (one bit after the other through a single data line) and produces a parallel output is known as Serial-In Parallel-Out shift register.

The logic circuit given below shows a serial-in-parallel-out shift register. The circuit consists of four D flip-flops which are connected. The clear (CLR) signal is connected in addition to the clock signal to all the 4 flip flops in order to RESET them. The output of the first flip flop is connected to the input of the next flip flop and so on. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip flop.

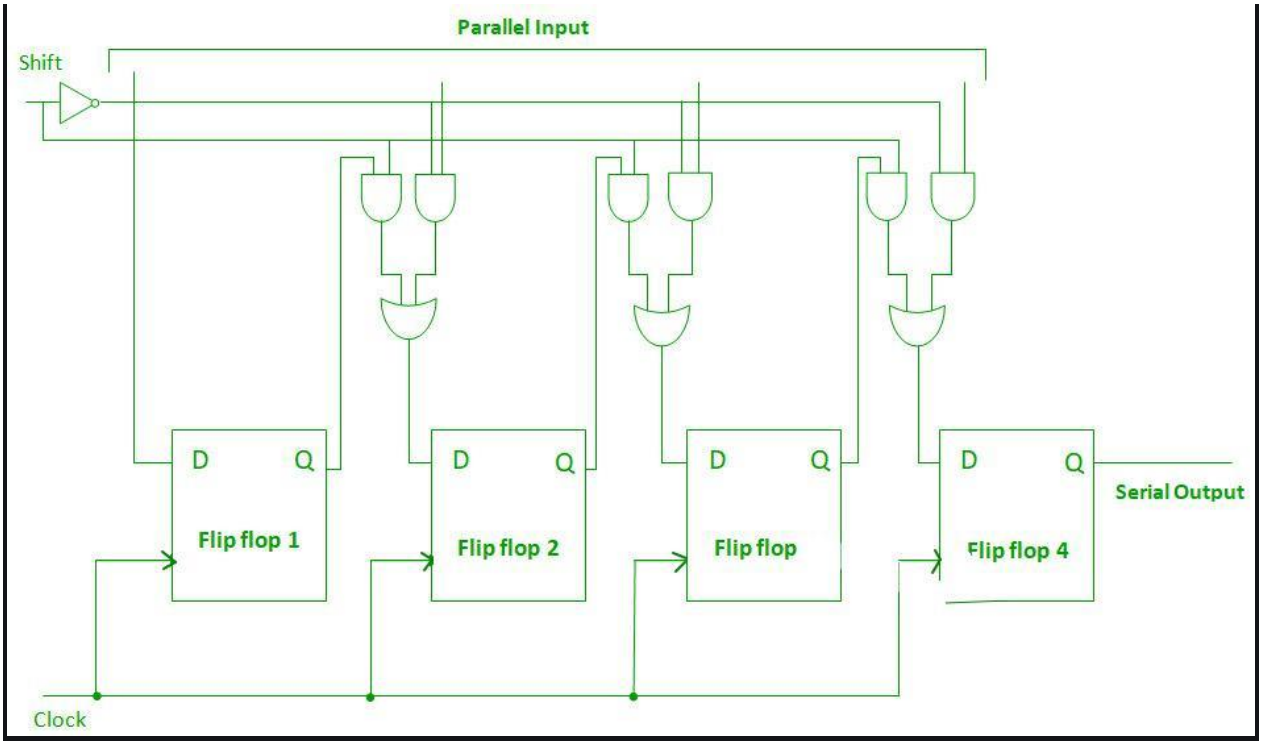


The above circuit is an example of shift right register, taking the serial data input from the left side of the flip flop and producing a parallel output. They are used in communication lines where demultiplexing of a data line into several parallel lines is required because the main use of the SIPO register is to convert serial data into parallel data.

Parallel-In Serial-Out Shift Register (PISO) –

The shift register, which allows parallel input (data is given separately to each flip flop and in a simultaneous manner) and produces a serial output is known as Parallel-In Serial-Out shift register.

The logic circuit given below shows a parallel-in-serial-out shift register. The circuit consists of four D flip-flops which are connected. The clock input is directly connected to all the flip flops but the input data is connected individually to each flip flop through a multiplexer at the input of every flip flop. The output of the previous flip flop and parallel data input are connected to the input of the MUX and the output of MUX is connected to the next flip flop. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip flop.

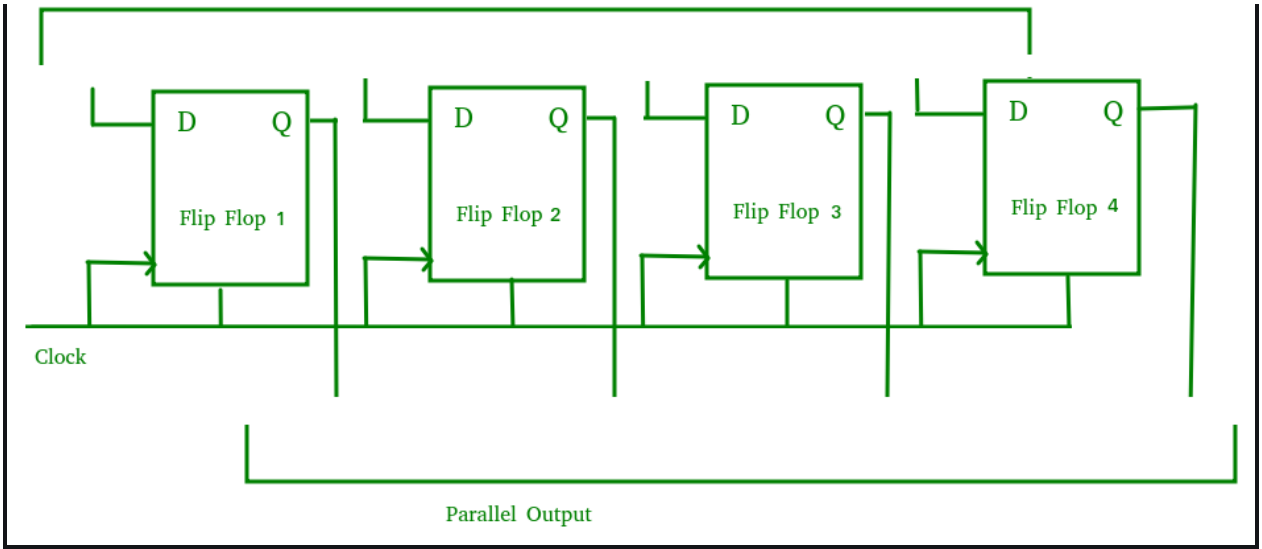


A Parallel in Serial out (PISO) shift register us used to convert parallel data to serial data.

Parallel-In Parallel-Out Shift Register (PIPO) –

The shift register, which allows parallel input (data is given separately to each flip flop and in a simultaneous manner) and also produces a parallel output is known as Parallel-In parallel-Out shift register.

The logic circuit given below shows a parallel-in-parallel-out shift register. The circuit consists of four D flip-flops which are connected. The clear (CLR) signal and clock signals are connected to all the 4 flip flops. In this type of register, there are no interconnections between the individual flip-flops since no serial shifting of the data is required. Data is given as input separately for each flip flop and in the same way, output also collected individually from each flip flop.



A Parallel in Parallel out (PIPO) shift register is used as a temporary storage device and like SISO Shift register it acts as a delay element.

9. What are the applications of Flip-flops

Applications of Flip-Flops:

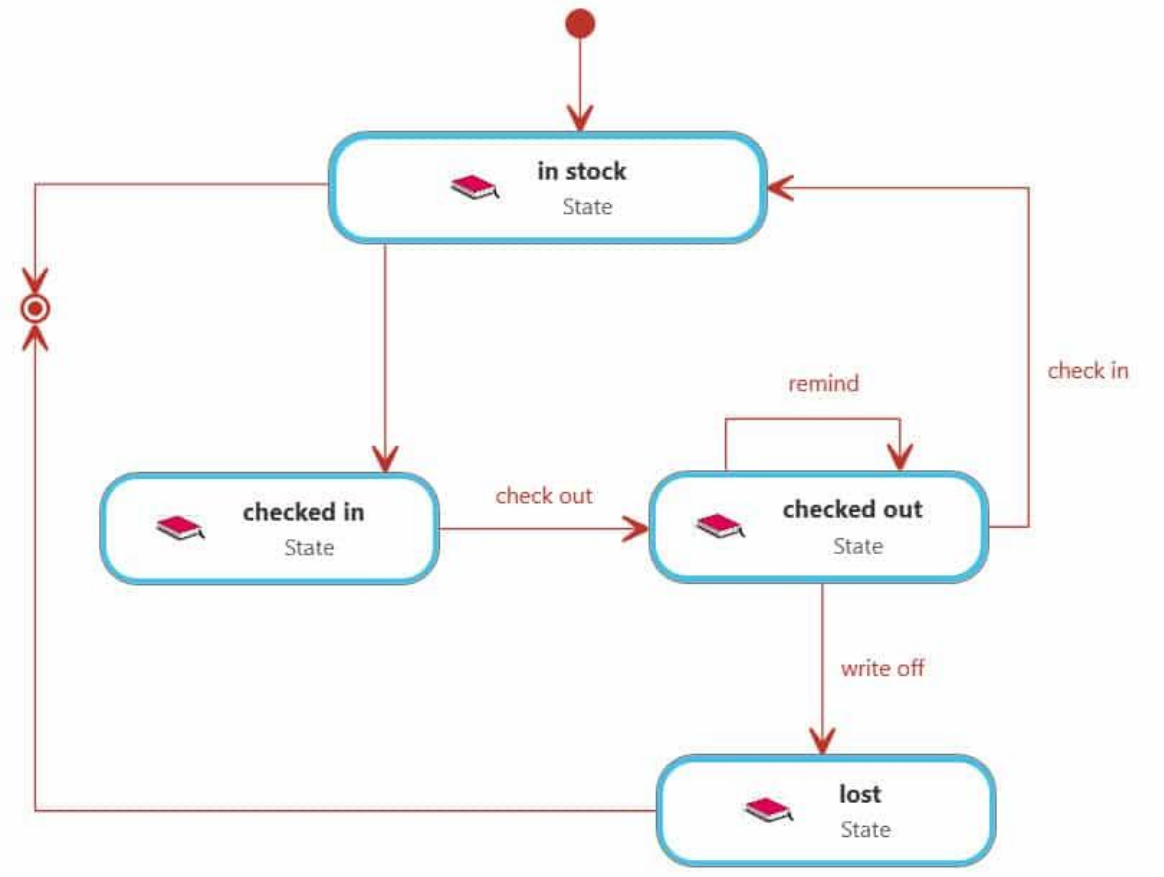
These are the various types of flip-flops being used in digital electronic circuits and the applications of Flip-flops are as specified below.

- Counters
- Frequency Dividers
- Shift Registers
- Storage Registers
- Bounce elimination switch
- Data storage
- Data transfer
- Latch
- Registers
- Memory

10.What is state diagram

A state diagram is the graphical representation of a state machine and one of the 14 UML diagram types for software and systems. State diagrams show a behavioural model consisting of states, state transitions and actions. UML state diagrams are based on the concept of state diagrams by David Harel. State diagrams depict the permitted states and transitions as well as the events that effect these transitions.

State diagrams are commonly used in the area of embedded systems. State diagrams help to visualize the entire life cycle of objects and thus help to provide a better understanding of state-based systems. An example of such a state-based system is a cash machine: Upon activation either the state *ready* or the state *malfunction* could be reached. As soon as the debit card is inserted it is verified. Depending on the result of the verification the pin number is requested or the process is aborted. Other possible states are account query or availablility check etc.



11.Write the truth table of clocked T- Flip Flop?

	Previous		Next	
T	Q	Q'	Q	Q'
0	0	1	0	1
0	1	0	1	0
1	0	1	1	0
1	1	0	0	1

12.How many types of Registers are there?

In Computer Organisation, the register is utilized to acknowledge, store, move information and directions that are being utilized quickly by the CPU. There are different kinds of registers utilized for different reasons. Some of the commonly used registers are:

- AC (accumulator)
- DR (Data registers)
- AR (Address registers)
- PC (Program counter)
- MDR (Memory data registers)
- IR (index registers)
- MBR (Memory buffer registers)

13.Define different types of latches.

There are various types of latches used in digital circuits which are as follows:

- **SR Latch**
- **Gated S-R Latch**
- **D latch**
- **Gated D Latch**
- **JK Latch**
- **T Latch**

for more details click here

14.Write the differences between synchronous and asynchronous counters?

	Synchronous Counter	Asynchronous Counter
1.	In synchronous counter, all flip flops are triggered with same clock simultaneously.	In asynchronous counter, different flip flops are triggered with different clock, not simultaneously.
2.	Synchronous Counter is faster than asynchronous counter in operation.	Asynchronous Counter is slower than synchronous counter in operation.
3.	Synchronous Counter does not produce any decoding errors.	Asynchronous Counter produces decoding error.
4.	Synchronous Counter is also called Parallel Counter.	Asynchronous Counter is also called Serial Counter.
5.	Synchronous Counter designing as well implementation are complex due to increasing the number of states.	Asynchronous Counter designing as well as implementation is very easy.
6.	Synchronous Counter will operate in any desired count sequence.	Asynchronous Counter will operate only in fixed count sequence (UP/DOWN).
7.	Synchronous Counter examples are: Ring counter, Johnson counter.	Asynchronous Counter examples are: Ripple UP counter, Ripple DOWN counter.
8.	In synchronous counter, propagation delay is less.	In asynchronous counter, there is high propagation delay.

15.Define Flip-flop and various types of flip flops?

refer-answer -3

16.Explain the Logic diagram of JK flip-flop?

refer-answer -3

17.Write difference between Combinational & Sequential circuits?

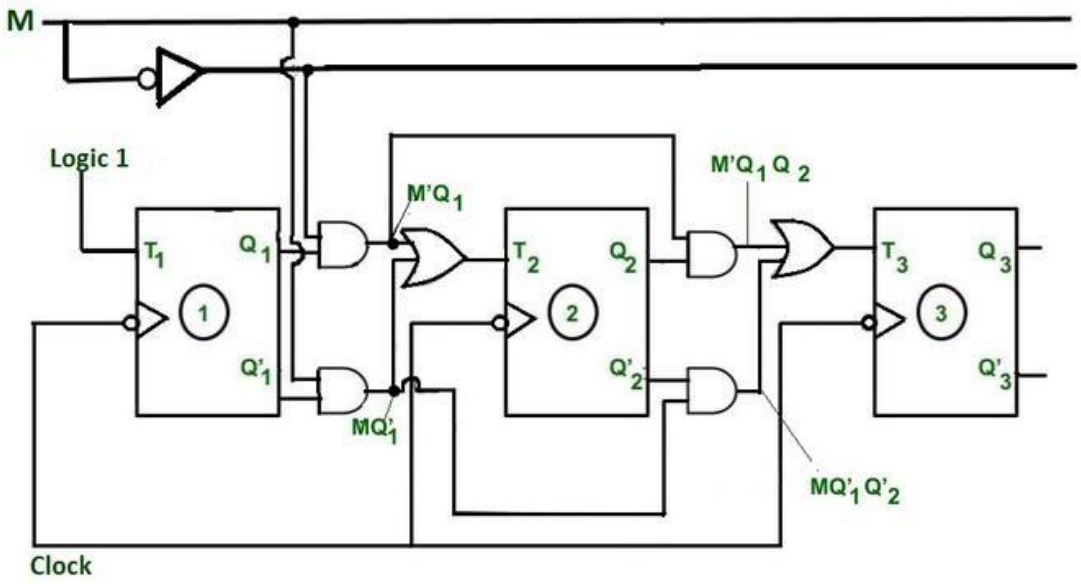
Combinational	Sequential
• In this output depends only upon present input. • Speed is fast. • It is designed easy. • There is no feedback between input and output. • This is time independent. • Elementary building blocks: Logic gates • Used for arithmetic as well as boolean operations. • Combinational circuits don't have capability to store any state. • As combinational circuits don't have clock, they don't require triggering. • These circuits do not have any memory element. • It is easy to use and handle.	• In this output depends upon present as well as past input. • Speed is slow. • It is designed tough as compared to combinational circuits. • There exists a feedback path between input and output. • This is time dependent. • Elementary building blocks: Flip-flops • Mainly used for storing data. • Sequential circuits have • capability to store any state or to retain earlier state. • As sequential circuits are clock dependent they need triggering. • These circuits have memory element. • It is not easy to use and handle.
Encoder, Decoder, Multiplexer, Demultiplexer	Flip-flops, Counters

18.Explain the Logic diagram of SR flip-flop?

refer-ans-3

19.Design and draw the 3 bit up-down synchronous counter?

click here for answer



20.Draw and explain the operation of D Flip-Flop?

refer to ans-3

21.Explain the working of Shift Registers?

refer to ans-8

22.Draw and explain the operation of SR LATCH?

SR (Set-Reset) Latch – They are also known as preset and clear states. The SR latch forms the basic building blocks of all other types of flip-flops.
SR Latch is a circuit with:
(i) 2 cross-coupled NOR gate or 2 cross-coupled NAND gate.
(ii) 2 input S for SET and R for RESET.
(iii) 2 output Q, Q'.

click-here-for-answer

23.Explain about Ring counter?

A ring counter is a typical application of the Shift register. The ring counter is almost the same as the shift counter. The only change is that the output of the last flip-flop is connected to the input of the first flip-flop in the case of the ring counter but in the case of the shift resister it is taken as output. Except for this, all the other things are the same.

No. of states in Ring counter = No. of flip-flop used

for-more-click-here

24.Explain about ripple counter?

Ripple counter is a cascaded arrangement of flip-flops where the output of one flip-flop drives the clock input of the following flip-flop. The number of flip flops in the cascaded arrangement depends upon the number of different logic states that it goes through before it repeats the sequence a parameter known as the modulus of the counter. A n-bit ripple counter can count up to 2^n states. It is also known as MOD n counter. It is known as ripple counter because of the way the clock pulse ripples its way through the flip-flops. Some of the features of ripple counter are:

1. It is an asynchronous counter.
2. Different flip-flops are used with a different clock pulse.
3. All the flip-flops are used in toggle mode.
4. Only one flip-flop is applied with an external clock pulse and another flip-flop clock is obtained from the output of the previous flip-flop.
5. The flip-flop applied with an external clock pulse act as LSB (Least Significant Bit) in the counting sequence.

for table click here

25.What is state assignment? Explain with a suitable example?

State assignment refers to the process of assigning binary values to the states of a sequential machine. The binary values should be given to the states in such a way that flip-flop input functions may be implemented with a minimum number of logic gates.

State assignment rules are as follows:
Rule 1: States having the same next state for a given input condition should have assignments that can be grouped into logically adjacent cells in a K-map.
Rule 2: States that are the next states of a single state should have assignments that can be grouped into logically adjacent cells in a K-map.

for-example-click here

26.Explain the working of the following

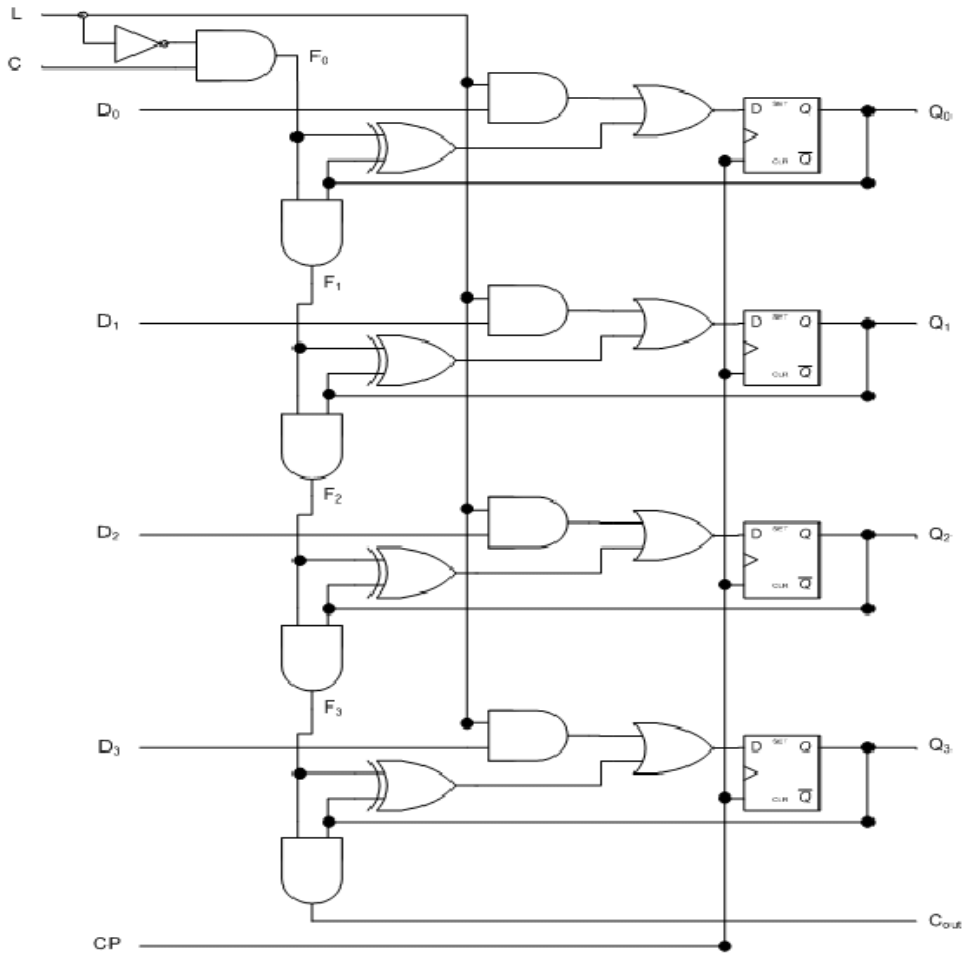
i) J-K flip-flop

ii) S- R flip-flop

iii) D flip-flop

refer answer-3

27.Explain the design of a 4 bit binary counter with parallel load in detail?



With the clear, load, and increment inputs all at 0, the outputs do not change even when pulses are applied to the C terminals. If the clear and load inputs are maintained at logic 0, the increment input controls the operation of the counter and the outputs change to the next binary count for each positive transition of the clock. The input data are loaded into the flip-flops when the load control input is equal to I provided that the clear is disabled, but the increment input can be 0 or I. The register is cleared to 0 with the clear control regardless of the values in the load and increment inputs.

28.How does it set eliminate is a Master –slave J-K flip-flop?

refer answer-5

29.Explain synchronous and ripple counters compare their merits and demerits?

Asynchronous counters are the simplest type of counters, easiest to design requiring minimum hardware. They are called so because all the flip flops in the counter are not made to change their states simultaneously i.e. these are not clocked simultaneously.

An asynchronous counter uses T flip flops to perform the counting function.

And these are commonly called as '**Ripple counters**' because only one of the flip flops is directly clocked from an external clock source and as the number of pulses increases, the consecutive flip flops get clocked which gives a 'ripple effect'.

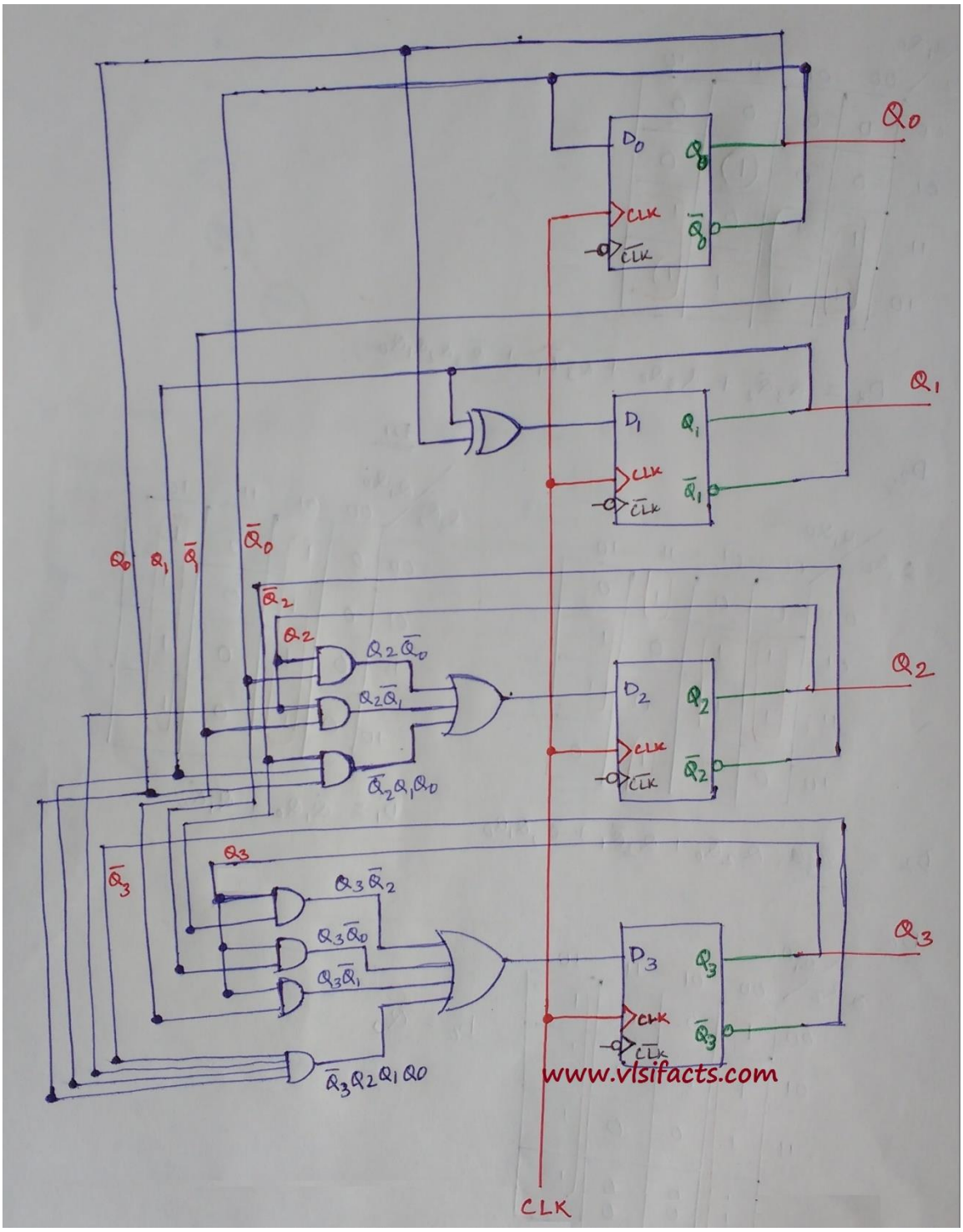
Compared with ripple-through counters, synchronous counters have certain advantages which may be important in some cases.

A major advantage is that all flip-flops in the counter change state at the same time thus avoiding the delay in propagating the clock pulse from one stage to the next.

Some disadvantages of synchronous systems are apparent however in that more components are often required if a large number bf stages are involved.

It should also be noted that at some state of the count, the outputs of most or all of the flip-flops may change from **1** to **0** or **0** to **1** simulataneously which can give rise to noise spikes on the supply rail.

30.Design a 4 bit binary synchronous counters with D-flip flop



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