EXPERIMENT No. 02

MAIN CODE:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity asd is
  Port ( a : in STD_LOGIC_VECTOR (3 downto 0);
  b : in STD_LOGIC_VECTOR (3 downto 0);
  m : in STD_LOGIC_VECTOR (2 downto 0);
  y : out STD_LOGIC_VECTOR (3 downto 0));
end asd;

architecture Behavioral of asd is
begin
process(a,b,m)
begin
case m is
when "000"=> y <= a+b;
when "001"=> y <= a-b;
when "010"=> y <= a and b;
when "011"=> y <= a or b;
when "100"=> y <= a nand b;
when "101"=> y <= a nor b;
when "110"=> y <= a xor b;
when "111"=> y <= a;
when others => y <= "0000";
end case;
end process;
end Behavioral;
```

TEST BENCH:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.all;
USE ieee.numeric_std.ALL;

ENTITY ertrt_vhd IS
END ertrt_vhd;

ARCHITECTURE behavior OF ertrt_vhd IS
  -- Component Declaration for the Unit Under Test (UUT)
  COMPONENT asd
  PORT(
    a : IN std_logic_vector(3 downto 0);
    b : IN std_logic_vector(3 downto 0);
    m : IN std_logic_vector(2 downto 0);
    y : OUT std_logic_vector(3 downto 0)
    );
END COMPONENT;

  --Inputs
  SIGNAL a : std_logic_vector(3 downto 0) := (others=>'0');
  SIGNAL b : std_logic_vector(3 downto 0) := (others=>'0');
  SIGNAL m : std_logic_vector(2 downto 0) := (others=>'0');

  --Outputs
  SIGNAL y : std_logic_vector(3 downto 0);
BEGIN
  -- Instantiate the Unit Under Test (UUT)
  uut: asd PORT MAP(
       a => a,
       b => b,
       m => m,
       y => y
  );
  tb : PROCESS
  BEGIN
    -- Wait 100 ns for global reset to finish
    wait for 100 ns;
    a<="1000";
    b<="0100";
```

```
    m<="000";
    wait for 100 ns;
a<="1000";
    b<="0100";
    m<="001";
    wait for 100 ns;
    a<="1000";
    b<="0100";
    m<="010";
    wait for 100 ns;
    a<="1000";
    b<="0100";
    m<="011";
    wait for 100 ns;
    a<="1000";
    b<="0100";
    m<="100";
    wait for 100 ns;
    a<="1000";
    b<="0100";
    m<="101";
    wait for 100 ns;
    a<="1000";
    b<="0100";
    m<="110";
    wait for 100 ns;
    a<="1000";
    b<="0100";
    m<="111";
    wait for 100 ns;
    wait; -- will wait forever
END PROCESS;
END;
```

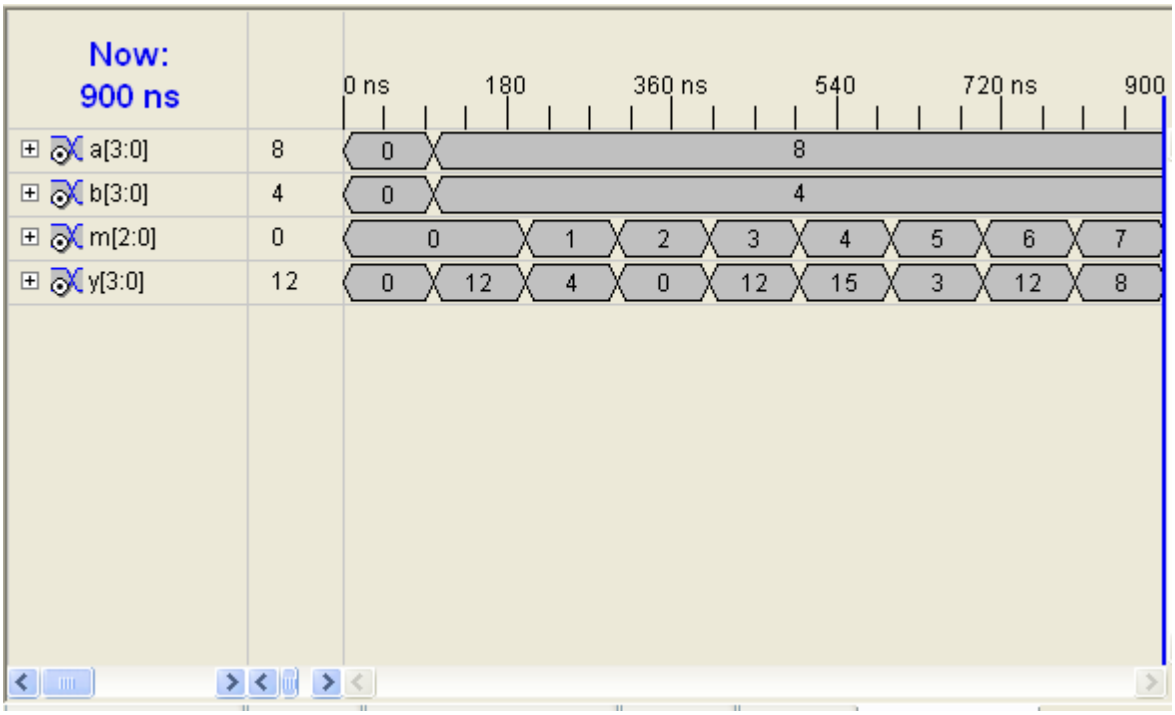
Final Results :

RTL Top Level Output File Name : asd.ngr
Top Level Output File Name : asd
Output Format : NGC
Optimization Goal : Speed
Keep Hierarchy : NO

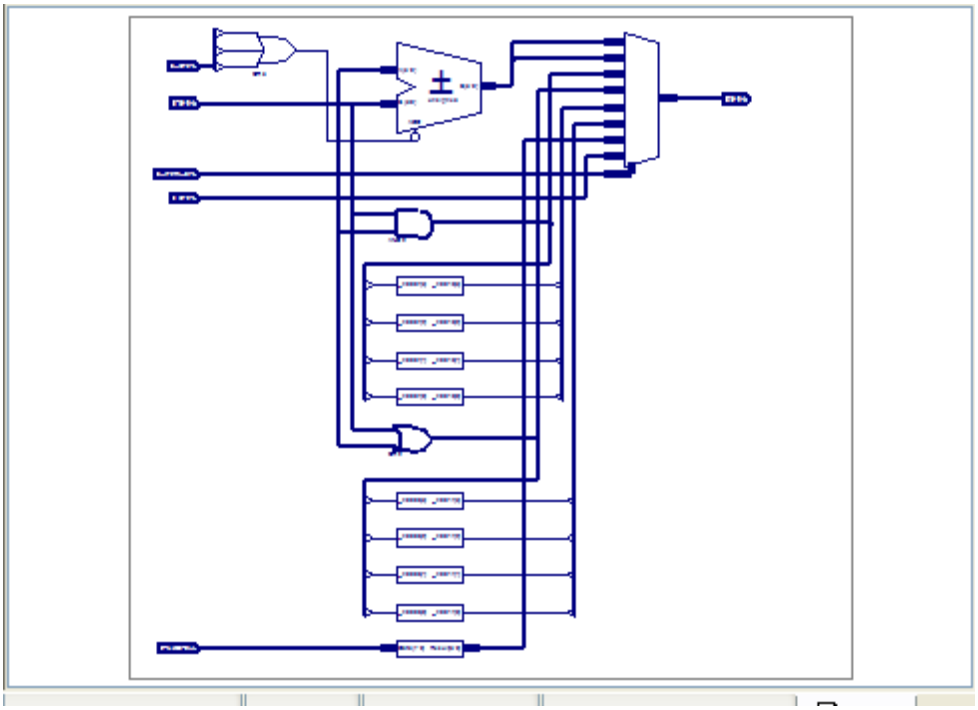
Design Statistics
IOs : 15

Cell Usage :
BELS : 33
LUT2 : 1
LUT3 : 16
LUT4 : 4
MUXF5 : 8
MUXF6 : 4
IO Buffers : 15
IBUF : 11
OBUF : 4

TEST BENCH WAVEFORM:



SIMULATION:



EXPERIMENT No. 03

MAIN CODE:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity qwedweer is
   Port ( d : in STD_LOGIC_VECTOR (3 downto 0);
      clk : in STD_LOGIC;
      rst : in STD_LOGIC;
      q : inout STD_LOGIC_VECTOR (3 downto 0);
      m : in STD_LOGIC_VECTOR (1 downto 0));
end qwedweer;

architecture Behavioral of qwedweer is
signal lsbin,msbin:std_logic;
signal clk_divider: std_logic_vector(23 downto 0);
begin
process(clk,rst)
begin
if rst='1' then
q<="0000";
elsif clk'event and clk='1' then
if clk_divider<x"3fffff" then
clk_divider<= clk_divider +'1';
else
clk_divider<=x"000000";
msbin<=d(3);
lsbin<=d(0);
case m is
when "00"=> q <= d;
when "01"=> q <= q (2 downto 0)& lsbin;
when "10"=> q <= msbin & q(3 downto 1);
when others=> q <= "0000";
```

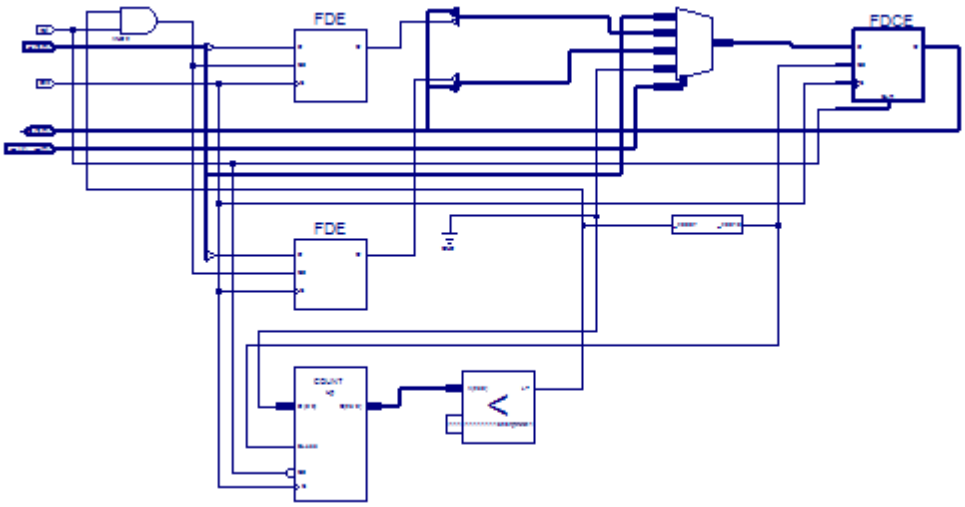
```
end case;
end if;
end if;
end process;
end Behavioral;
```

FINAL RESULT:

```
RTL Top Level Output File Name     : qwedweer.ngr
Top Level Output File Name         : qwedweer
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : NO
Design Statistics

# IOs                              : 12
Cell Usage :

# BELS                             : 99
#      GND                         : 1
#      INV                         : 3
#      LUT2                        : 1
#      LUT2_D                      : 1
#      LUT2_L                      : 25
#      LUT3                        : 4
#      LUT4                        : 4
#      LUT4_L                      : 5
#      MULT_AND                    : 1
#      MUXCY                       : 30
#      VCC                         : 1
#      XORCY                       : 23
#                                  30
FlipFlops/Latches
#      FDCE                        : 4
#      FDE                         : 26
# Clock Buffers                    : 1
```

BUFGP : 1
IO Buffers : 11
IBUF : 7
OBUF : 4

RTL SCHEMATIC:



EXPERIMENT No. 04

MAIN CODE:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity pppp is
   Port ( clk : in STD_LOGIC;
   en : in STD_LOGIC;
   din : in STD_LOGIC_VECTOR (7 downto 0);
   dout : out STD_LOGIC_VECTOR (7 downto 0);
   full : out STD_LOGIC;
   empty : out STD_LOGIC);
end pppp;

architecture Behavioral of pppp is

type mem is array (0 to 255)of std_logic_vector(7 downto 0);
signal memory:mem;
signal readptr,writep tr:std_logic_vector(7 downto 0);
 SIGNAL CLK_DIVIDER :std_logic_vector(23 downto 0);

begin
process(clk)
begin
if clk' event and clk='1' then
if clk_divider < x"7fffff" then
clk_divider<= clk_divider +'1';
 else
clk_divider<= x"000000";

if en='1' then
dout<=memory(conv_integer(readptr));
readptr<=readptr+'1';
else memory(conv_integer(writeptr))<=din;
```

```
writeptr<=writeptr+'1';
end if;
if writeptr="11111111" then
full<='1';
writeptr<="00000000";
else full<='0';
end if;
if writeptr="00000000" then
empty<='1';
else empty<='0';
end if;
end if;
end if;
end process;
end Behavioral;
```

FINAL RESULT:

```
RTL Top Level Output File Name :     pppp.ngr
Top Level Output File Name :     pppp
Output Format :     NGC
Optimization Goal :     Speed
Keep Hierarchy :     NO

Design Statistics
# IOs   20

 Cell Usage
# BELS                    : 118
#      GND                : 1
#      INV                : 5
#      LUT1               : 11
#      LUT1_L             : 12
#      LUT2               : 8
#      LUT2_D             : 1
#      LUT2_L             : 3
#      LUT3               : 2
#      LUT3_L             : 3
#      LUT4               : 9
#      LUT4_L             : 9
#      MUXCY              : 30
#      VCC                : 1
```

```
#      XORCY                : 23
# FlipFlops/Latches         : 42
#      FDE                  : 10
#      FDR                  : 24
#      FDRE                 : 8
# RAMS                      : 1
#      RAMB16_S9_S9         : 1
# Clock Buffers             : 1
#      BUFGP                : 1
# IO Buffers                : 19
#      IBUF                 : 9
#      OBUF                 : 10
```

MAIN CODE:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity fiffo is
Port ( din : in STD_LOGIC_VECTOR (7 downto 0);
   clk : in STD_LOGIC;
   en : in STD_LOGIC;
   full : out STD_LOGIC;
   empty : out STD_LOGIC;
   dout : out STD_LOGIC_VECTOR (7 downto 0));
end fiffo;

architecture Behavioral of fiffo is
type mem is array(0 to 255)of std_logic_vector(7 downto 0);
signal memory:mem;
signal readptr,writeptr: std_logic_vector(7 downto 0);
signal clk_divider :std_logic_vector(23 downto 0);
begin
process(clk)
begin
if clk' event and clk='1' then
if clk_divider< x"0fffff" then
clk_divider<= clk_divider+'1';
else
clk_divider <=x"000000";
if en='1' then
memory (conv_integer(writeptr))<= din;
writeptr <= writeptr+'1';
else
dout<= memory(conv_integer(readptr));
readptr<= readptr+'1';
end if;
```

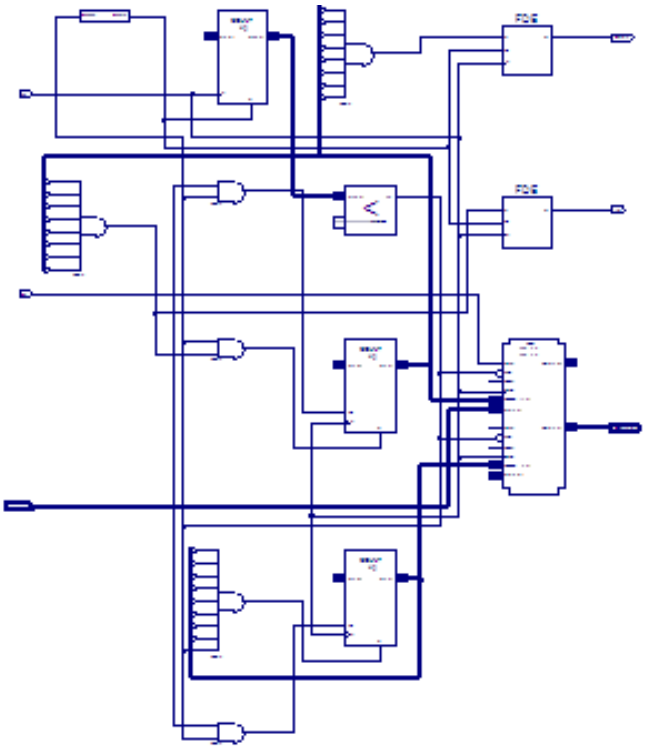
```
if readptr="11111111" then
readptr <= "00000000";
end if;
if writeptr="11111111" then
writeptr <= "00000000";
full <='1';
else
full<='0';
end if;
if writeptr= "00000000" then
empty<='1';
else
empty<='0';
end if;
end if;
end if;
end process;
end Behavioral;
```

FINAL RESULT:

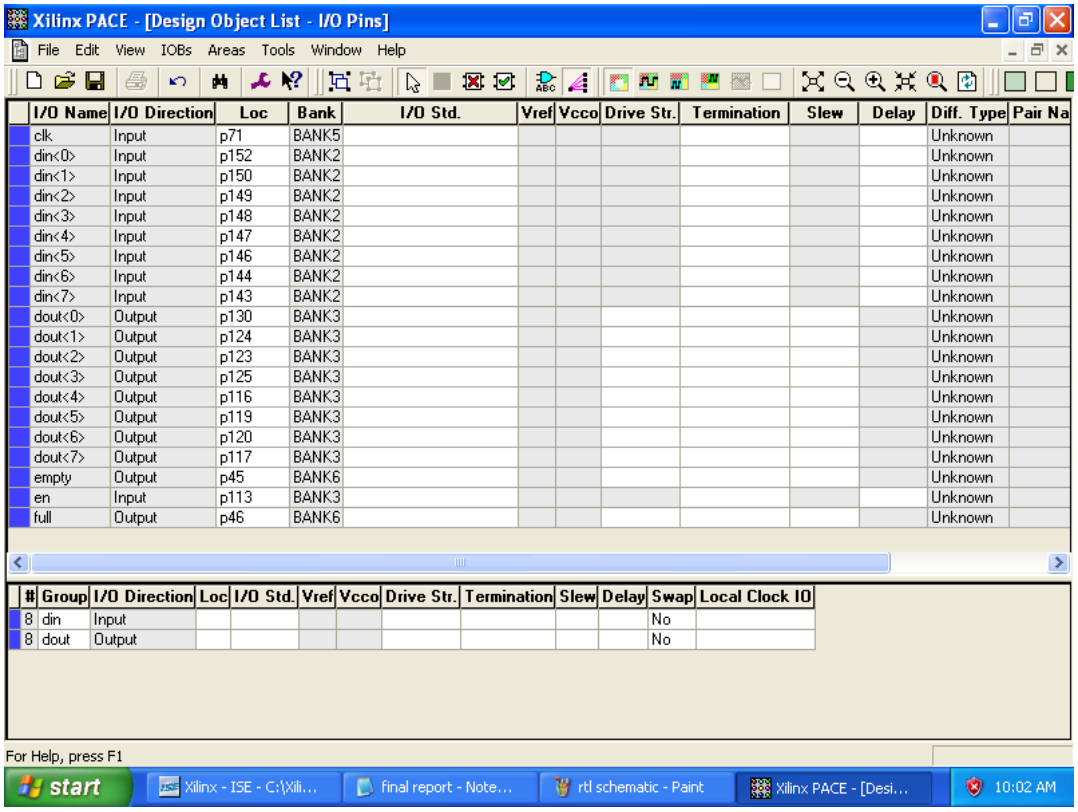
```
RTL Top Level Output File Name   :    pppp.ngr
Top Level Output File Name :     :    fiffo
Output Format :                  NGC
Optimization Goal                :    Speed
Keep Hierarchy :                    NO


Design Statistics
# IOs                            20
Cell Usage :

# BELS                                : 118
#      GND                           : 1
#      INV                           : 3
#      LUT1                               : 11
#      LUT1_L                        : 12
#      LUT2                               : 8
#      LUT2_D                             : 2
#      LUT2_L                             : 3
#      LUT3                               : 2
#      LUT3_L                             : 2
#      LUT4                               : 11
#      LUT4_L                             : 10
```

```
#      MUXCY                           : 29
#      VCC                             : 1
#      XORCY                           : 23
# FlipFlops/Latches                    : 42
#      FDE                             : 2
#      FDR                             : 24
#      FDRE                            : 16
# RAMS                                 : 1
#      RAMB16_S9_S                     : 19
# Clock Buffers                        : 1
#      BUFGP                           : 1
# IO Buffers                           : 19
#      IBUF                            : 9
#      OBUF                            : 10
```

RTL SCHEMATIC:

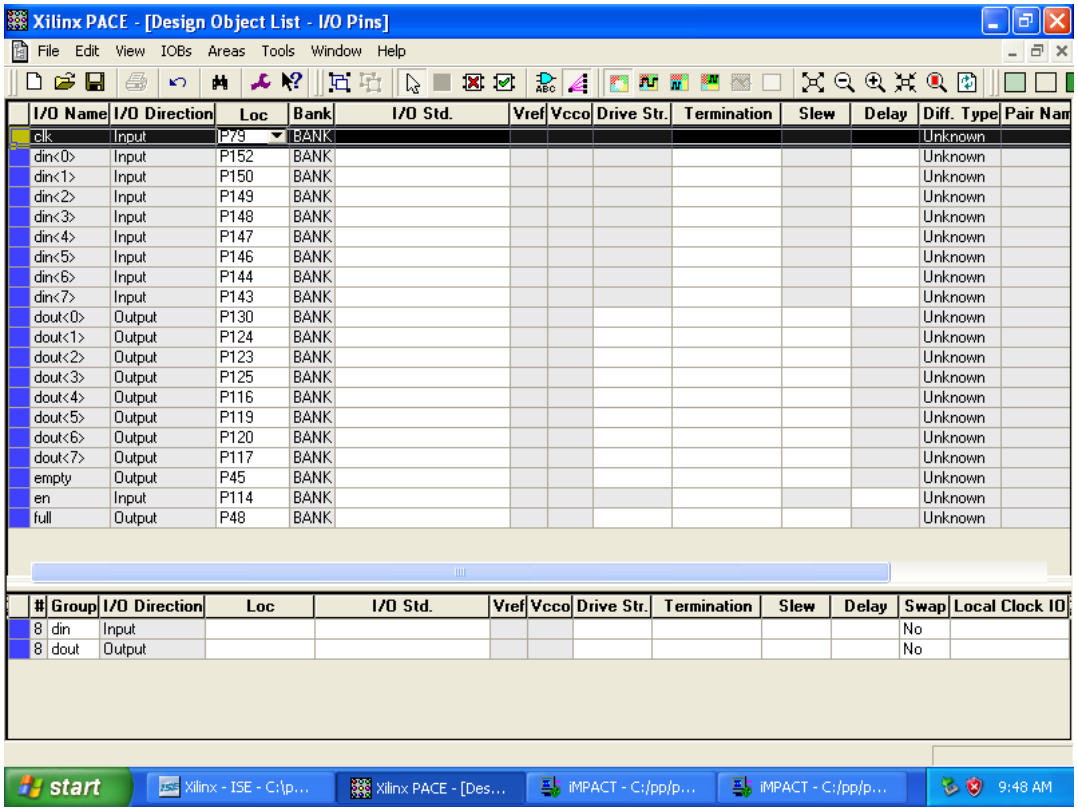


PIN PACKAGE:



I/O Name	I/O Direction	Loc	Bank	I/O Std.	Vref	Vcco	Drive Str.	Termination	Slew	Delay	Diff. Type	Pair Na
clk	Input	p71	BANK5								Unknown	
din<0>	Input	p152	BANK2								Unknown	
din<1>	Input	p150	BANK2								Unknown	
din<2>	Input	p149	BANK2								Unknown	
din<3>	Input	p148	BANK2								Unknown	
din<4>	Input	p147	BANK2								Unknown	
din<5>	Input	p146	BANK2								Unknown	
din<6>	Input	p144	BANK2								Unknown	
din<7>	Input	p143	BANK2								Unknown	
dout<0>	Output	p130	BANK3								Unknown	
dout<1>	Output	p124	BANK3								Unknown	
dout<2>	Output	p123	BANK3								Unknown	
dout<3>	Output	p125	BANK3								Unknown	
dout<4>	Output	p116	BANK3								Unknown	
dout<5>	Output	p119	BANK3								Unknown	
dout<6>	Output	p120	BANK3								Unknown	
dout<7>	Output	p117	BANK3								Unknown	
empty	Output	p45	BANK6								Unknown	
en	Input	p113	BANK3								Unknown	
full	Output	p46	BANK6								Unknown	

#	Group	I/O Direction	Loc	I/O Std.	Vref	Vcco	Drive Str.	Termination	Slew	Delay	Swap	Local Clock IO
8	din	Input									No	
8	dout	Output									No	



I/O Name	I/O Direction	Loc	Bank	I/O Std.	Vref	Vcco	Drive Str.	Termination	Slew	Delay	Diff. Type	Pair Nam
clk	Input	P79	BANK								Unknown	
din<0>	Input	P152	BANK								Unknown	
din<1>	Input	P150	BANK								Unknown	
din<2>	Input	P149	BANK								Unknown	
din<3>	Input	P148	BANK								Unknown	
din<4>	Input	P147	BANK								Unknown	
din<5>	Input	P146	BANK								Unknown	
din<6>	Input	P144	BANK								Unknown	
din<7>	Input	P143	BANK								Unknown	
dout<0>	Output	P130	BANK								Unknown	
dout<1>	Output	P124	BANK								Unknown	
dout<2>	Output	P123	BANK								Unknown	
dout<3>	Output	P125	BANK								Unknown	
dout<4>	Output	P116	BANK								Unknown	
dout<5>	Output	P119	BANK								Unknown	
dout<6>	Output	P120	BANK								Unknown	
dout<7>	Output	P117	BANK								Unknown	
empty	Output	P45	BANK								Unknown	
en	Input	P114	BANK								Unknown	
full	Output	P48	BANK								Unknown	

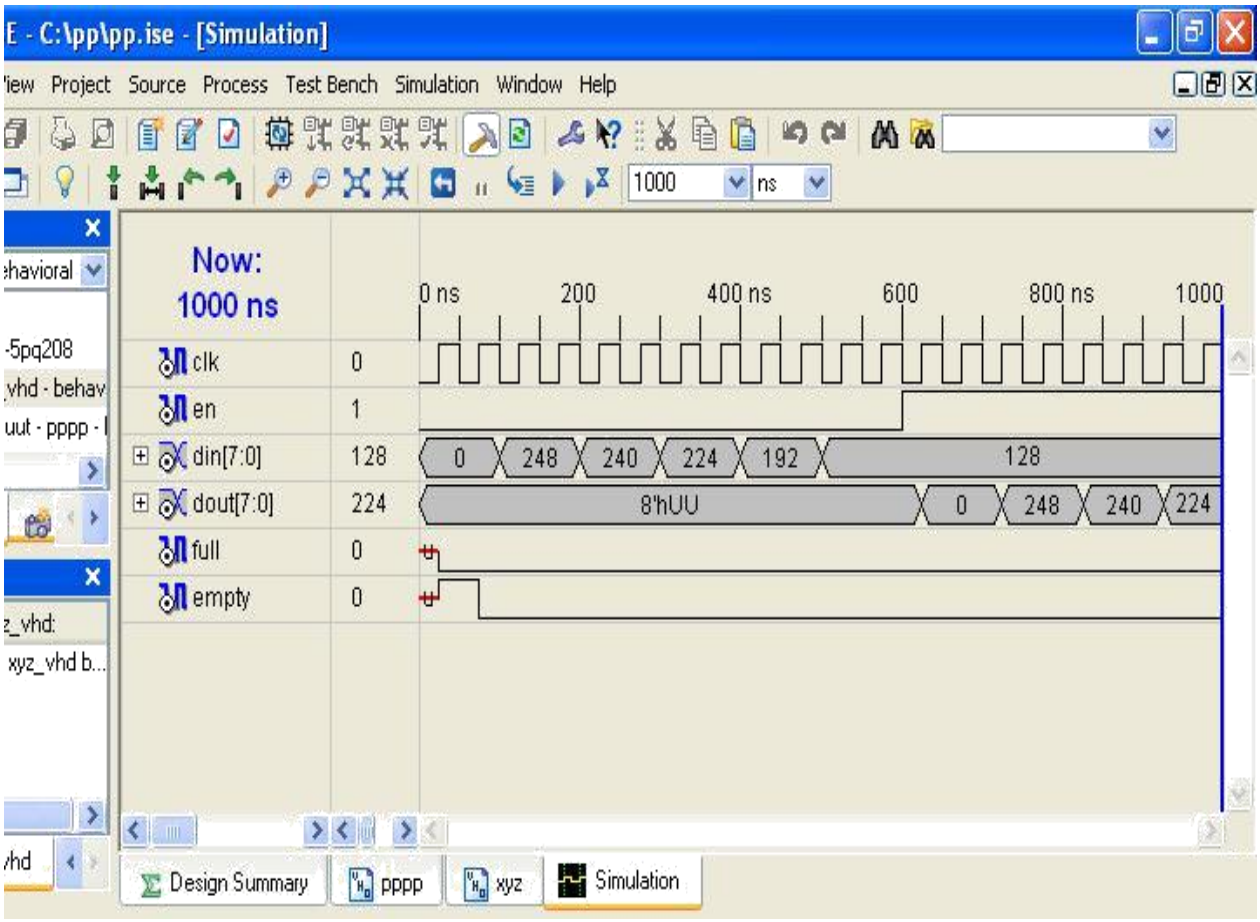
#	Group	I/O Direction	Loc	I/O Std.	Vref	Vcco	Drive Str.	Termination	Slew	Delay	Swap	Local Clock IO
8	din	Input									No	
8	dout	Output									No	

TEST BENCH:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.all;
USE ieee.numeric_std.ALL;

ENTITY xyz_vhd IS
END xyz_vhd;

ARCHITECTURE behavior OF xyz_vhd IS

        -- Component Declaration for the Unit Under Test
        (UUT) COMPONENT pppp
        PORT(
                clk : IN std_logic;
                en : IN std_logic;
                din : IN std_logic_vector(7 downto 0);
                dout : OUT std_logic_vector(7 downto 0);
                full : OUT std_logic;
                empty : OUT std_logic
                );
        END COMPONENT;

        --Inputs
        SIGNAL clk : std_logic := '0';
        SIGNAL en :  std_logic := '0';
        SIGNAL din :  std_logic_vector(7 downto 0) := (others=>'0');

        --Outputs
        SIGNAL dout : std_logic_vector(7 downto 0);
        SIGNAL full :  std_logic;
        SIGNAL empty : std_logic;

BEGIN

        -- Instantiate the Unit Under Test
        (UUT) uut: pppp PORT MAP(
                clk => clk, en
                => en, din =>
                din, dout =>
                dout, full =>
                full, empty =>
                empty
```

```
);

tb :
process
begin
clk<='0';
wait for 25 ns;

clk<='1';
wait for 25 ns;

end process;


process
begin

        -- Wait 100 ns for global reset to
        finish wait for 100 ns;
        en<='0';
        din<="11111000";

        wait for 100 ns;

        din<="11110000";

        wait for 100 ns;
        din<="11100000";

        wait for 100 ns;

        din<="11000000";

        wait for 100 ns;

        din<="10000000";

        wait for 100 ns;
        en<='1';
        wait; -- will wait forever
END process;

END;
```

TEST BENCH WAVEFORM:



EXPERIMENT No.05

MAIN CODE:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
entity keypad is
Port ( rst : in STD_LOGIC;
clk : in STD_LOGIC;
row : in STD_LOGIC_VECTOR (3 downto 0);
column : out STD_LOGIC_VECTOR (3 downto 0);
data : out STD_LOGIC_VECTOR (3 downto 0));
end keypad;
architecture Behavioral of keypad is
type state_type is(co1,co2,co3,co4);
signal coltest: state_type:= co1;
begin
process(clk,rst)
begin
if rst='1'then
coltest <= co1;
column <= "1110";
data <="0001";
elsif clk' event and clk='1' then
case coltest is
when co1=> column <="1110";
case row is
when"1110"=> data <= "0001";
when"1101"=> data <= "0100";
when"1011"=> data <= "0111";
when"0111"=> data <= "1110";
when others => coltest <= co2;
column <="1101";
end case;
when co2=> column <="1101";
case row is
when"1110"=> data <= "0010";
when"1101"=> data <= "0101";
when"1011"=> data <= "1000";
when"0111"=> data <= "0000";
```

```
when others => coltest <= co3;
column <="1011";
end case;
when co3=> column <="1011";
case row is
when"1110"=> data <= "0011";
when"1101"=> data <= "0110";
when"1011"=> data <= "1001";
when"0111"=> data <= "1111";
when others => coltest <= co4;
column <="0111";
end case;
when co4=> column <="0111";
case row is
when"1110"=> data <= "1010";
when"1101"=> data <= "1011";
when"1011"=> data <= "1100";
when"0111"=> data <= "1101";
when others => coltest <= co1;
column <="1110";
end case;
end case;
end if ;
end process;
end Behavioral;
```

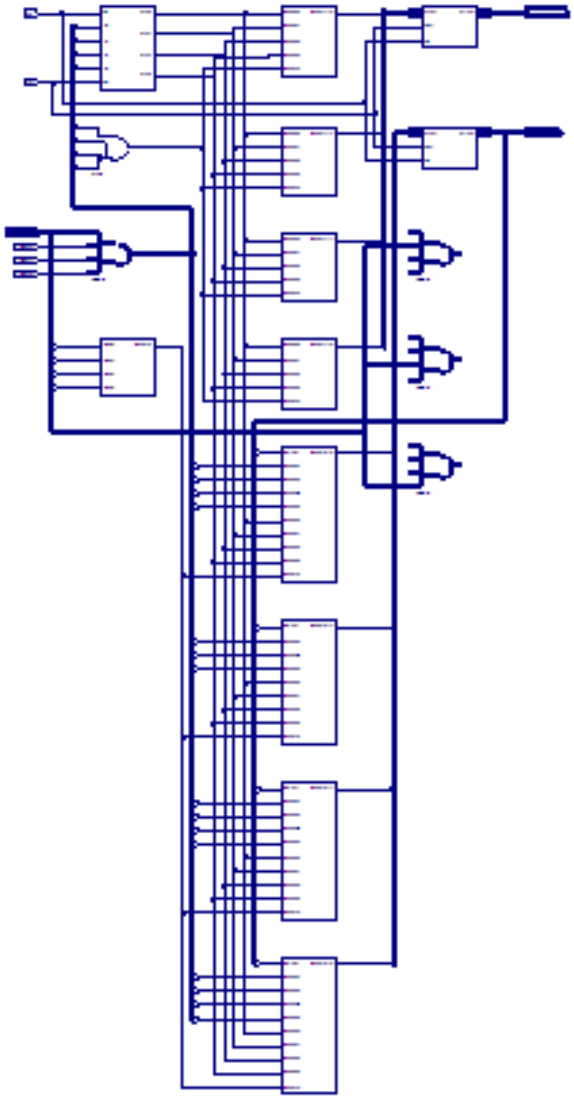
FINAL RESULT:

RTL Top Level Output File Name : keypad.ngr
Top Level Output File Name : keypad
Output Format : NGC
Optimization Goal : Speed
Keep Hierarchy : NO

Design Statistics
IOs : 14

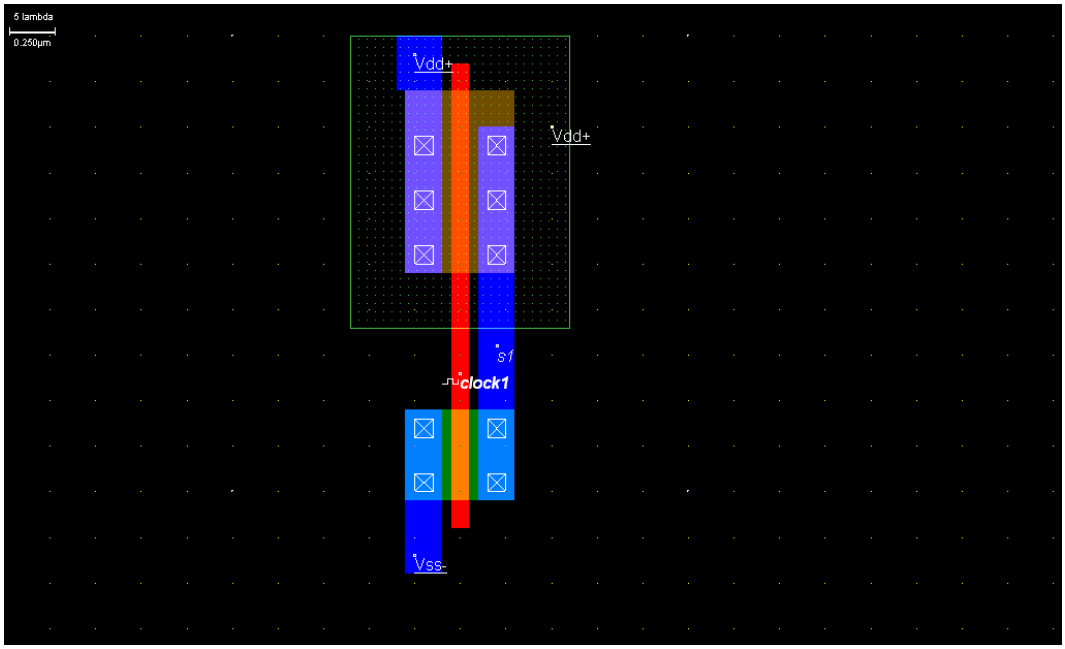
Cell Usage :
BELS : 30
INV : 1
LUT2 : 4
LUT2_L : 1
LUT3 : 1
LUT3_L : 5
LUT4 : 12
LUT4_L : 6
FlipFlops/Latches 10
FDC : 4
FDCE : 2
FDP : 4
Clock Buffers : 1
BUFGP : 1
IO Buffers : 13
IBUF : 5
OBUF : 8

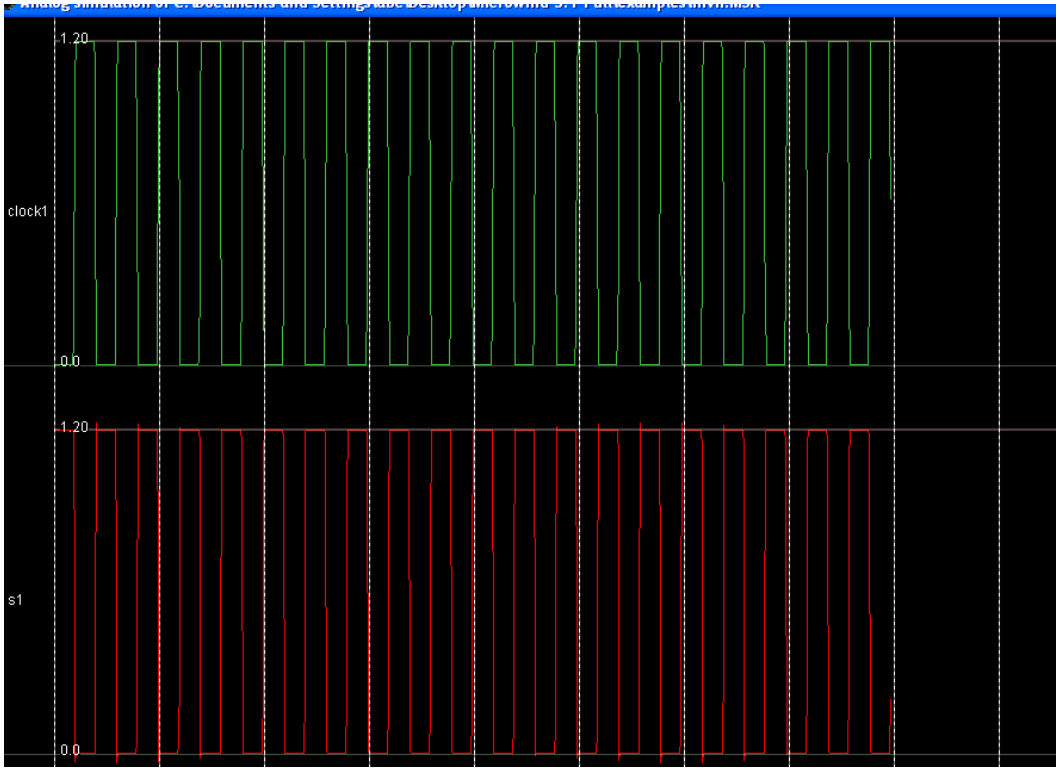
RTL SCHEMATIC:



EXPERIMENT No. 06(A)

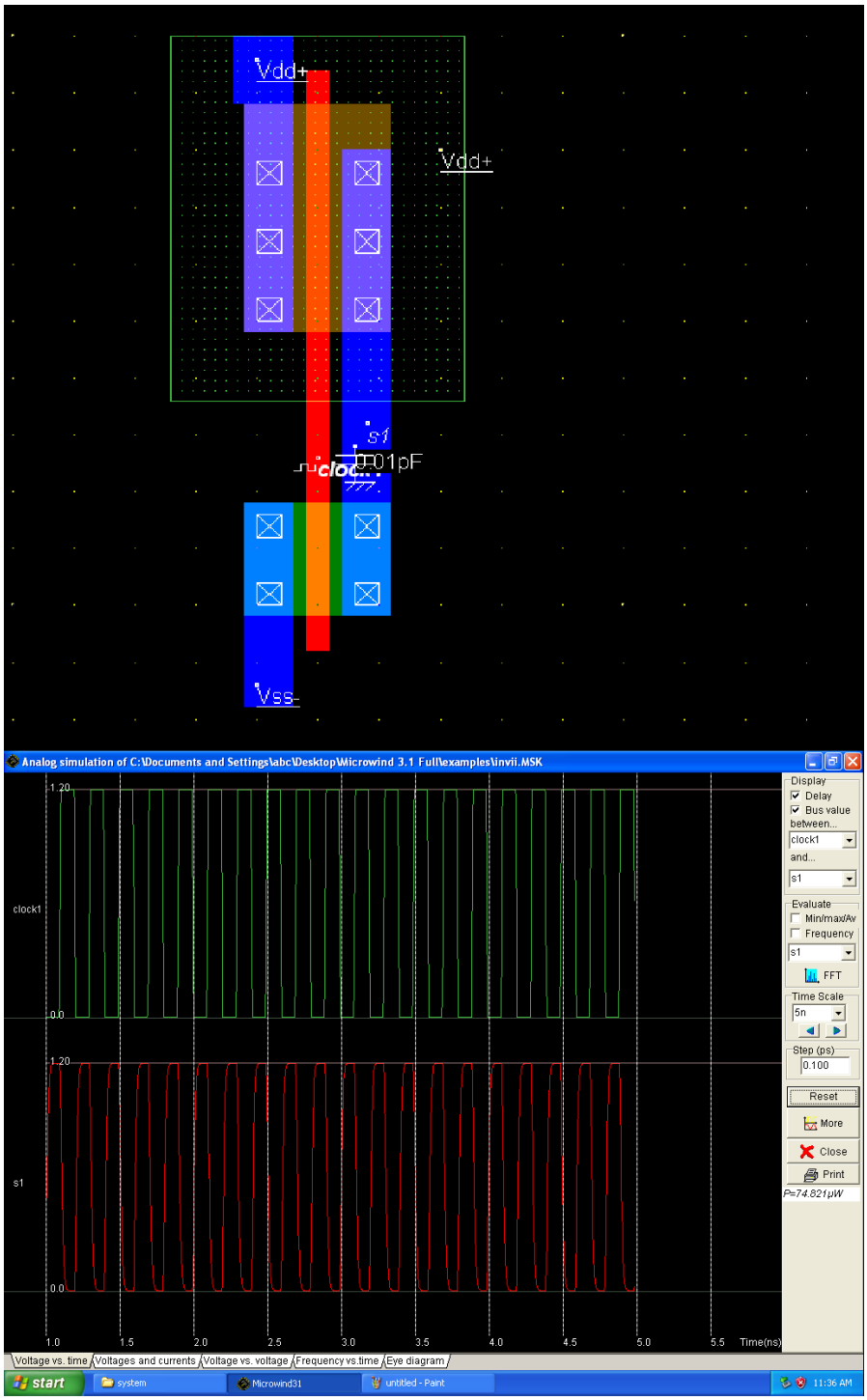
1. CMOS without Capacitor





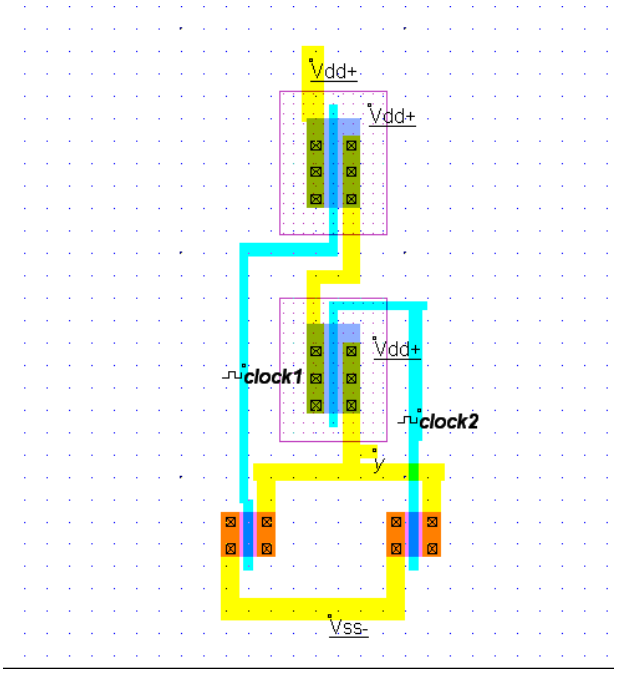
EXPERIMENT No. 06(A)

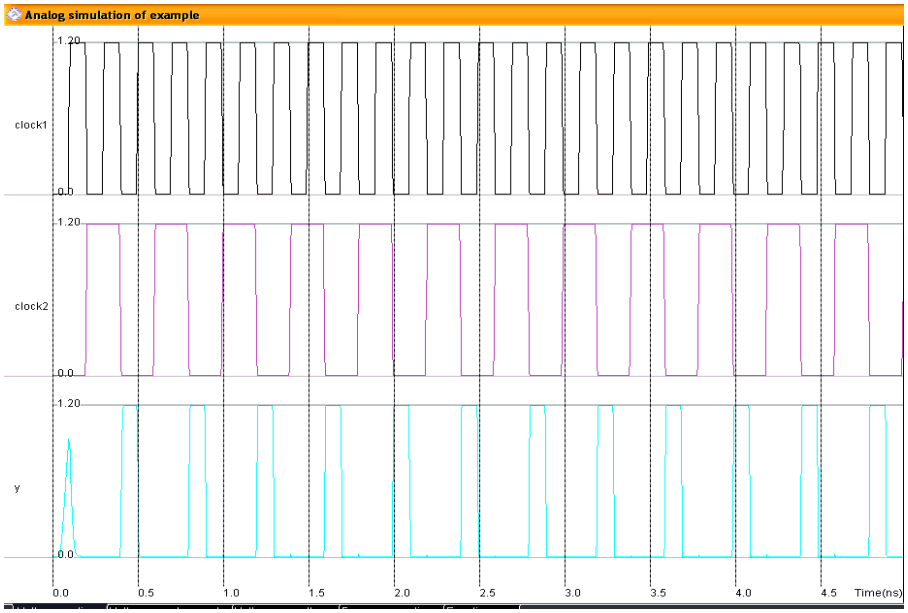
2. CMOS with Capacitor



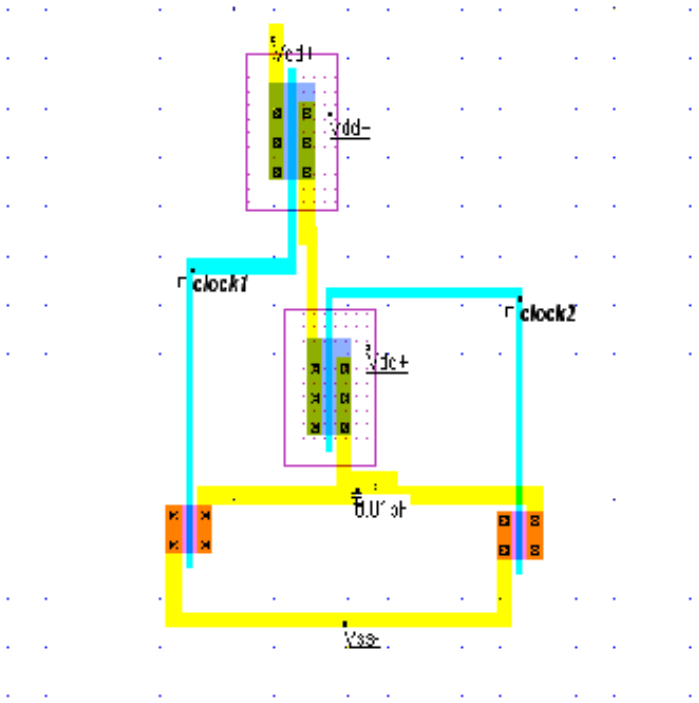
EXPERIMENT No. 06(B)

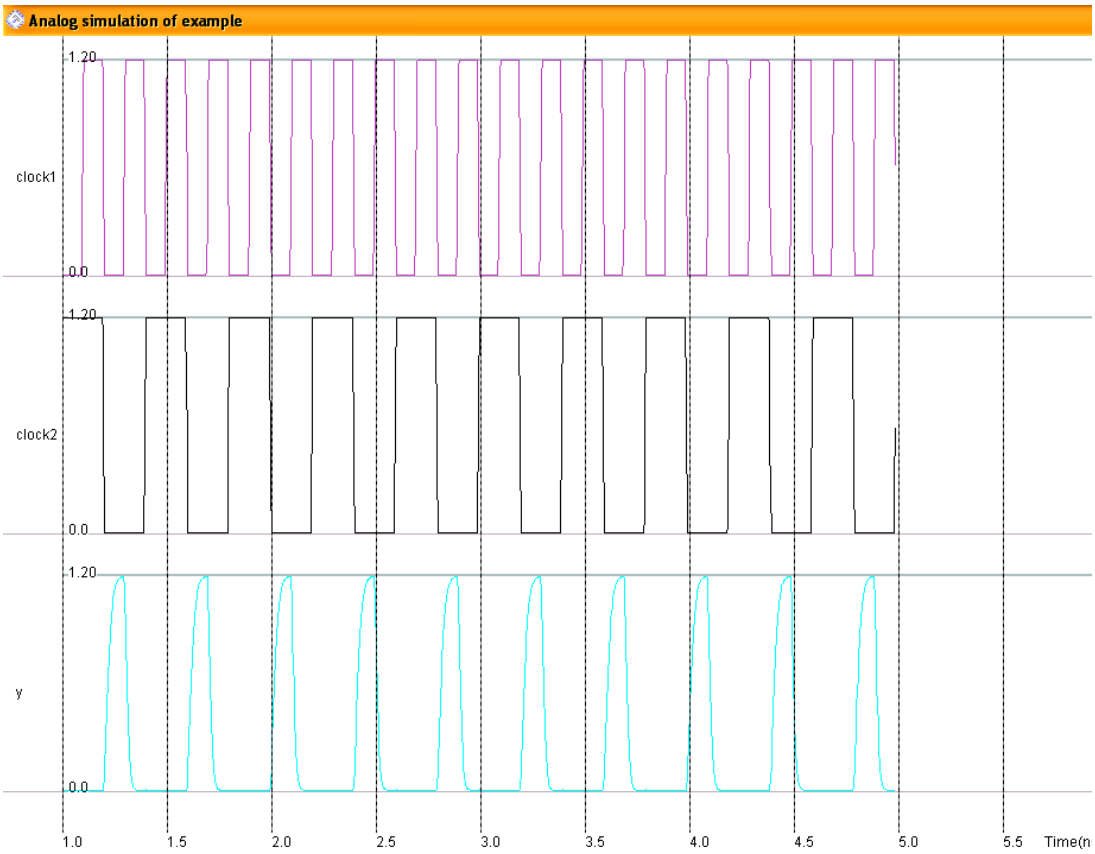
NOR : WITHOUT CAPACITOR



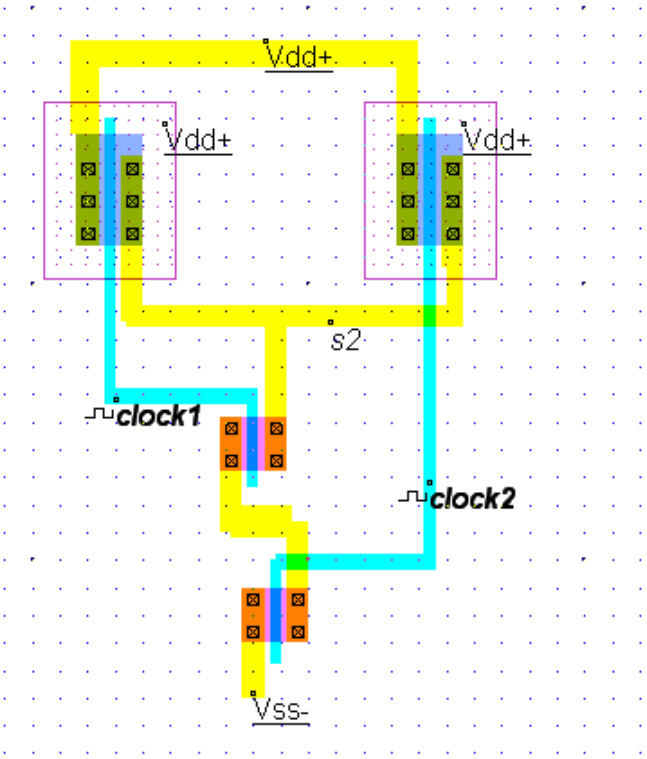


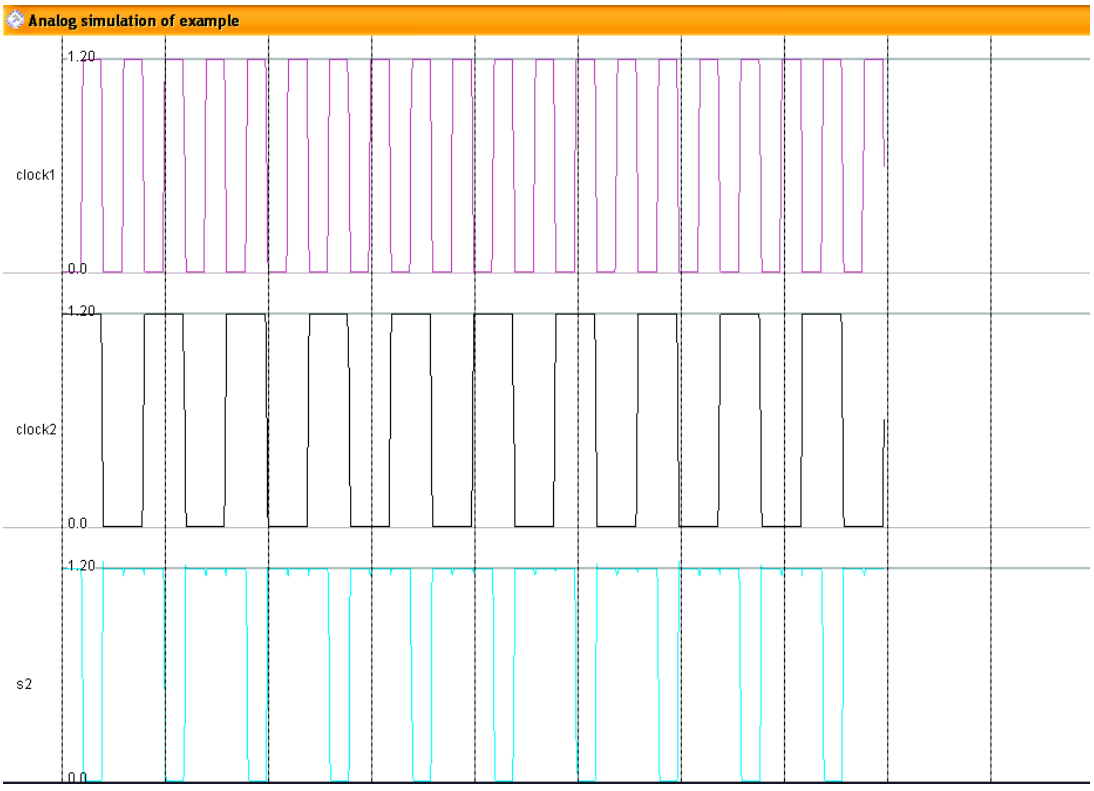
NOR : WITH CAPACITOR



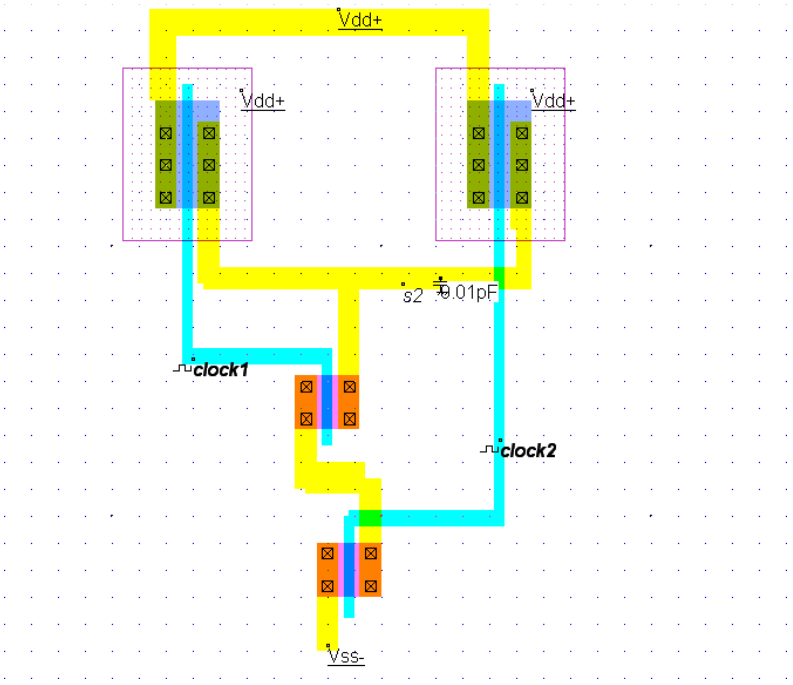


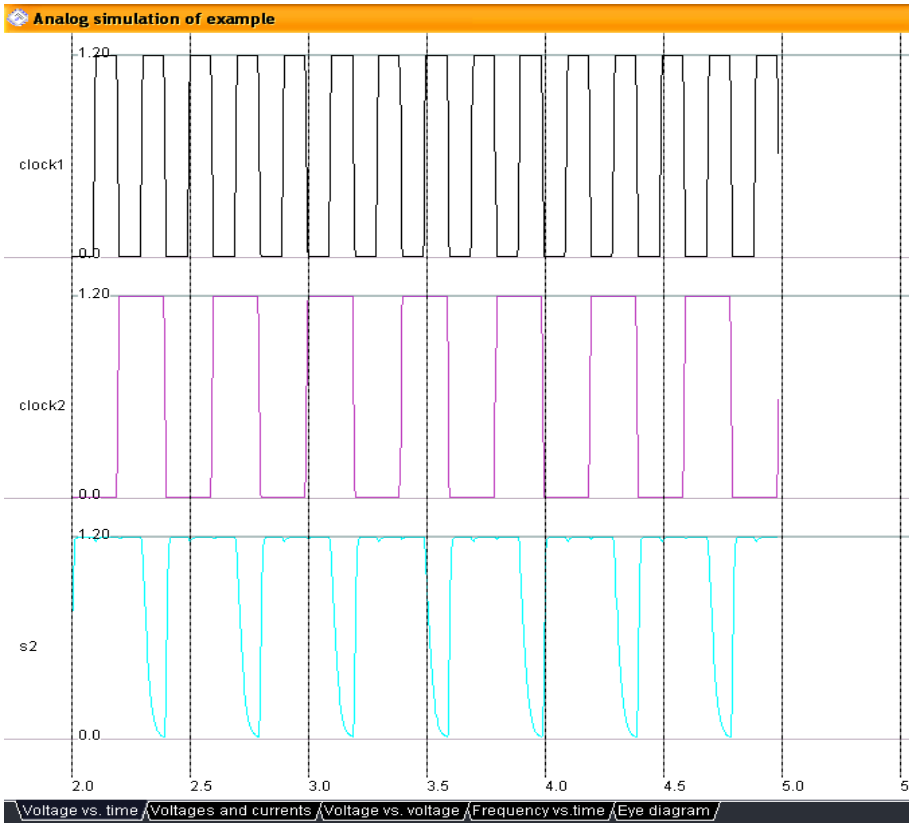
NAND: WITHOUT CAPACITOR



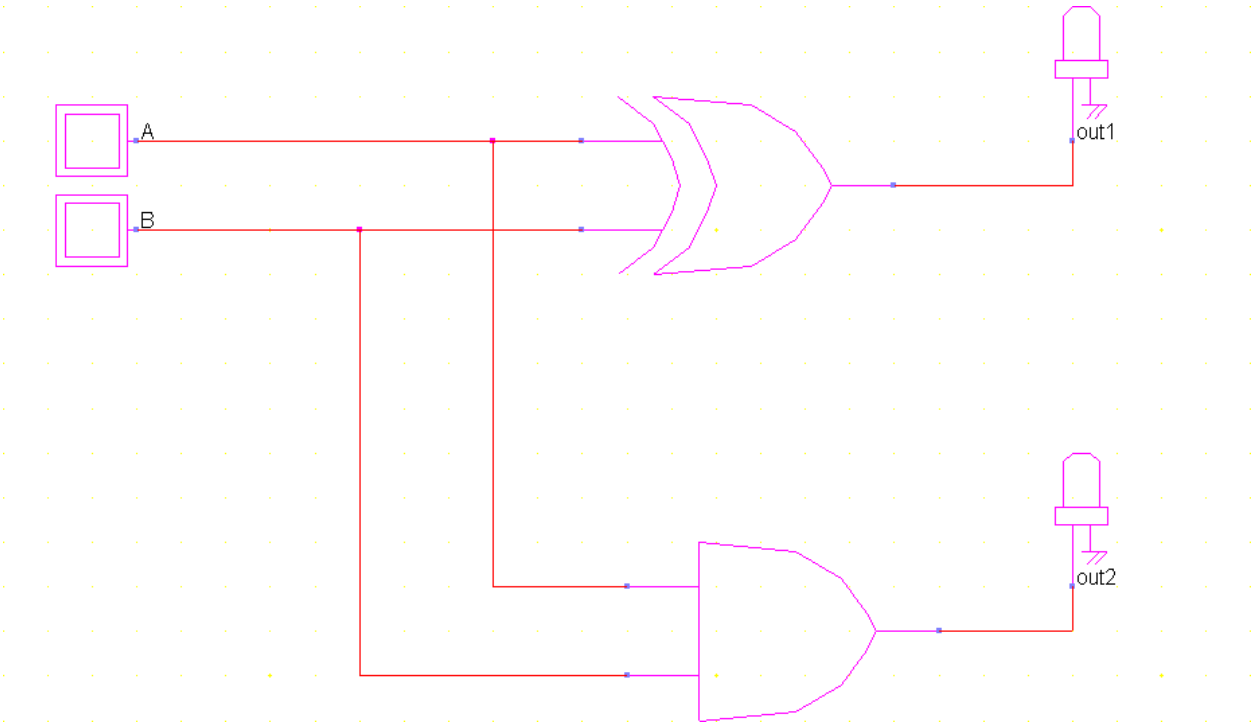


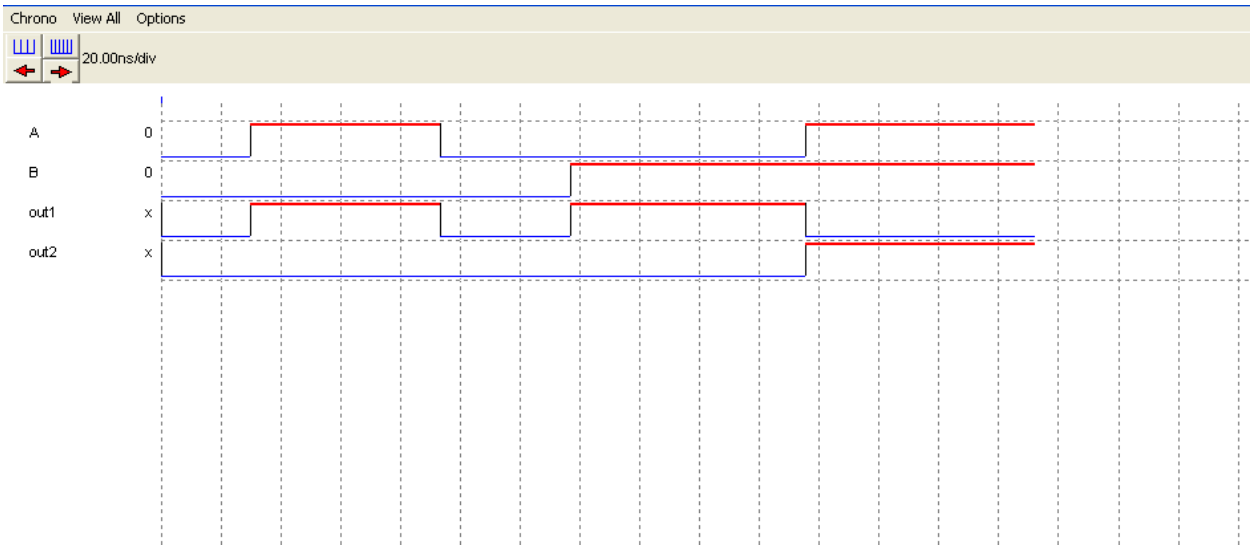
NAND: WITH CAPACITOR



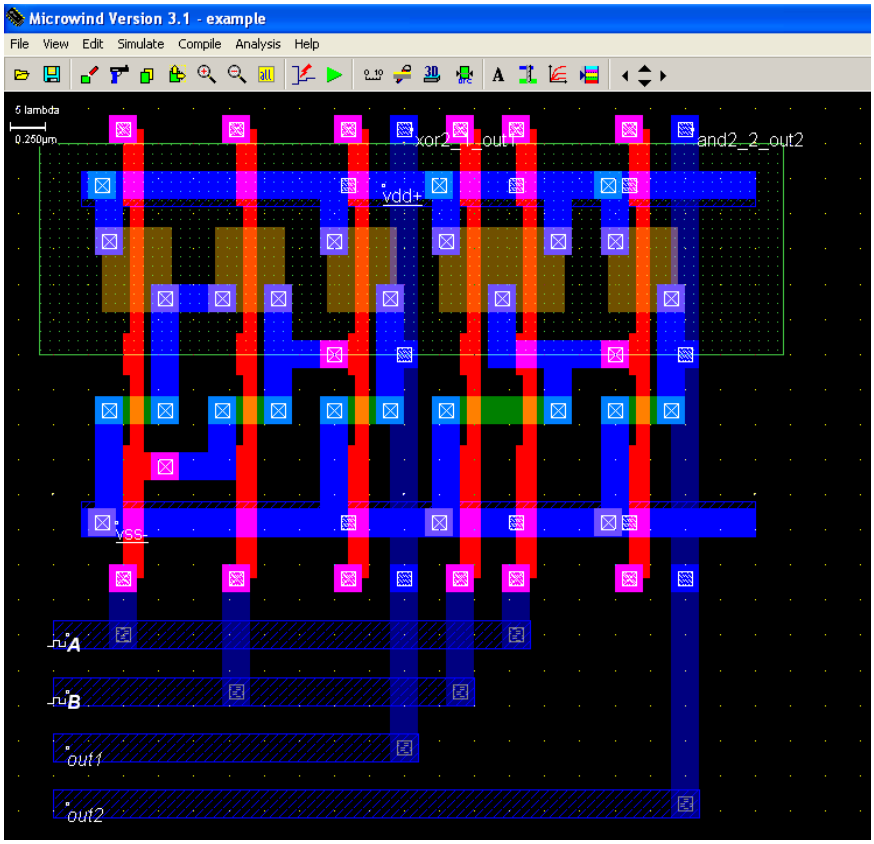


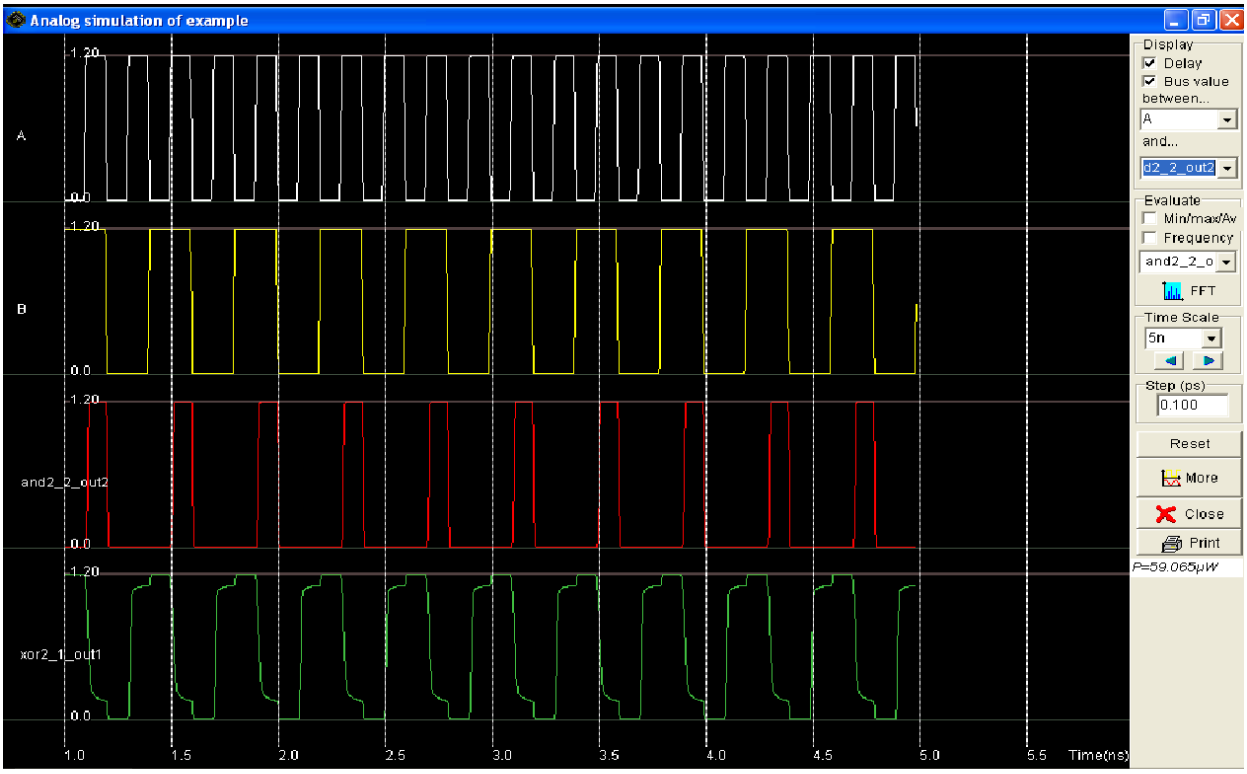
EXPERIMENT No. 06(C)



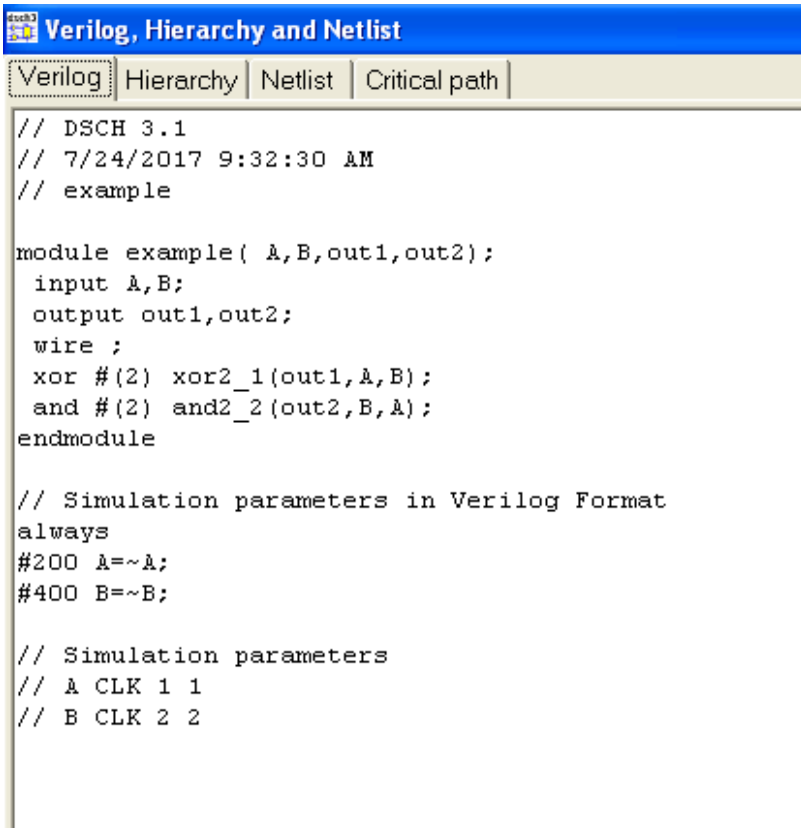


HALF ADDER:


Microwind Version 3.1 - example
File View Edit Simulate Compile Analysis Help
5 lambda
0.250µm
xor2_1_out1
and2_2_out2
vdd
vss
A
B
out1
out2

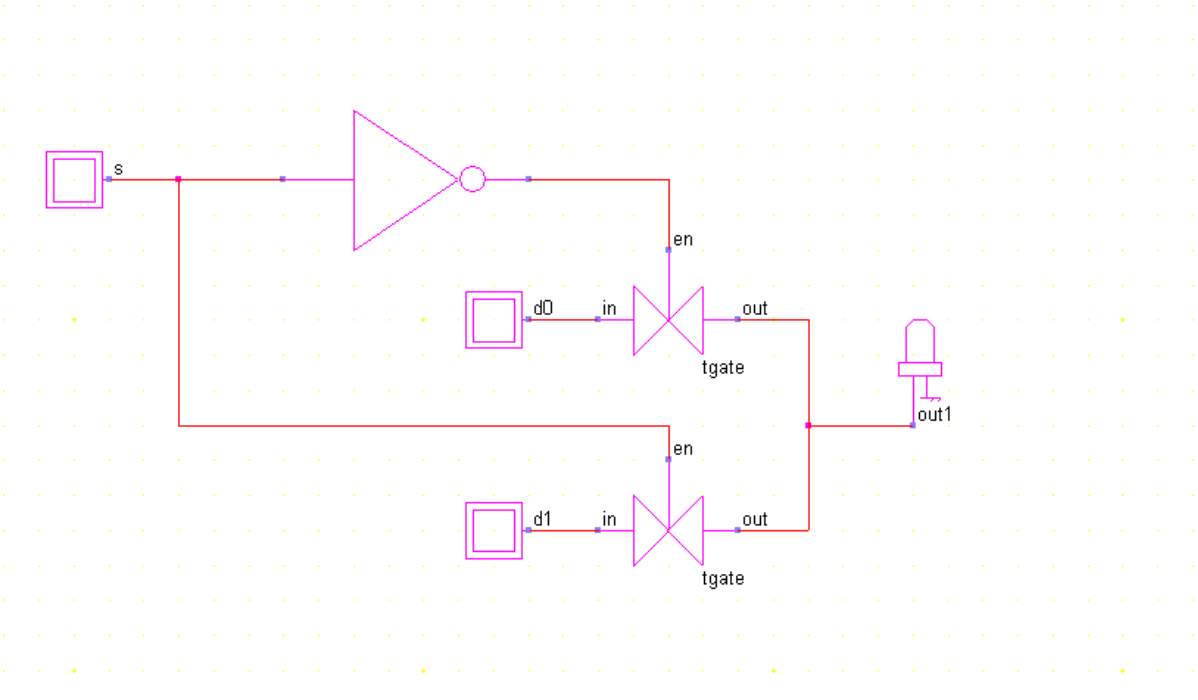

Analog simulation of example
A
B
and2_2_out2
xor2_1_out1
1.20
0.0
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
Time(ns)
Display
Delay
Bus value
between...
A
and...
d2_2_out2
Evaluate
Min/max/Av
Frequency
and2_2_o
FFT
Time Scale
5n
Step (ps)
0.100
Reset
More
Close
Print
P=59.065µW

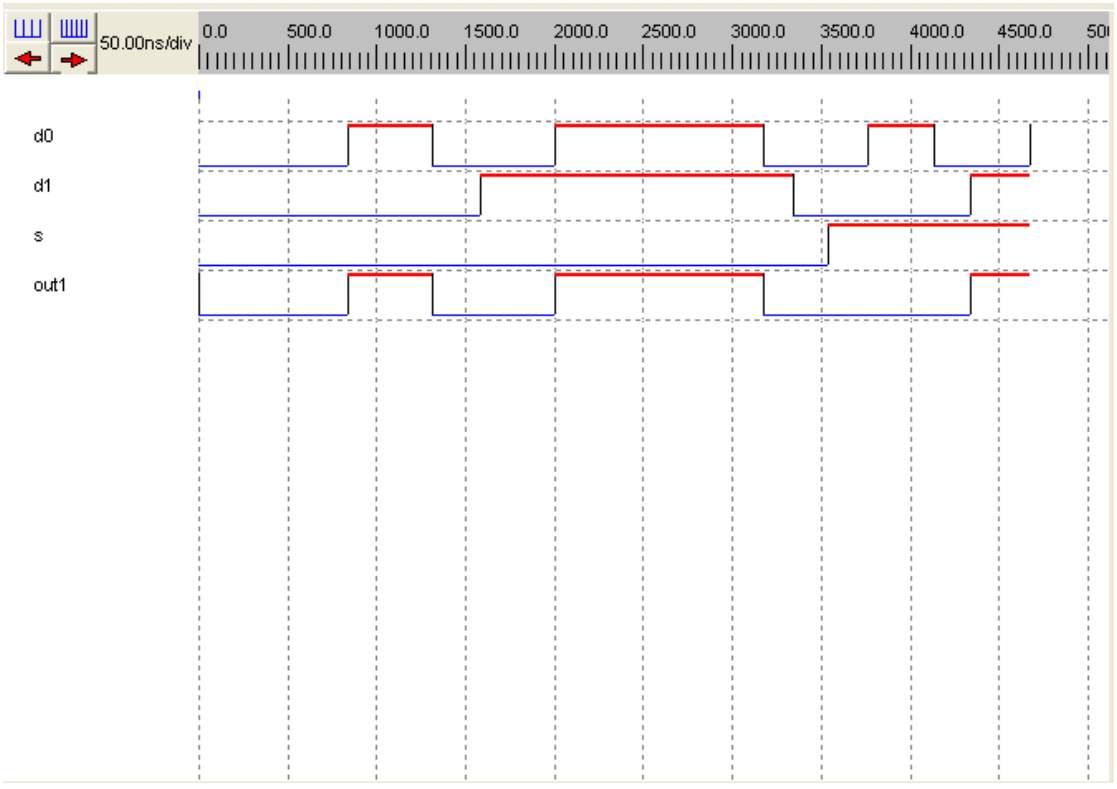
VERILOG:

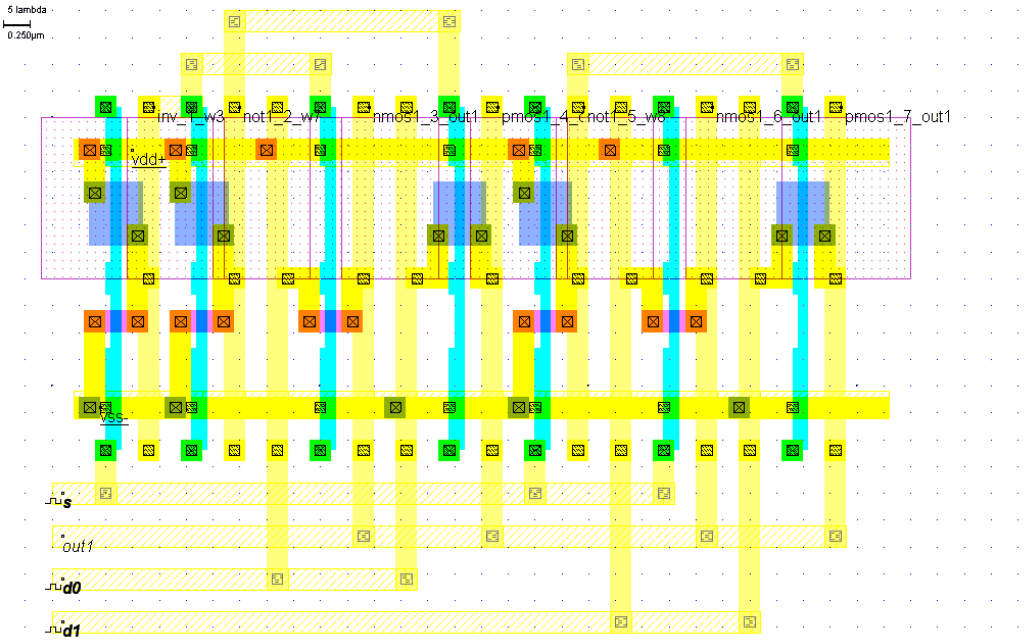

Verilog, Hierarchy and Netlist
Verilog
Hierarchy
Netlist
Critical path
// DSCH 3.1
// 7/24/2017 9:32:30 AM
// example
module example(A,B,out1,out2);
input A,B;
output out1,out2;
wire ;
xor #(2) xor2_1(out1,A,B);
and #(2) and2_2(out2,B,A);
endmodule
// Simulation parameters in Verilog Format
always
#200 A=~A;
#400 B=~B;
// Simulation parameters
// A CLK 1 1
// B CLK 2 2

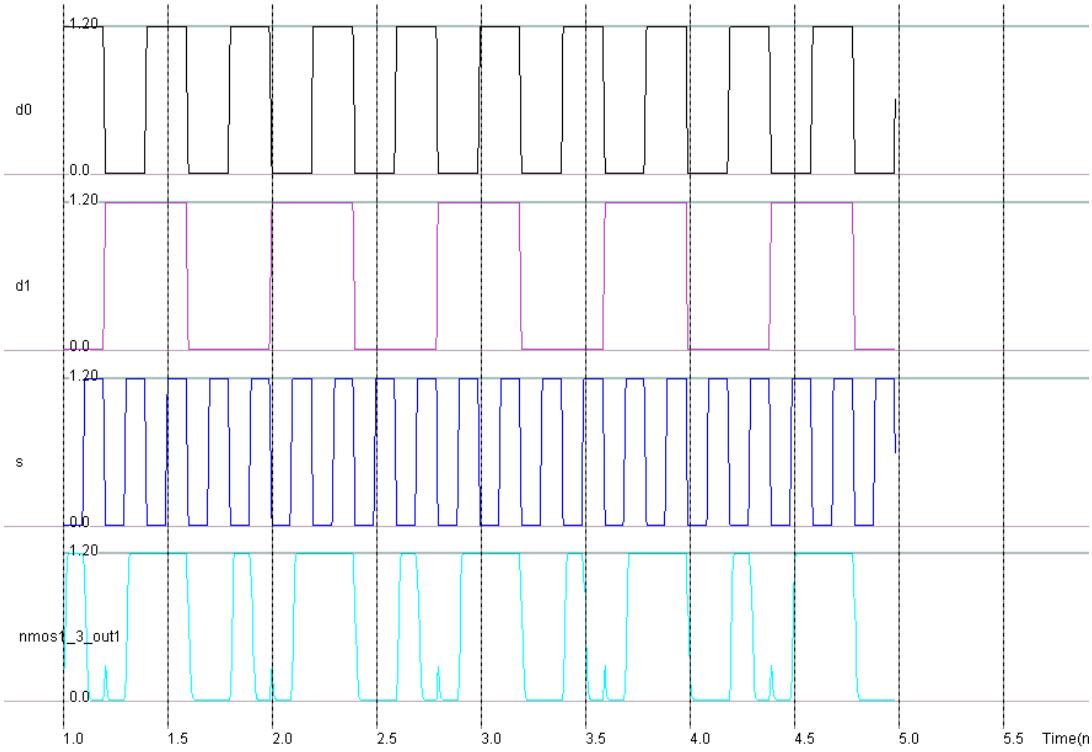
EXPERIMENT No.07

MUX 2:1:

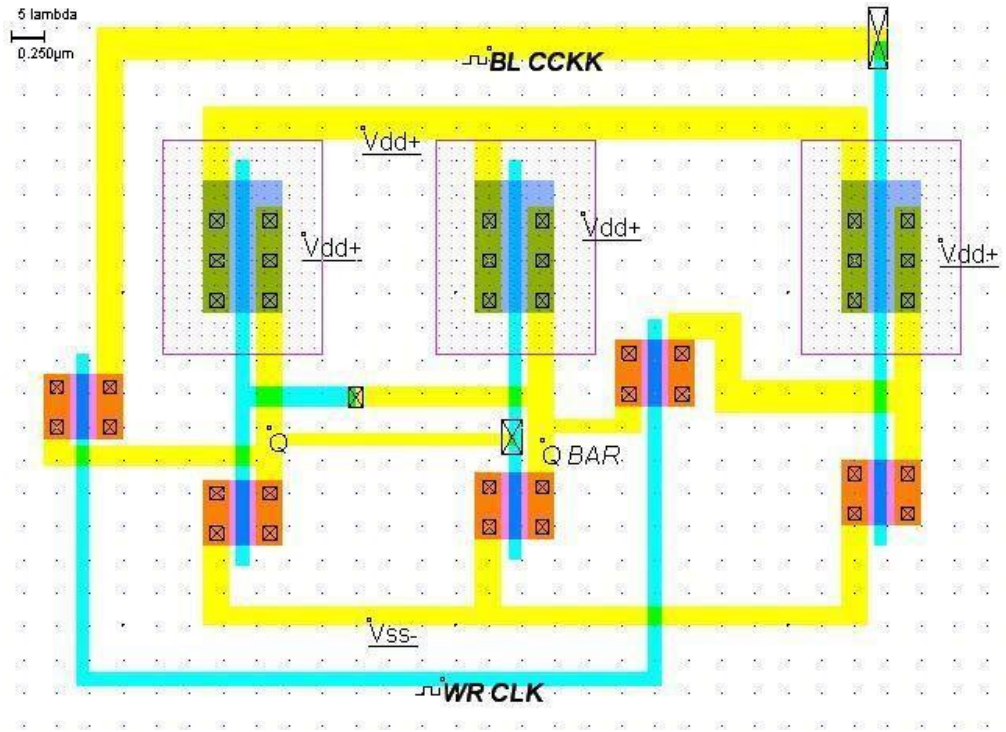


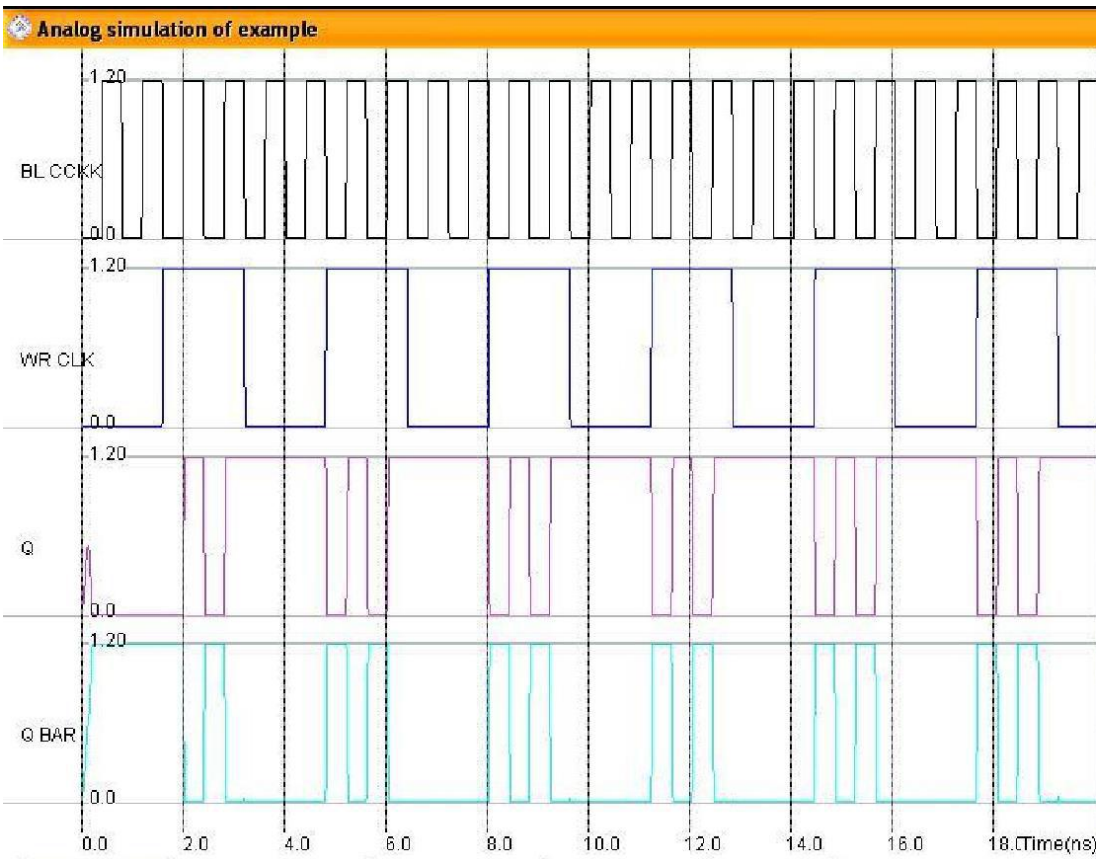



5 lambda
0.250µm
inv_1_w3
not1_2_w7
nmos1_3_out1
pmos1_4_(not1_5_w8
nmos1_6_out1
pmos1_7_out1
vdd+
vss-
s
out1
d0
d1


d0
d1
s
nmos1_3_out1
1.20
0.0
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
Time(n

EXPERIMENT No. 08





EXPERIMENT No. 09

D FLIP FLOP