Neeraj Prabhu

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EDUCATION

Indian Institute of Technology Bombay (IITB)   *[Nov 2020 - Present]*
Bachelors of Technology | Department of Electrical Engineering   GPA: 8.83/10
Pursuing a major in **Electrical Engineering** (with honors), and a minor degree in **Computer Science**

RESEARCH INTERESTS

Computer Architecture, Domain-Specific Accelerators, Digital Design, FPGA-Based System Architecture, VLSI Circuits, ASIC Design

RESEARCH EXPERIENCE

Accelerating Fully Homomorphic Encryption on UPMEM   *[May 2023 - Present]*
Utah Arch Group, University of Utah | Prof. Rajeev Balasubramonian

- Characterized FHE operations implemented in the **Microsoft SEAL** library using **Intel VTune** and **Perf**
- Generated **roofline plots** for multiple workloads using FHE operations and analyzed the memory-access instructions, compute instructions, and last-level cache accesses to identify that FHE is **memory-bound**
- Implemented addition, multiplication—including **key switching**, rescaling, **NTT** transforms—and rotation in the CKKS scheme on **UPMEM** by parallelizing them on several DPUs to improve performance
- Conducted extensive literature survey regarding FHE to understand optimization techniques used in state-of-the-art **FHE accelerators** and studied the architecture of **UPMEM PIM** to correlate the two

Analyzing and Improving Performance of Branch Target Buffers   *[July 2023 - Present]*
Computer Architecture and Dependable Systems Lab, IIT Bombay | Prof. Virendra Singh

- Analyzing the use of **STTRAM** for BTBs and the performance benefits with the faster read accesses
- Implemented **BTB-X** on **ChampSim** and compared its performance with a conventional BTB along with an analysis of BTB **MPKI**, **memory footprint**, branches stored, and power requirements
- Surveyed existing literature regarding different **BTB organizations** and ways to reduce the size of BTBs

FPGA-based experiment design for an NV Center Setup   *[Jan 2023 - Present]*
PQUEST, IIT Bombay | Prof. Kasturi Saha, Prof. Laxmeesha Somappa

Realtime Bayesian ODMR on Xilinx ZCU111

- Designing an FPGA-based **Bayesian inference** technique to reduce the time required for the completion of ODMR with **on-board estimation** of the intensity, and feedback to generate the excitation signal
- Implementing the algorithm consisting of a **random number generator**, a computation unit to update the weights of the sampling points, and a selection unit to minimize the number of samples required
- Integrated custom Verilog code with the **Zynq MPSoC** and **RFSoC IPs** to generate microwave signals

FPGA-based photon correlator

- Simulated a photon correlator on Xilinx Vivado using the **multi-tau correlation** technique to accommodate large experiment times while avoiding the use of a large number of correlation channels
- Designed and integrated an input sampler, **clock divider**, and an **accumulator** to form the correlator
- Obtained a **Poissonian distribution** of photon strikes with a timing resolution of approximately 200ps

Pangenome Graph Visualization on Hammerblade Manycore   *[Feb 2023 - Jul 2023]*
Computer Systems Laboratory, Cornell University | Prof. Zhiru Zhang

- Studied the flow of the **odgi pangenome graph visualization** algorithm to understand its functionality and its role in highlighting subtle differences in genomes of species in certain demographics
- Wrote the pangenome visualization code and programmed **kernels** to run the code on **Hammerblade**
- Implemented a faster version of the pangenome visualization code by using a **stochastic gradient descent** technique to draw the final graph and implemented the same on Hammerblade to analyze its performance

Awards And Accolades

- Acheived **All India Rank 207** in the JEE-Advanced Exam, out of over 0.15 million candidates *[2020]*
- Secured **All India Rank 691** in the JEE-Mains Examination, out of over 800 thousand candidates *[2020]*
- Qualified for **INChO** by securing a rank in the **top 802** in NSEC *[2020]*
- Selected for the prestigious **KVPY** (Kishore Vaigyanik Protsahan Yojana) fellowship *[2020]*
- Awarded a **Best Project Award** for our design of a fluxgate sensor & lock-in amplifier in EE 344 *[2023]*

Technical Projects

Slow Scan Television Transmitter *[Apr 2021 - Present]*
Student Satellite Program, IIT Bombay

- Performed extensive **component level** testing of the SSTV Module to ensure proper working of the EEPROM and waveform generator when interfaced with the ATmega32 microcontroller
- Implemented **SPI**, **I²C** and **UART** protocols to interface peripheral ICs with Atmega microcontrollers
- Designed and simulated a **Yagi-Uda** and a **Horn** antenna to analyze the S11 plots and radiation patterns

Implementation of Freeflow Core on GEM5 *[Sep 2023 - Present]*
Advanced Topics in Computer Architecture (EE748) | Prof. Virendra Singh

- Conducted extensive literature survey regarding techniques to optimize the performance of in-order cores by exploiting **memory level parallelism** while maintaining a low power budget
- Implemented an In-Order Core on GEM5 while using Out-of-Order features such as **register renaming**
- Implemented **multiple queues** before the dispatch stage to separate **memory access** and **address-generating** instructions which will be identified using a backward propagation algorithm

Lock-in Amplifier with flux-gate sensor *[Jan 2023 - Apr 2023]*
Electronics Design Lab (EE 344) | Prof. Siddharth Tallur, Prof. Kasturi Saha, Prof. Laxmeesha Somappa

- Designed a flux-gate sensor from scratch using **in-house components**, which included the design of a printed circuit board (PCB) and optimization of **coil parameters**, all in a ready-to-go package
- Studied the principles of **lock-in detection** and programmed a **Red-Pitaya** board to serve as a lock-in amplifier which takes 2 input signals and uses one of them as reference for the lock-in detection
- Integrated the lock-in amplifier with the flux-gate magnetometer to facilitate **real-time sensing** of DC magnetic fields and display the results on a PC connected to the Red-Pitaya Board

Pipelined Microprocessor Design *[Jan 2022 - Apr 2022]*
Microprocessors (EE 309) | Prof. Virendra Singh

- Designed a **6-stage pipelined**, 16-bit microprocessor to implement a 17 instruction **RISC** architecture
- Modelled components such as the **ALUs**, **register banks** and **memory**, and integrate them onto the datapath along with the necessary hardware to accomodate instructions in all stages of the pipeline
- Mapped out a suitable datapath and delineated hardware flowcharts for each of the instructions and designed a **control status word** and a **finite state machine** to implement the same
- Optimized the architecture by using **hazard detection blocks** and **stall reduction** techniques

Superscalar Microprocessor Design *[Aug 2022 - Nov 2022]*
Advanced Computer Architecture (CS 683) | Prof. Virendra Singh

- Extended the pipelined architecture to design a **2-way fetch Out-Of-Order** superscalar microprocessor
- Implemented a **128-entry reservation station** to control the issuing of instructions out-of-order and a 256-entry reorder buffer to retire the instructions in order once execution of each is complete
- Designed a **physical register file** to support register renaming to handle various dependencies
- Developed a **2-bit branch predictor** and hardware to **resolve incorrect branches** after execution

Analyzing Decoupled L1 Caches in GPGPUs *[Jun 2022 - Aug 2022]*
Computer Architecture and Dependable Systems Lab, IIT Bombay | Prof. Virendra Singh

- Conducted extensive literature survey regarding analyzing and leveraging **decoupled L1 caches** in different configurations and implemented the decoupled L1 cache model on GPGPU Sim
- Studied the **SIMT 3 loop approximations** of GPGPU Architecture and the GPU memory interfaces
- Simulated multiple operations on GPGPU-Sim and analysed the **benchmark** outputs

Accelerating VLSI CAD Algorithms [Jan 2023 - Apr 2023]
Parallel Scientific Computing and Visualization (AE6102) | Prof. Prabhu Ramachandran

- Improved the performance of **graph algorithms** used in VLSI circuit design and analyzed the results, comparing the time for multiple graph sizes against Python libraries such as **pyEDA** and **NetworkX**
- Achieved a performance benefit of the order of **100x** for large graphs using **numba accelerated** versions of graph algorithms (shortest path, minimum spanning tree) over the networkx implementation
- Implemented **logic simulators** and accelerated the simulation of circuits by **two orders** of magnitude
- Automated the generation of results for multiple graph sizes and edge weights using the **Automan** library

Wavelet transforms for image super-resolution and restoration [Aug 2022 - Nov 2022]
Image Processing (EE610) | Prof. Amit Sethi

- Achieved a binary cross entropy loss of **0.238** and an accuracy of **0.865** by implementing a UNet for **semantic segmentation** of multi-organ tissue images included in the MoNuSeg challenge
- Modified the UNet architecture with various **convolution layers** in order to increase performance
- Performed **image denoising** using neighboring wavelet coefficients and thresholding and reported PSNR
- Employed techniques like **Wiener filtering**, histogram manipulation, and SVR for image restoration

Text to Image Synthesis with Stacked GANs [Jun 2022 - Aug 2022]
Introduction to Machine Learning (DS303) | Prof. Biplab Bannerjee

- Modelled **generator** and **discriminator** blocks consisting of multiple **convolutional layers**
- Conducted literature survey to understand **GANs** and their usage with embedding compressors
- Developed a **2 stage GAN model** to generate bird images from their text description

View other projects on my website [link]

POSITIONS OF RESPONSIBILITY

System Engineer | Student Satellite Program, IIT Bombay [Oct 2022 - Sep 2023]
A 50+ member student team with the vision of making IIT Bombay a centre of excellence in space technology, working on developing various CubeSat-compatible modules and an automated ground station

- Part of the leadership group of a multi-disciplinary team of **50+ students** across 4 projects with **INR 2.8M** annual budget and assigned the responsibility of managing the **ham radio club** of the institute
- Restructured the team's **leadership structure** and adopted a technical approach emphasising iterative **hardware prototyping and testing**, resulting in increased efficiency and faster project completion
- Ensuring implementation of **QA practices** & team's version control guidelines for better organisation
- Conducted a day-long workshop to help 80+ participants from various institutes setup their ground stations

Department Academic Mentor (DAMP Mentor) [May 2023 - Present]
DAMP Cabinet, Student Mentorship Programme, IIT Bombay

- Selected into a team of **46 members** out of **100+ prospects** on the basis of **rigorous interviews** to help **6 sophomores** strike a balance between academics and extracurricular activities
- Selected as a senior DAMP Mentor to help academically weaker students improve their academic standing
- Actively participated in compiling **reviews of projects and courses** undertaken by the students

Teaching Assistant [Jan 2023 - May 2023]
EE 309: Microprocessors | Prof. Virendra Singh

- Entrusted with the responsibility of being a teaching assistant for the sophomore year course EE 309
- Conducted sessions for **50+ students** to recap the course contents and attend to doubts
- Helped out in **invigilation** duties for the day-long end-semester examination which consisted of 2 parts

TECHNICAL SKILLS

Programming Languages	C++, Verilog, VHDL, Embedded C, Python, MATLAB
Libraries	Numba, MPI4PY, Automan, Mayavi, SciPy, Pynq, NumPy, Pandas, Scikit-learn, Tensorflow, OpenCV, PyRPL
Software	GEM5, ChampSim, GPGPU-Sim, Vivado, Vitis, Intel Pin, Intel VTune, Perf, Ansys HFSS, EAGLE, NGspice, GNU-Radio

Key Courses Undertaken

Computer Architecture	Advanced Topics in Computer Architecture, Advanced Computer Architecture, Microprocessors§
Digital Design & VLSI	VLSI Design, Algorithmic Design of Digital Systems, Foundation of VLSI CAD, Embedded Systems, Digital Systems§
Machine Learning	Image Processing, Programming for Data Science, Intro to Machine Learning
Electrical Engineering	Electronic Design Lab, Analog Circuits§, Electronic Devices§, Signal Processing, Communication Systems§, Electromagnetic Waves, Markov Chains and Queuing Systems, Control Systems§, Power Engineering§
Computer Science	Principles of Data and System Security, Parallel Scientific Computing and Visualization, Data Structures and Algorithms, Design and Analysis of Algorithms

§*along with a lab component*

Extra-Curricular Activities

- Completed **80+ hours** of volunteering service in the **Green Campus** department of **NSS, IIT Bombay**
- Satellite Tracking
  - Tracked the **ISS** and received **SSTV** images during the **ARISS event** using a Yagi Antenna
  - Tracked the **NOAA** Satellites and received **weather images** using an in-house Egg-Beater Antenna
- Conducted an online session to help high school students prepare for the Joint Entrance Examination
- Secured **1st place** in the **National Round** of the **Microsoft Office Specialist Championship**
- Placed **First** in the School Science Fair for generating alternating current from wave energy
- Participated in the **Indian International Model United Nations** and the **Billabong High Model United Nations**, receiving the **High Commendation** award in the latter

References

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