

# NEGAR NEDA

School of Electrical & Computer Engineering, University of Tehran, 16th Azar St, Enghelab Sq., Tehran, Iran

📞(+98)9155353543 📩 ne.neda74@gmail.com 💻 negarnd.github.io 💬 negarnd

## EDUCATION

- **University of Tehran (UT), Tehran, Iran** Sep. 2018 - present  
M.Sc. in Computer Architecture  
Cumulative GPA: **17.26/20 (3.63/4)**  
Thesis: FPGA-based Multi-precision Accelerator for Deep Neural Networks
- **Amirkabir University of Technology (AUT), Tehran, Iran** Sep. 2014 - Sep. 2018  
B.Sc. in Computer Engineering, Computer Architecture Systems  
GPA (last two years): **17.91/20 (3.79/4)**  
Cumulative GPA: **17.2/20 (3.62/4)**  
Thesis: Implementation of a Tracking System Using LoRaWAN Protocol
- **National Organization for Development of Exceptional Talents (NODET), Birjand, Iran** Sep. 2010 - Jun 2014  
Diploma, Mathematics and Physics  
Cumulative GPA: **19.68/20**

## RESEARCH INTERESTS

- Hardware Accelerators
- FPGA
- Reconfigurable Computing
- Deep Neural Networks
- Approximate Computing
- Data/Computation Reuse

## RESEARCH EXPERIENCES

- **Research Assistant in Network on Chip Laboratory**, University of Tehran 2018 - present  
Supervised by **Dr. Mehdi Modarressi**

In this laboratory, I have been working on implementing an FPGA based Multi-precision Accelerator for Deep Neural Networks. This architecture is able to change the working bit-width dynamically according to the minimum bit-width required to preserve the original accuracy. I have designed a fusible LUT-based multiplier that uses approximation to reduce the cost of activation/weight products.

- **Researcher in IoT Lab**, Amirkabir University of Technology 2018  
Supervised by **Dr. Mehdi Rasti**

In this laboratory, I worked on designing a portable Tracking System using ADXL335, NEO-6m and LoRaWAN protocol as my B.Sc thesis.

- **Researcher in Digital System Design Lab**, Amirkabir University of Technology 2017 - 2018  
Supervised by **Dr.Mahmoud Momtazpour** and **Dr.Morteza Sahebzamani**

In this laboratory, we worked on the Amirkabir University of Technology IoT Gateway Project.

## PUBLICATIONS

- N. Neda**, S. Ullah, A. Ghanbari, A. Kumar, M. Modarressi and H. Mahdiani, "MpDNN: Multi-Precision Deep Neural Network Acceleration on FPGAs", In preparation, University of Tehran, Iran & Dresden University of Technology, Germany. ↗

## TEACHING EXPERIENCES

- **Computer-Aided Digital**, T.A. ( Dr. Mehdi Modarressi) 2019 & 2020
- **Logic Circuit Laboratory**, Lab Instructor 2018
- **Computer Networks**, T.A. ( Dr. Siavash Khorsandi) 2017
- **Digital Design Automation**, T.A. ( Dr. Morteza Sahebzamani) 2017
- **Electrical Circuit1**, T.A. ( Dr. Siavash Khorsandi) 2016
- **Logic Circuits**, T.A. ( Dr. Mehdi Sedighi & Dr. Mahmoud Momtazpour) 2016

## HONOR & AWARDS

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Ranked Top 3 in term of GPA, among Computer Architecture Students in AUT	2019
Eligible to study in two fields simultaneously	2015
Ranked top 0.6% out of 222,500, Nationwide University Entrance Exam, Mathematics (1304 among 222,500 Participants)	2014

## NOTABLE PROJECTS

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- Accelerating CNN inference by OpenMP & CUDA, (MultiCore Embedded Systems)  2020
- Implementing an Approximate Multiplier, by limiting carry propagation for fast partial product accumulation (Computer Arithmetics) 2020
- Forecasting the number of taxi requests by RNN, (Deep Neural Networks)  2019
- Image Template Matching with CUDA, Implemented the Template Matching algorithm in CUDA & OpenMP, on a dataset of coin/face images. (Multi-Core Programming Course) 2018
- Temperature controller, using Wi-Fi development board (WEMOS D1) and LM35 to measure the room temperature and transfer to Android-Smartphone, (Computer Interface Design) 2018
- Implementing various projects on FRDM-KL25Z board, (Embedded Systems)  2018
- Implementing a home environment controller, Co-design of a system including lighting control, temperature control and voice recognition using Xilinx MicroBlaze Soft Processor Core 2017
- Implementing a 16\*4 SRAM, and 2:4 address decoder using HSpice (Digital Electronics)  2016
- Implementing an Engineering Calculator, using CORDIC IP Core  2016
- Implementing a Basic ALU, Cache, and RAM, by VHDL (Computer Architecture)  2016
- Implementing Robo Kill game, using JAVA (Advanced Programming) 2015

## ONLINE COURSES

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- "Convolutional Neural Networks" [Certificate](#) - Offered by deeplearning.ai 2020
- "Neural Networks and Deep Learning" [Certificate](#) - Offered by deeplearning.ai
- "Improving Deep Neural Networks: Hyperparameter tuning, Regularization, and Optimization" [Certificate](#) - Offered by deeplearning.ai - Coursera 2019

## ATTENDED WORKSHOPS

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- Third IPM<sup>1</sup> Advanced School on Computing, Computer Architecture 2019
- 8th IPM-HPC Workshop on Multi-core Systems and Parallel Platforms 2019
- Introduction to FPGA Workshop, Co-design and hardware implementation, held in AUT 2016

## TECHNICAL SKILLS

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- **Programming:** Python(Keras, Tensorflow, PyTorch), C/C++, Java, VHDL, Verilog, Co-Design, CUDA, OpenMP, Assembly
- **Frameworks & Scientific Tools:** Visual Studio, Qt, MATLAB, Jupyter Notebook, Arduino IDE, Git
- **Typesetting Tools:** L<sup>A</sup>T<sub>E</sub>X, Microsoft office
- **Hardware CAD Tools:** Vivado Design Suite, Xilinx ISE Design Suite, PSPICE, HSPICE, Modelsim, Proteus, Keil
- **Operating Systems:** Microsoft Windows, Linux
- **Language:** English (IELTS Overal Score: 7.5), Persian (Native)

<sup>1</sup>Institute for Research in Fundamental Sciences