

Design & Verification of a Dual-port Memory as an APB subordinate (slave)

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1 Introduction

The purpose of this project is to build a reusable verification environment based on the SystemVerilog (SV) Object-Oriented Programming (OOP) methodology.

2 Design Specs for the Dual-port Memory

2.1 Read Operation

2.2 Write Operation

3 Verification Specs for the Dual-port Memory with an APB interface

3.1 Test-plan

3.2 OOP Components

3.2.1 Transaction

3.2.2 Generator

3.2.3 Driver

3.2.4 Monitor

3.2.5 Scoreboard

3.2.6 Enviromnent