

EE 5323 Homework #1: Ring Oscillator Schematic Design

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Setting Up Cadence

- Created a working directory in home folder (/home/class/sawan050) using mkdir command: `mkdir asap7_rundir`
- Going to the working directory: `cd ~/asap7_rundir`
- Setting the environment variable PDK_DIR using the following command, so that it points to the ASAP 7nm PDK directory:
`setenv PDK_DIR /home/class/ee5323ta/ASAP7_PDKandLIB_v1p6/asap7PDK_r1p6`
- Sourcing the PDK configuration file to copy all necessary files in the run directory to copy all necessary files to the working directory
`source $PDK_DIR/cdslib/setup/config_asap7.csh`
- Running Cadence virtuoso using
`source setup.csh`

Creating Library as ring_lib

- From the virtuoso CIW box, File -> New -> Library -> ring_lib
- Selecting the “Attach to an existing technology library” option, click OK.
- Now, in the pop-up window, selecting asap7_TechLib library and click OK. Created library “ring_lib” as “/home/class/sawan050/asap7_rundir/ring_lib”
- Create a new cell From the Virtuoso CIW, File -> New -> Cellview -> with cell name inverter4

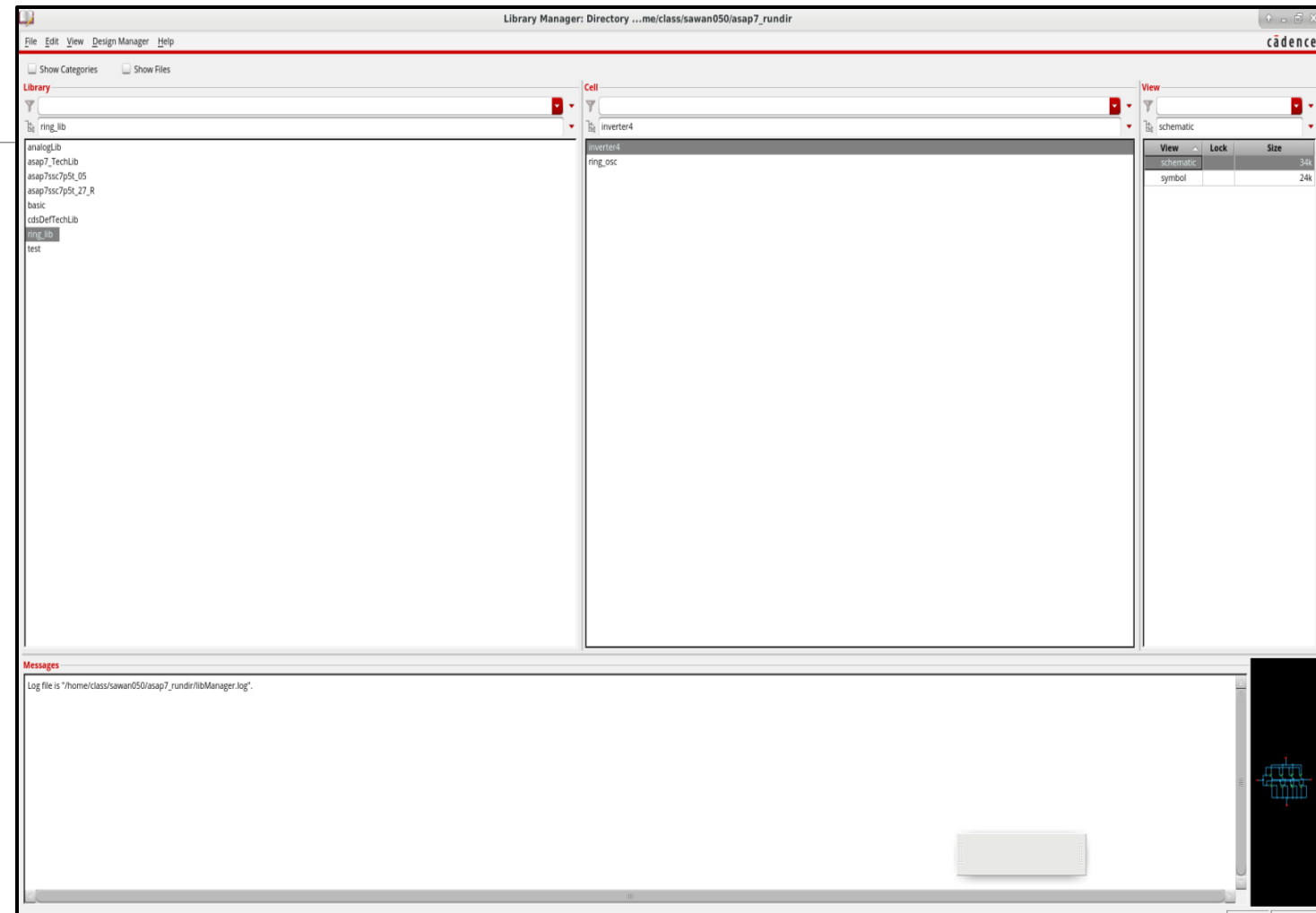


Fig 1: Creating Library ring_lib and cell name as inverter4

Creating Inverter4 Schematic in ring_lib

- Using asap7_TechLib library to browser for nmos_rvt and pmos_rvt, symbol view.
 - No of fin = 3
 - Fin width = 27nm.
 - Length = 20nm
 - Transistor width = 81nm
- And respective pins and wires to complete the circuit
- Here A is input pin , Y is output pin, VDD ,VSS are power and ground respectively
- Output is taken from drain terminal of mosfets.

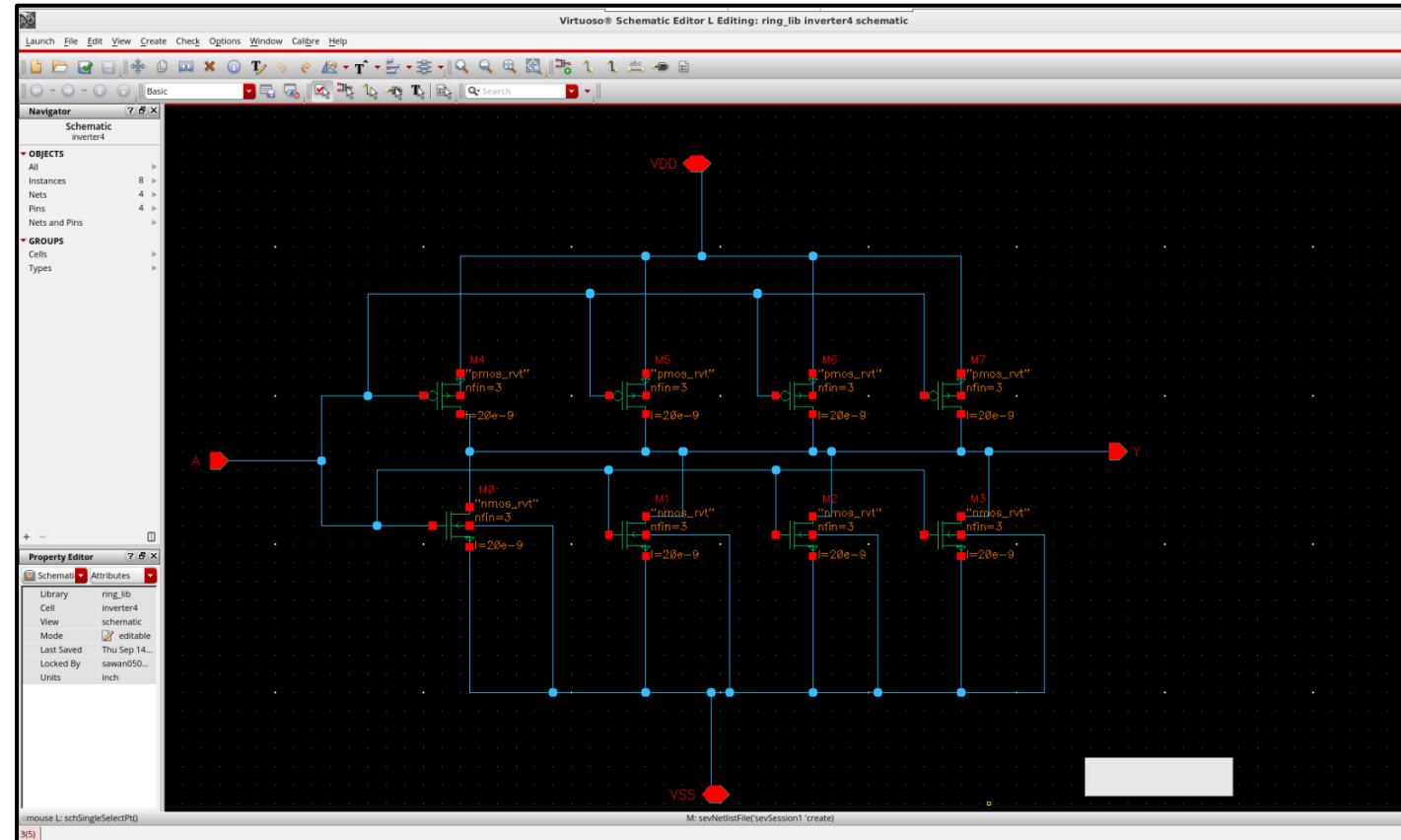


Fig 2: Creating schematic in Library ring_lib for inverter4

Setting up ADL , Creating Netlist , Waveforms in Cosmoscope

- Setting up Simulator and the environment in ADL to Hspice .
- Creating netlist for inverter4 to run in cosmoscope.
- The image shows output Y is in the inverted form from input signal A.

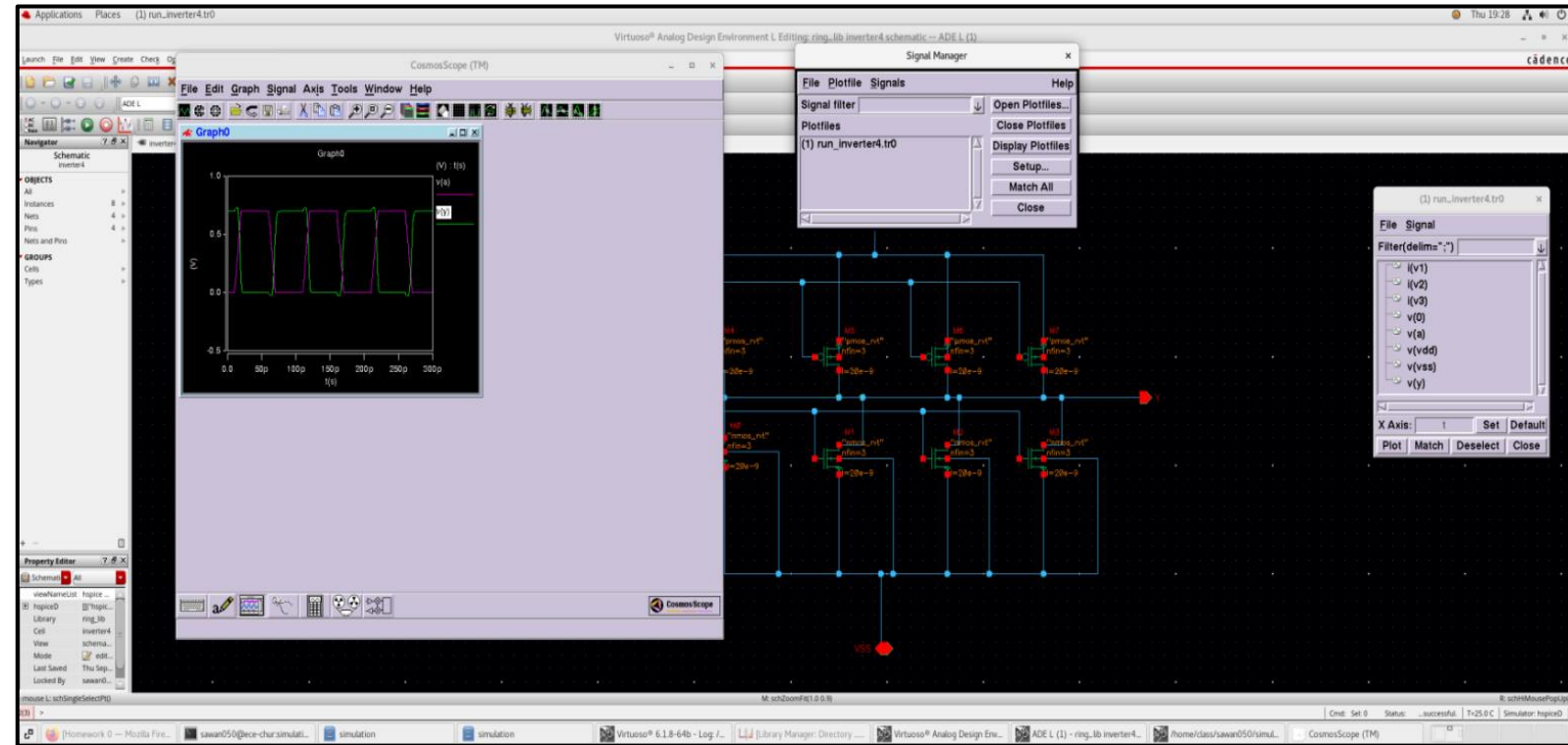


Fig 3: Creating waveforms in cosmoscope for inverter4

Creating a new symbol

- Saving the schematic before creating its symbol: File->Check and Save
- Create->Cellview->From Cellview, click OK.
- From View Name should be schematic and To View Name should be symbol.
- Tool /Data Type should be set to schematicSymbol. Click on OK.
- This symbol of inverter4 to be used in creating schematic of ring oscillator

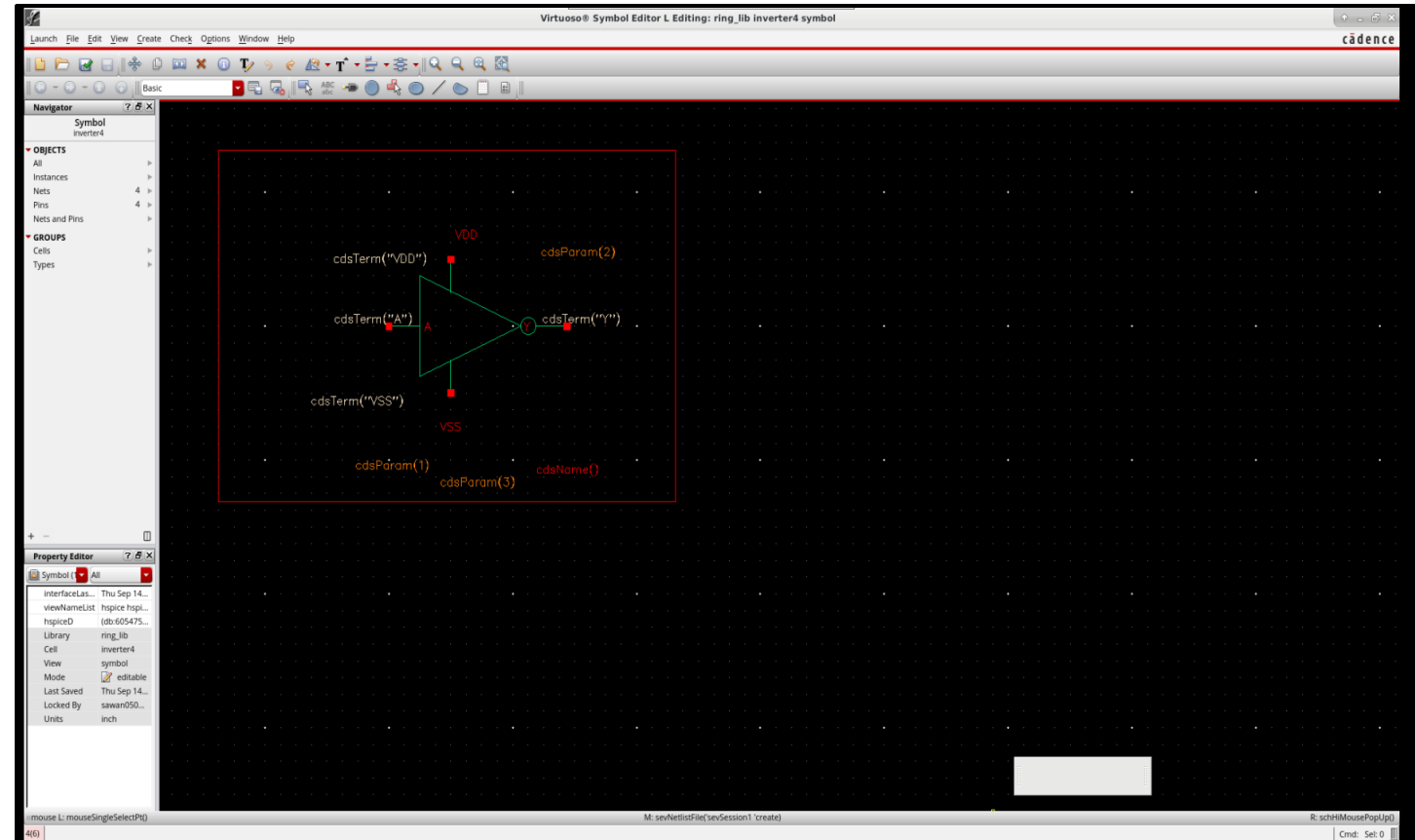


Fig 4: Creating symbol in Library ring_lib for inverter4

Creating cell name ring_osc for 99 stage ring oscillator schematic

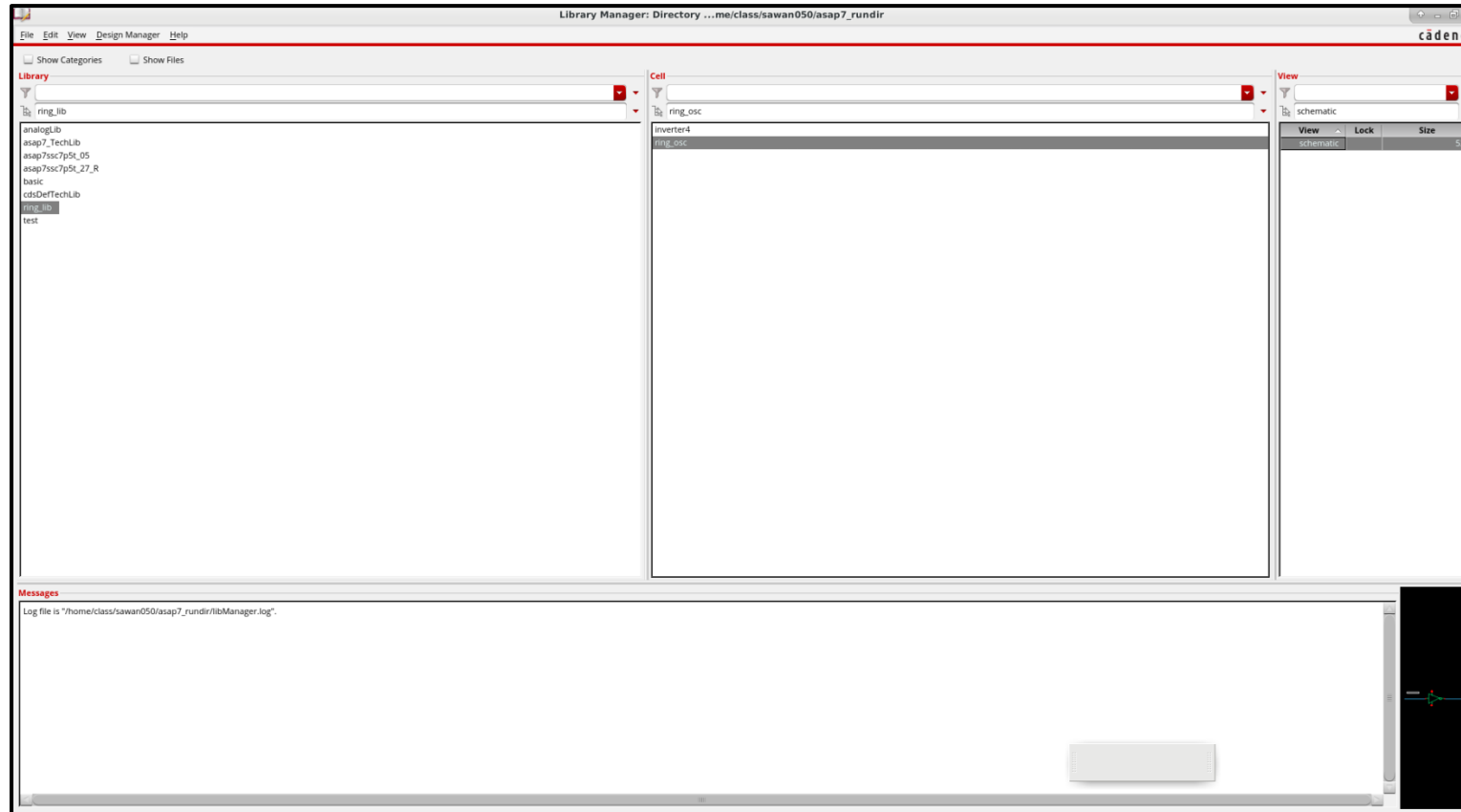


Fig 5: Creating in Library ring_lib , cell name as ring_osc

Using the inverter4 symbol created earlier in ring_lib to use in ring_osc schematic

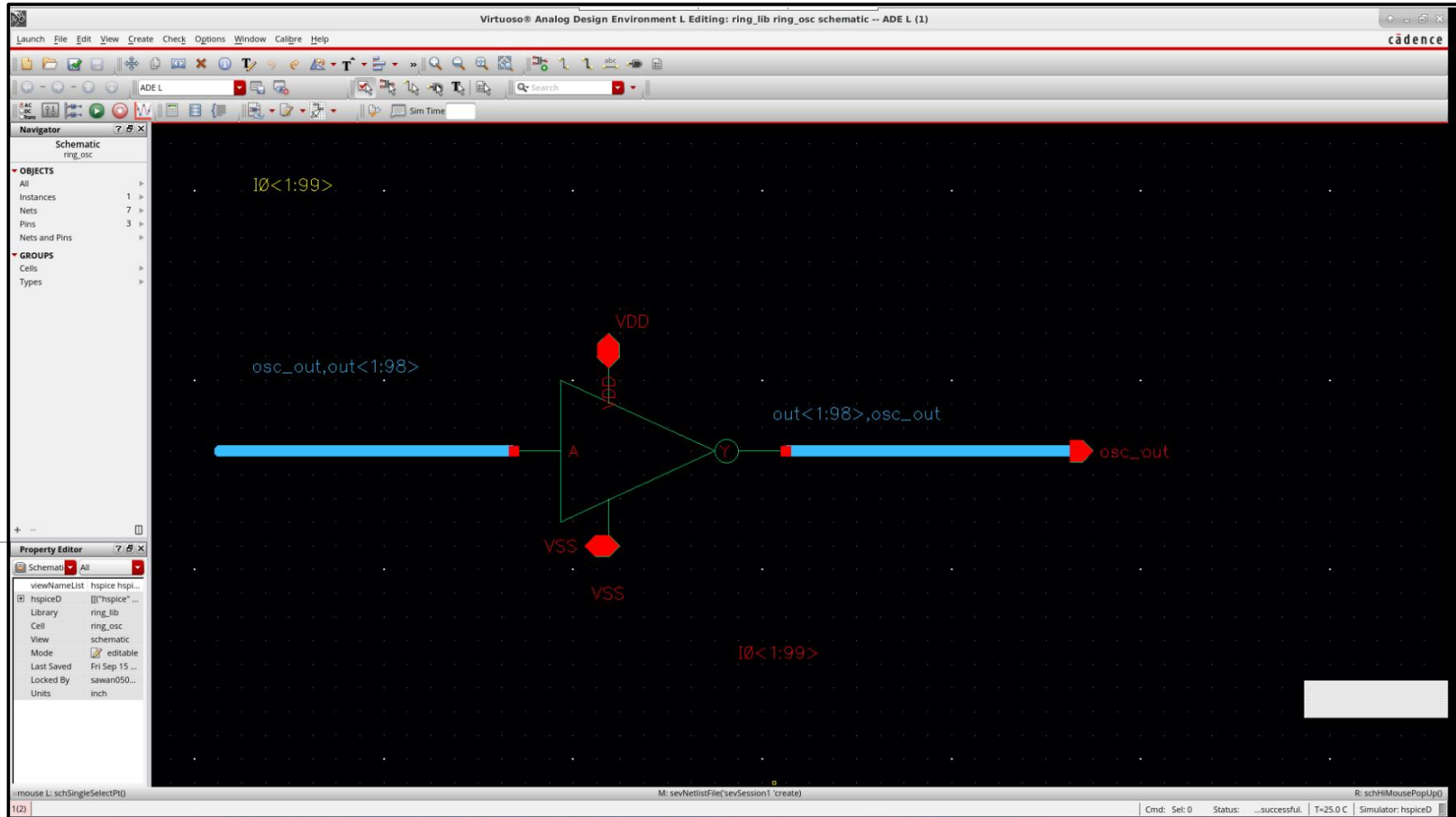


Fig 6: Creating in Library ring_lib schematic for 99 stage ring oscillator

Setting ADL for ring oscillator

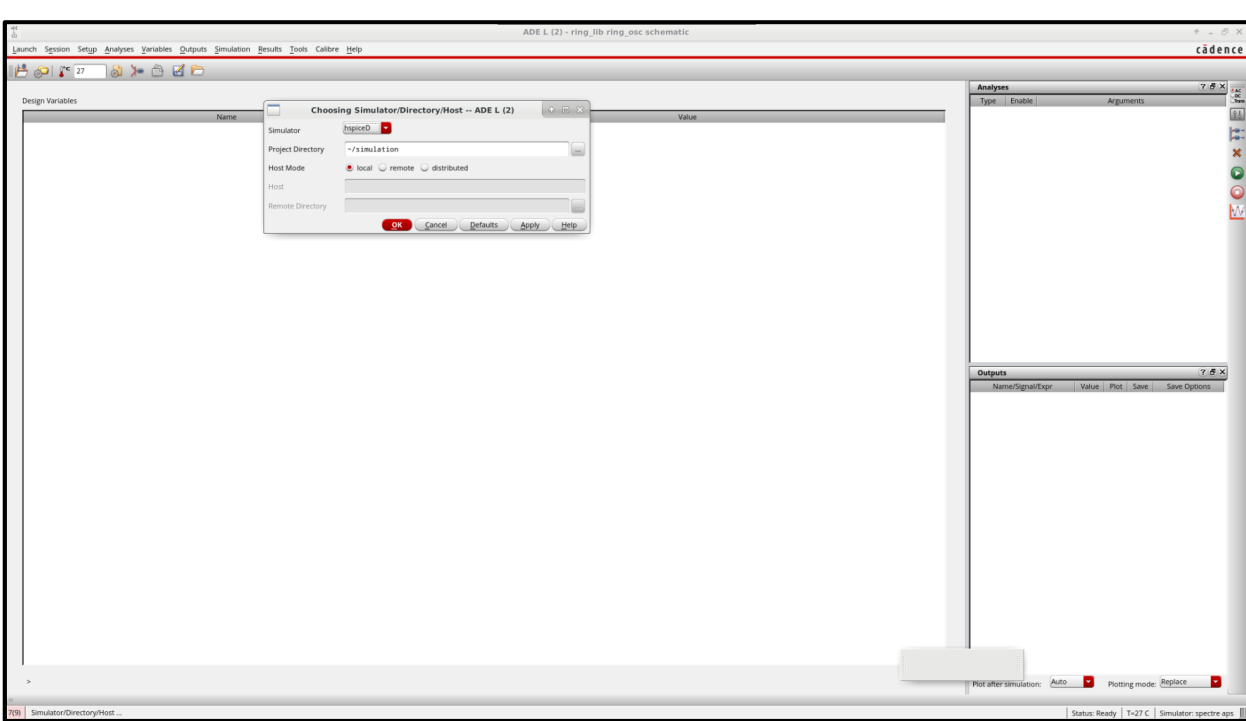


Fig 7: Setting up simulation folder in ADL

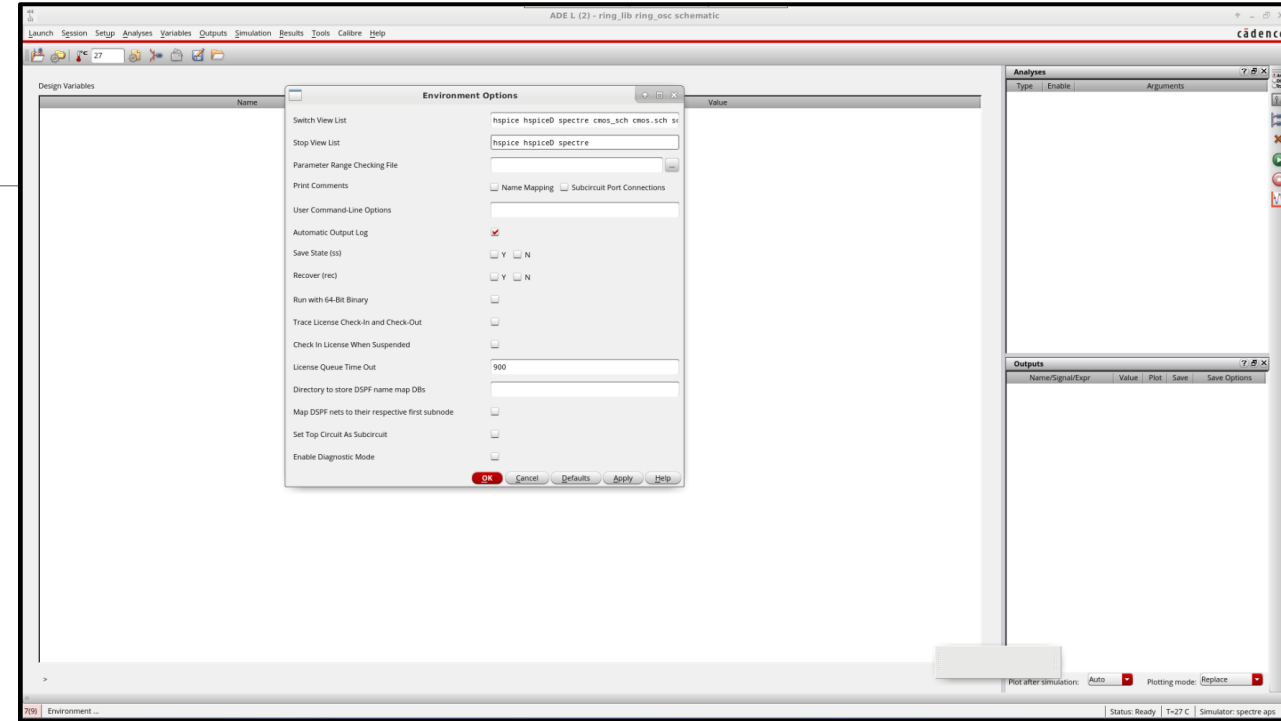


Fig 8: Setting up environment in ADL for simulation

Creating Netlist for Ring Oscillator

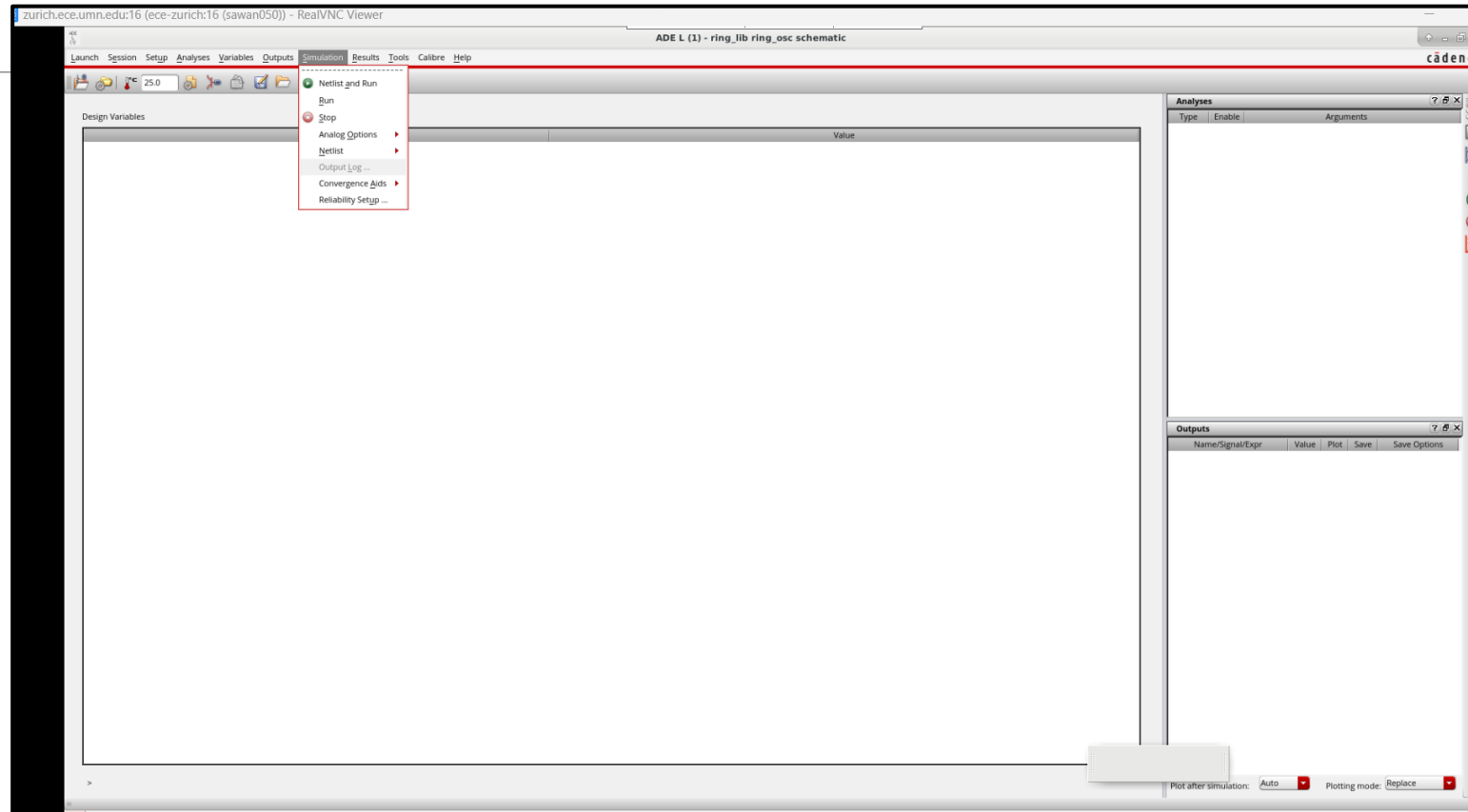


Fig 9: Creating netlist for 99-stage ring oscillator

Netlist generated for ring oscillator as input.ckt file in default simulation folder

```

/home/class/sawan050/simulation/ring_oschpice0/schematicnetlistinput.ckt
File Edit View Help
cadence

** Generated for: ngspice0
** Generated on: Sep 16 17:28:43 2023
** Design library name: ring.lib
** Design cell name: ring_osc
** Design view name: schematic

.TEMP 25.0
* OPTION
* ARTIST=2
* INGOLD=2
* PARTICE=LOCAL
* PSF=2

** Library name: ring.lib
** Cell name: invert4
** View name: schematic
subckt invert4 a vdd vss y
nm0 y a vss nm0s_rvt w=0e-9 l=20e-9 nfin=3
nm2 y a vss nm0s_rvt w=0e-9 l=20e-9 nfin=3
nm1 y a vss nm0s_rvt w=0e-9 l=20e-9 nfin=3
nm3 y a vss nm0s_rvt w=0e-9 l=20e-9 nfin=3
nm4 y a vdd vdd pmos_rvt w=0e-9 l=20e-9 nfin=3
nm6 y a vdd vdd pmos_rvt w=0e-9 l=20e-9 nfin=3
nm5 y a vdd vdd pmos_rvt w=0e-9 l=20e-9 nfin=3
nm7 y a vdd vdd pmos_rvt w=0e-9 l=20e-9 nfin=3
ends invert4
** End of subcircuit definition.

** Library name: ring.lib
** Cell name: ring_osc
** View name: schematic
v100> osc out vdd vss out<0> invert4
v100> out<0> vdd vss out<2> invert4
v100> out<2> vdd vss out<3> invert4
v100> out<3> vdd vss out<4> invert4
v100> out<4> vdd vss out<5> invert4
v100> out<5> vdd vss out<6> invert4
v100> out<6> vdd vss out<7> invert4
v100> out<7> vdd vss out<8> invert4
v100> out<8> vdd vss out<9> invert4
v100> out<9> vdd vss out<10> invert4
v100> out<10> vdd vss out<11> invert4
v100> out<11> vdd vss out<12> invert4
v100> out<12> vdd vss out<13> invert4
v100> out<13> vdd vss out<14> invert4
v100> out<14> vdd vss out<15> invert4
v100> out<15> vdd vss out<16> invert4
v100> out<16> vdd vss out<17> invert4
v100> out<17> vdd vss out<18> invert4
v100> out<18> vdd vss out<19> invert4
v100> out<19> vdd vss out<20> invert4
v100> out<20> vdd vss out<21> invert4
v100> out<21> vdd vss out<22> invert4
v100> out<22> vdd vss out<23> invert4
v100> out<23> vdd vss out<24> invert4
v100> out<24> vdd vss out<25> invert4
v100> out<25> vdd vss out<26> invert4
v100> out<26> vdd vss out<27> invert4
v100> out<27> vdd vss out<28> invert4
v100> out<28> vdd vss out<29> invert4
v100> out<29> vdd vss out<30> invert4
v100> out<30> vdd vss out<31> invert4
v100> out<31> vdd vss out<32> invert4
v100> out<32> vdd vss out<33> invert4
v100> out<33> vdd vss out<34> invert4
v100> out<34> vdd vss out<35> invert4
v100> out<35> vdd vss out<36> invert4
v100> out<36> vdd vss out<37> invert4
v100> out<37> vdd vss out<38> invert4
v100> out<38> vdd vss out<39> invert4

```

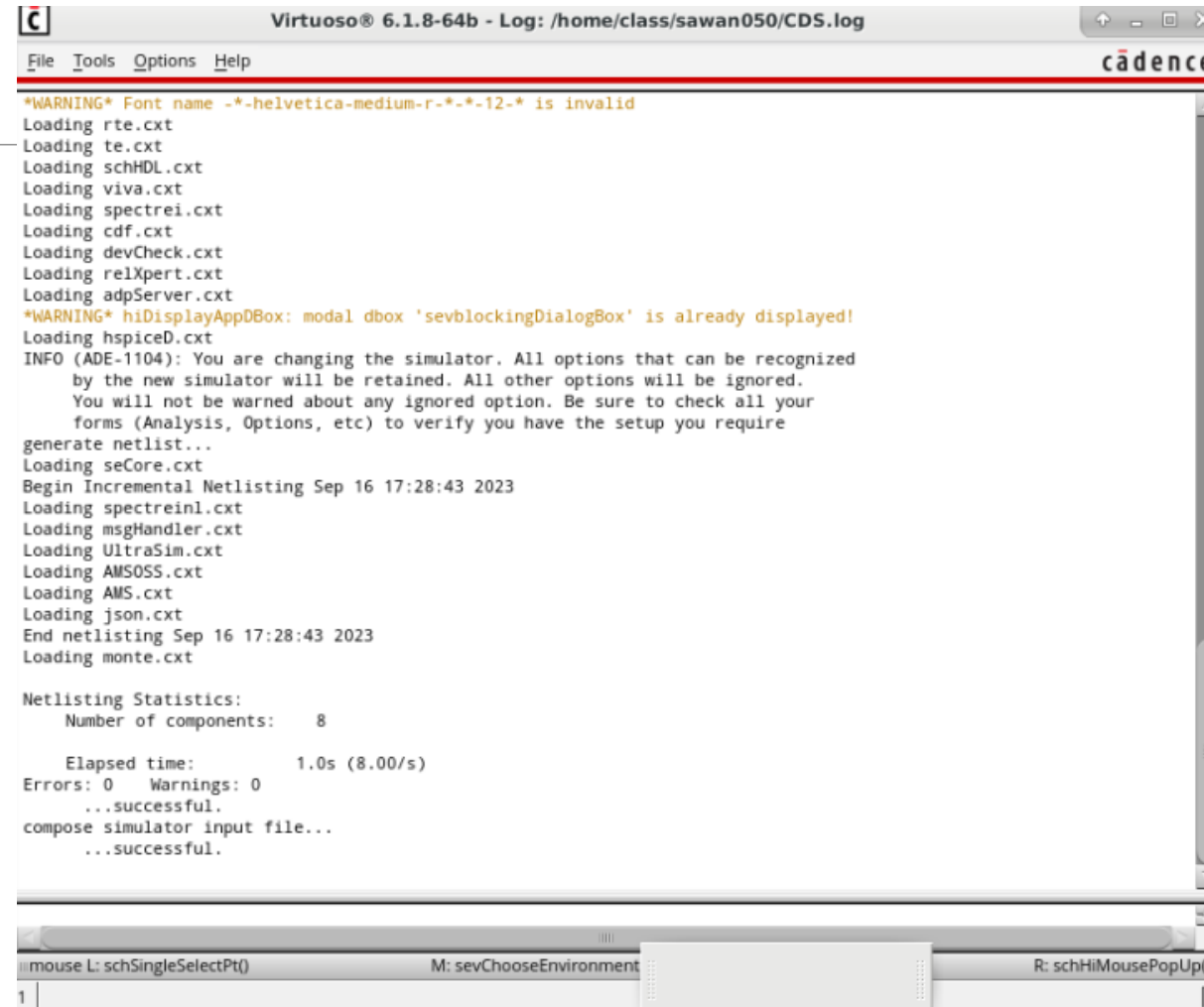
Fig 10: Netlist for ring oscillator before editing

```
File Edit View Help
/home/class/sawan050/simulation/ring_osc/hspiceD/schematic/netlist/input.ckt
cadence

xio<31> out<30> vdd vss out<31> inverter4
xio<32> out<31> vdd vss out<32> inverter4
xio<33> out<32> vdd vss out<33> inverter4
xio<34> out<33> vdd vss out<34> inverter4
xio<35> out<34> vdd vss out<35> inverter4
xio<36> out<35> vdd vss out<36> inverter4
xio<37> out<36> vdd vss out<37> inverter4
xio<38> out<37> vdd vss out<38> inverter4
xio<39> out<38> vdd vss out<39> inverter4
xio<40> out<39> vdd vss out<40> inverter4
xio<41> out<40> vdd vss out<41> inverter4
xio<42> out<41> vdd vss out<42> inverter4
xio<43> out<42> vdd vss out<43> inverter4
xio<44> out<43> vdd vss out<44> inverter4
xio<45> out<44> vdd vss out<45> inverter4
xio<46> out<45> vdd vss out<46> inverter4
xio<47> out<46> vdd vss out<47> inverter4
xio<48> out<47> vdd vss out<48> inverter4
xio<49> out<48> vdd vss out<49> inverter4
xio<50> out<49> vdd vss out<50> inverter4
xio<51> out<50> vdd vss out<51> inverter4
xio<52> out<51> vdd vss out<52> inverter4
xio<53> out<52> vdd vss out<53> inverter4
xio<54> out<53> vdd vss out<54> inverter4
xio<55> out<54> vdd vss out<55> inverter4
xio<56> out<55> vdd vss out<56> inverter4
xio<57> out<56> vdd vss out<57> inverter4
xio<58> out<57> vdd vss out<58> inverter4
xio<59> out<58> vdd vss out<59> inverter4
xio<60> out<59> vdd vss out<60> inverter4
xio<61> out<60> vdd vss out<61> inverter4
xio<62> out<61> vdd vss out<62> inverter4
xio<63> out<62> vdd vss out<63> inverter4
xio<64> out<63> vdd vss out<64> inverter4
xio<65> out<64> vdd vss out<65> inverter4
xio<66> out<65> vdd vss out<66> inverter4
xio<67> out<66> vdd vss out<67> inverter4
xio<68> out<67> vdd vss out<68> inverter4
xio<69> out<68> vdd vss out<69> inverter4
xio<70> out<69> vdd vss out<70> inverter4
xio<71> out<70> vdd vss out<71> inverter4
xio<72> out<71> vdd vss out<72> inverter4
xio<73> out<72> vdd vss out<73> inverter4
xio<74> out<73> vdd vss out<74> inverter4
xio<75> out<74> vdd vss out<75> inverter4
xio<76> out<75> vdd vss out<76> inverter4
xio<77> out<76> vdd vss out<77> inverter4
xio<78> out<77> vdd vss out<78> inverter4
xio<79> out<78> vdd vss out<79> inverter4
xio<80> out<79> vdd vss out<80> inverter4
xio<81> out<80> vdd vss out<81> inverter4
xio<82> out<81> vdd vss out<82> inverter4
xio<83> out<82> vdd vss out<83> inverter4
xio<84> out<83> vdd vss out<84> inverter4
xio<85> out<84> vdd vss out<85> inverter4
xio<86> out<85> vdd vss out<86> inverter4
xio<87> out<86> vdd vss out<87> inverter4
xio<88> out<87> vdd vss out<88> inverter4
xio<89> out<88> vdd vss out<89> inverter4
xio<90> out<89> vdd vss out<90> inverter4
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xio<92> out<91> vdd vss out<92> inverter4
xio<93> out<92> vdd vss out<93> inverter4
xio<94> out<93> vdd vss out<94> inverter4
xio<95> out<94> vdd vss out<95> inverter4
xio<96> out<95> vdd vss out<96> inverter4
xio<97> out<96> vdd vss out<97> inverter4
xio<98> out<97> vdd vss osc out<98> inverter4
xio<99> out<98> vdd vss osc out<99> inverter4
END
```

Fig 11: Netlist for ring oscillator before editing

Log File showcasing Netlist Created successfully



The screenshot shows the Cadence Virtuoso log window with the title bar 'Virtuoso® 6.1.8-64b - Log: /home/class/sawan050/CDS.log'. The log content includes several loading messages for various components, two warnings about font and dialog box, an information message about changing the simulator, and a successful netlisting process. The netlisting statistics show 8 components, 1.0s elapsed time, and 0 errors/warnings. The process concludes with 'compose simulator input file...' and '...successful.'

```
Virtuoso® 6.1.8-64b - Log: /home/class/sawan050/CDS.log
File Tools Options Help
cadence

*WARNING* Font name *-helvetica-medium-r-*-12-* is invalid
Loading rte.cxt
Loading te.cxt
Loading schHDL.cxt
Loading viva.cxt
Loading spectrei.cxt
Loading cdf.cxt
Loading devCheck.cxt
Loading relXpert.cxt
Loading adpServer.cxt
*WARNING* hiDisplayAppDBox: modal dbox 'sevblockingDialogBox' is already displayed!
Loading hspiceD.cxt
INFO (ADE-1104): You are changing the simulator. All options that can be recognized
by the new simulator will be retained. All other options will be ignored.
You will not be warned about any ignored option. Be sure to check all your
forms (Analysis, Options, etc) to verify you have the setup you require
generate netlist...
Loading seCore.cxt
Begin Incremental Netlisting Sep 16 17:28:43 2023
Loading spectreinl.cxt
Loading msgHandler.cxt
Loading UltraSim.cxt
Loading AMSOSS.cxt
Loading AMS.cxt
Loading json.cxt
End netlisting Sep 16 17:28:43 2023
Loading monte.cxt

Netlisting Statistics:
  Number of components:      8

  Elapsed time:              1.0s (8.00/s)
Errors: 0  Warnings: 0
...successful.
compose simulator input file...
...successful.
```

Fig 12: Cadence Log denoting Netlist for ring oscillator created successfully

Netlist generated for ring oscillator as input.ckt file in default simulation folder copying to project directory simulation folder and renaming it as ring_osc.sp

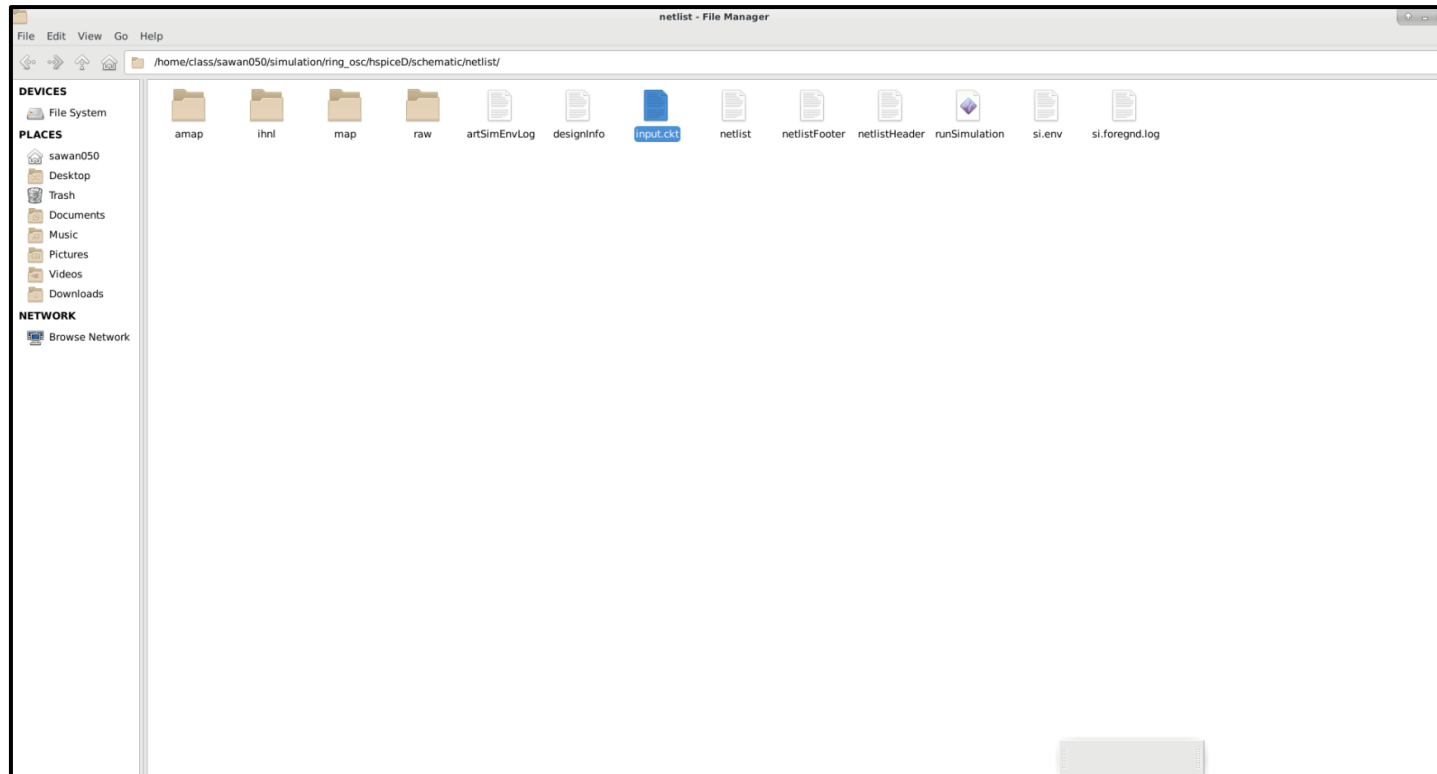


Fig 13: Netlist for ring oscillator and renaming it

Removing the temperature code and x from the gates from netlist file

```
** Generated for: hspiceD                                w=81e-9 l=20e-9 nfin=3    xi0<3> out<2> vdd vss
                                                         out<3> inverter4

** Generated on: Sep 16 17:28:43 2023                    ** Library name: ring_lib  xm5 y a vdd vdd pmos_rvt
                                                         w=81e-9 l=20e-9 nfin=3    xi0<4> out<3> vdd vss
                                                         out<4> inverter4

** Design library name: ring_lib                        ** Cell name: inverter4    xm4 y a vdd vdd pmos_rvt
                                                         w=81e-9 l=20e-9 nfin=3    xi0<5> out<86> inverter4

** Design cell name: ring_osc                          .subckt inverter4 a vdd vss y .ends inverter4
                                                         ** End of subcircuit
                                                         definition.
                                                         xi0<87> out<86> vdd vss
                                                         out<87> inverter4

** Design view name: schematic                        xm3 y a vss vss nmos_rvt
                                                         w=81e-9 l=20e-9 nfin=3    xi0<88> out<87> vdd vss
                                                         out<88> inverter4

.TEMP 25.0                                             xm2 y a vss vss nmos_rvt
                                                         w=81e-9 l=20e-9 nfin=3    ** Library name: ring_lib
                                                         xi0<96> out<95> vdd vss
                                                         out<96> inverter4

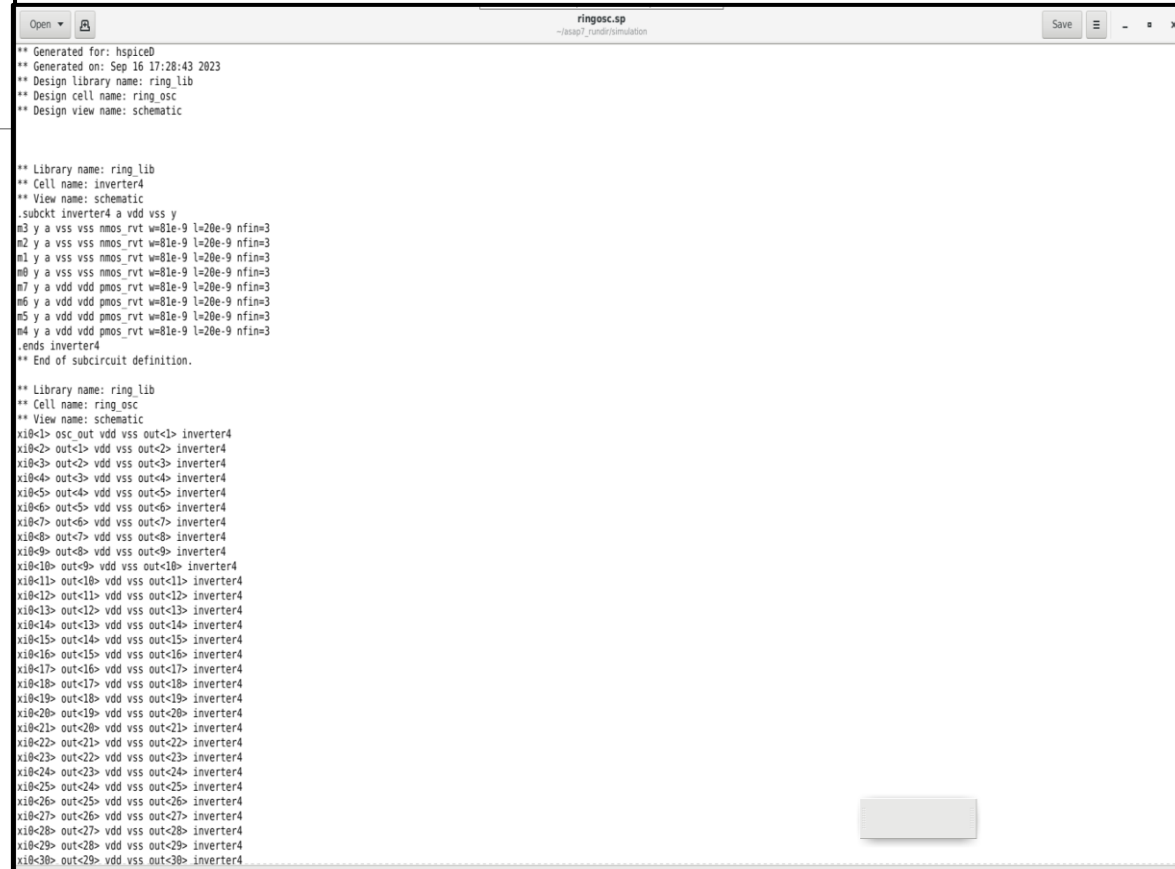
.OPTION
                                                         xm1 y a vss vss nmos_rvt
                                                         w=81e-9 l=20e-9 nfin=3    ** Cell name: ring_osc
                                                         xi0<97> out<96> vdd vss
                                                         out<97> inverter4

+ ARTIST=2                                             xm0 y a vss vss nmos_rvt
                                                         w=81e-9 l=20e-9 nfin=3    ** View name: schematic
                                                         xi0<98> out<97> vdd vss
                                                         out<98> inverter4

+ INGOLD=2                                             xm7 y a vdd vdd pmos_rvt
                                                         w=81e-9 l=20e-9 nfin=3    xi0<99> out<98> vdd vss
                                                         osc_out inverter4

+ PARHIER=LOCAL                                       xm6 y a vdd vdd pmos_rvt
                                                         .END
```

Fig 14: Netlist for ring oscillator before editing



```
ringosc.sp
-./asp7_run/simulation

** Generated for: hspiceD
** Generated on: Sep 16 17:28:43 2023
** Design library name: ring lib
** Design cell name: ring_osc
** Design view name: schematic

** Library name: ring lib
** Cell name: inverter4
** View name: schematic
.subckt inverter4 a vdd vss y
m3 y a vss vss nmos_rvt w=81e-9 l=20e-9 nfin=3
m2 y a vss vss nmos_rvt w=81e-9 l=20e-9 nfin=3
m1 y a vss vss nmos_rvt w=81e-9 l=20e-9 nfin=3
m0 y a vss vss nmos_rvt w=81e-9 l=20e-9 nfin=3
m7 y a vdd vdd pmos_rvt w=81e-9 l=20e-9 nfin=3
m6 y a vdd vdd pmos_rvt w=81e-9 l=20e-9 nfin=3
m5 y a vdd vdd pmos_rvt w=81e-9 l=20e-9 nfin=3
m4 y a vdd vdd pmos_rvt w=81e-9 l=20e-9 nfin=3
.ends inverter4
** End of subcircuit definition.

** Library name: ring lib
** Cell name: ring_osc
** View name: schematic
xi0<1> osc_out vdd vss out<1> inverter4
xi0<2> out<1> vdd vss out<2> inverter4
xi0<3> out<2> vdd vss out<3> inverter4
xi0<4> out<3> vdd vss out<4> inverter4
xi0<5> out<4> vdd vss out<5> inverter4
xi0<6> out<5> vdd vss out<6> inverter4
xi0<7> out<6> vdd vss out<7> inverter4
xi0<8> out<7> vdd vss out<8> inverter4
xi0<9> out<8> vdd vss out<9> inverter4
xi0<10> out<9> vdd vss out<10> inverter4
xi0<11> out<10> vdd vss out<11> inverter4
xi0<12> out<11> vdd vss out<12> inverter4
xi0<13> out<12> vdd vss out<13> inverter4
xi0<14> out<13> vdd vss out<14> inverter4
xi0<15> out<14> vdd vss out<15> inverter4
xi0<16> out<15> vdd vss out<16> inverter4
xi0<17> out<16> vdd vss out<17> inverter4
xi0<18> out<17> vdd vss out<18> inverter4
xi0<19> out<18> vdd vss out<19> inverter4
xi0<20> out<19> vdd vss out<20> inverter4
xi0<21> out<20> vdd vss out<21> inverter4
xi0<22> out<21> vdd vss out<22> inverter4
xi0<23> out<22> vdd vss out<23> inverter4
xi0<24> out<23> vdd vss out<24> inverter4
xi0<25> out<24> vdd vss out<25> inverter4
xi0<26> out<25> vdd vss out<26> inverter4
xi0<27> out<26> vdd vss out<27> inverter4
xi0<28> out<27> vdd vss out<28> inverter4
xi0<29> out<28> vdd vss out<29> inverter4
xi0<30> out<29> vdd vss out<30> inverter4
```

Fig 15: Netlist for ring oscillator after editing

Creating run_ringosc.sp file to run over hspice for analysis

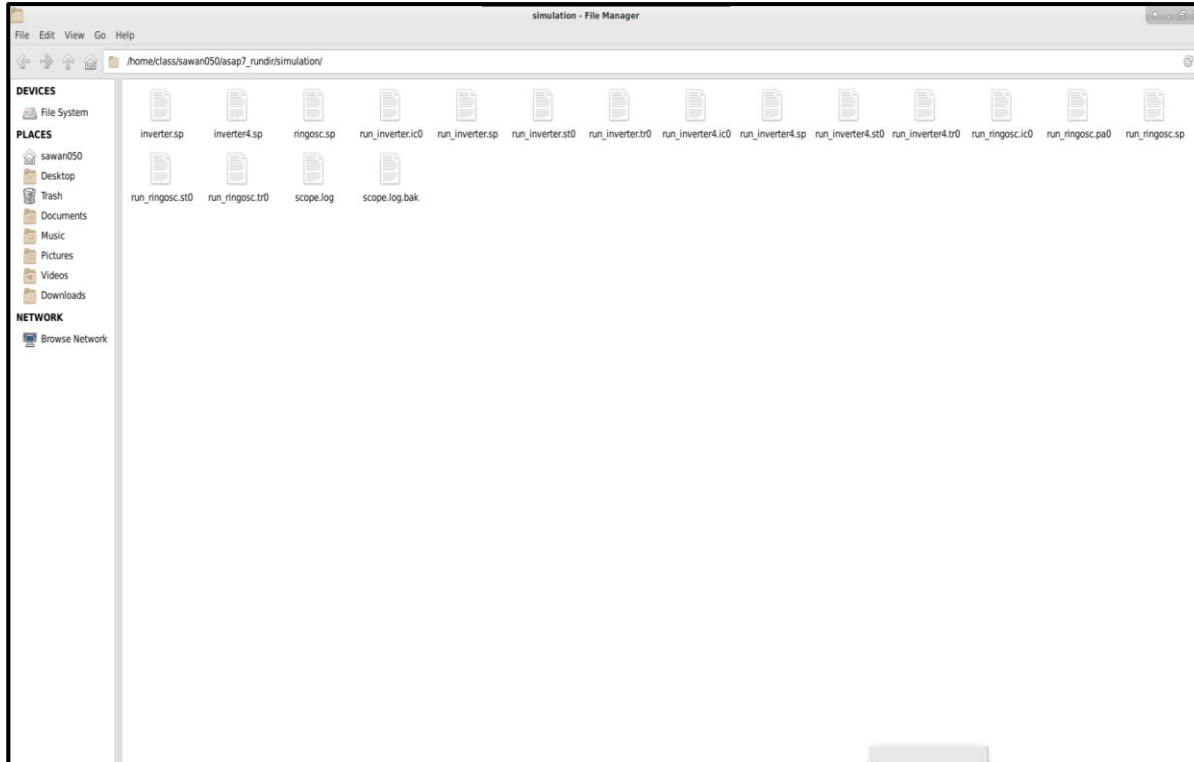


Fig 16: Run simulation file for ring oscillator

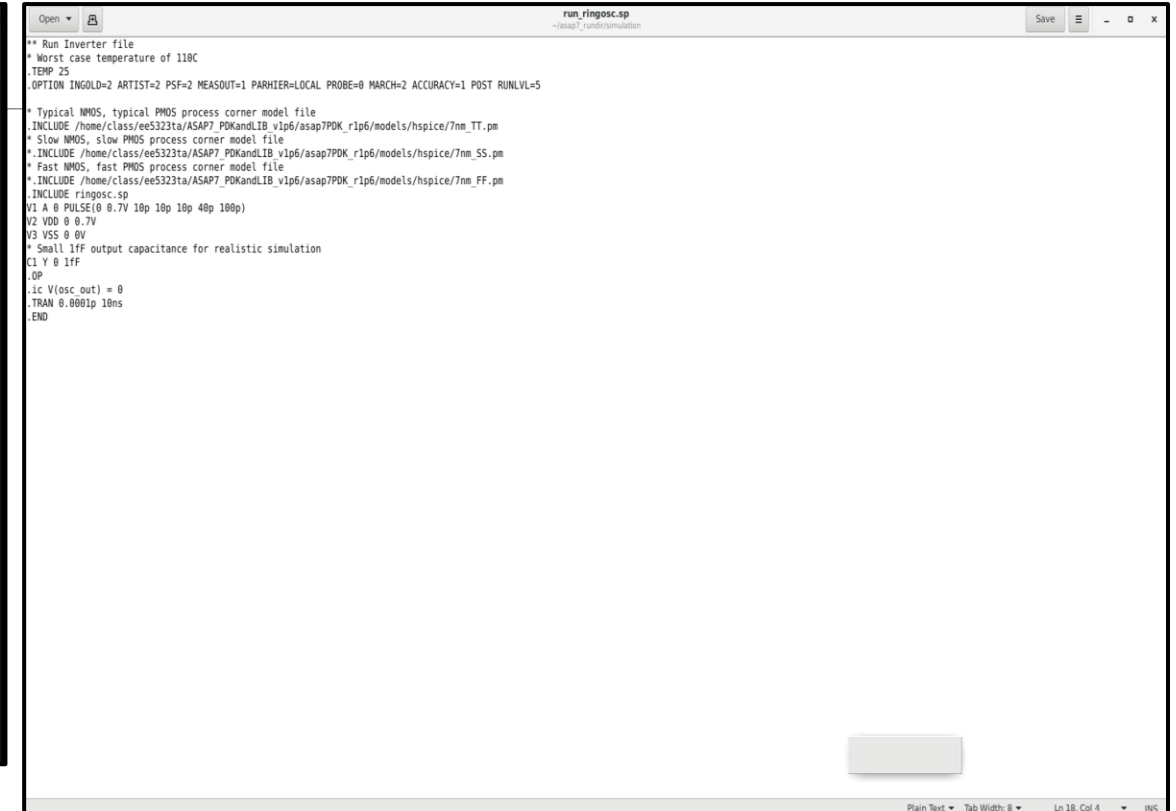
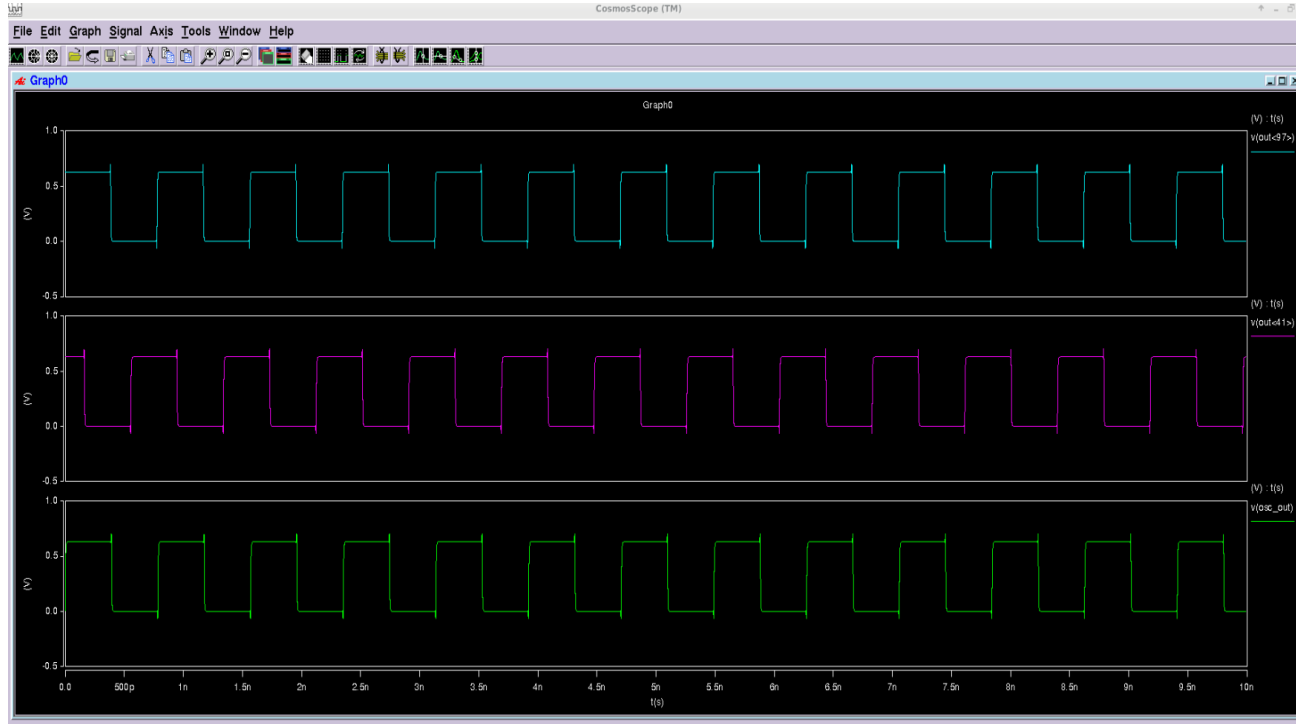


Fig 17: Run simulation file for ring oscillator manipulating it

**Process corner = SS (slow), VDD = 0.63V (-10% VDD),
Temperature = 110°C,**



*Fig 18: Process corner = SS (slow), VDD = 0.63V (-10% VDD),
Temperature = 110°C*

cgd 3.191e-17 3.191e-17

```
*****  
** run inverter file  
  
***** transient analysis tnom= 25.000 temp= 110.000 *****  
period= 7.8931e-10 targ= 2.3616e-09 trig= 1.5723e-09  
frequency= 1.2669e+09  
iavg=-1.3250e-04 from= 0.0000e+00 to= 1.0000e-08  
power=-8.3472e-05  
  
***** job concluded  
*****  
** run inverter file  
  
***** job statistics summary tnom= 25.000 temp= 110.000 *****  
  
***** Machine Information *****
```

Fig 19: freq = 1.266 GHz , Power = -8.3472e-5 W

Process corner = FF (fast), VDD = 0.77V (+10% VDD), Temperature = -40°C

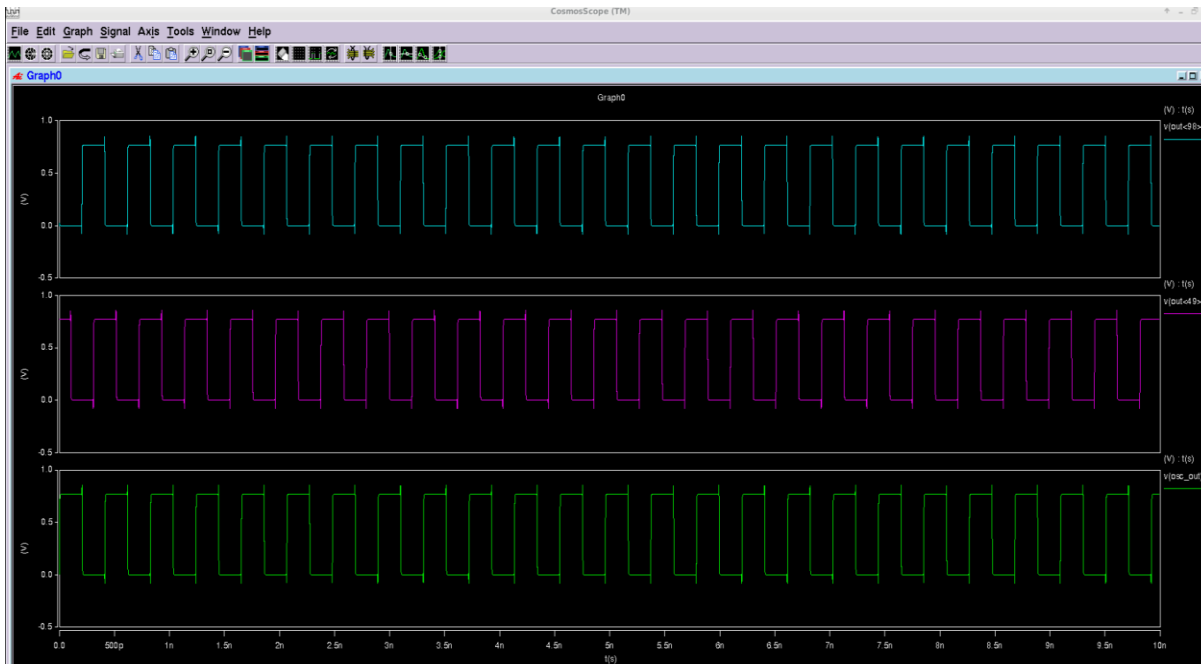


Fig 20: Process corner = FF (fast), VDD = 0.77V (+10% VDD), Temperature = -40°C

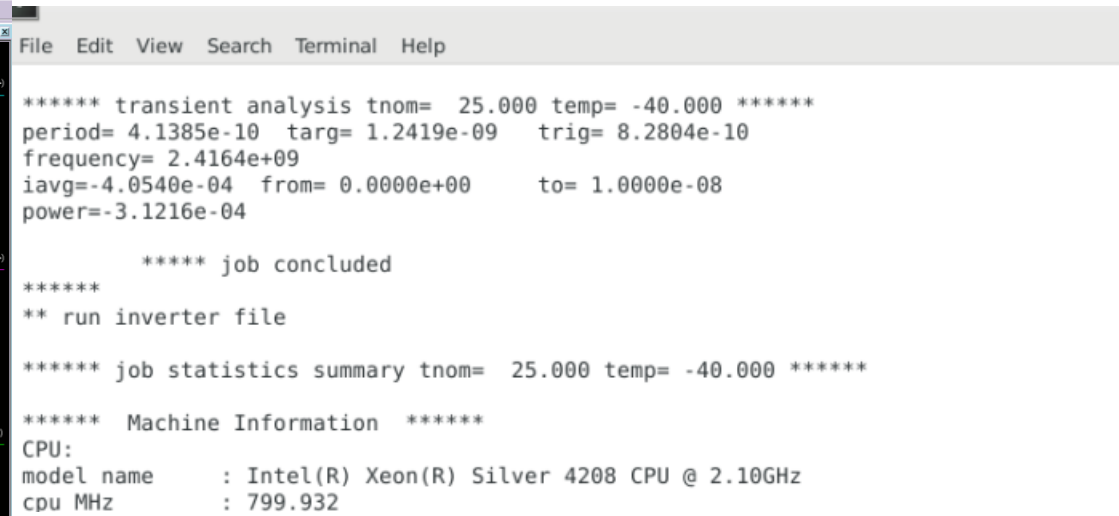


Fig 21: freq = 2.4164GHz, Power = -3.1216e-4 W

Process corner = TT (typical, i.e. nominal), VDD = 0.7V (-10% VDD), Temperature = 25°C (nominal),

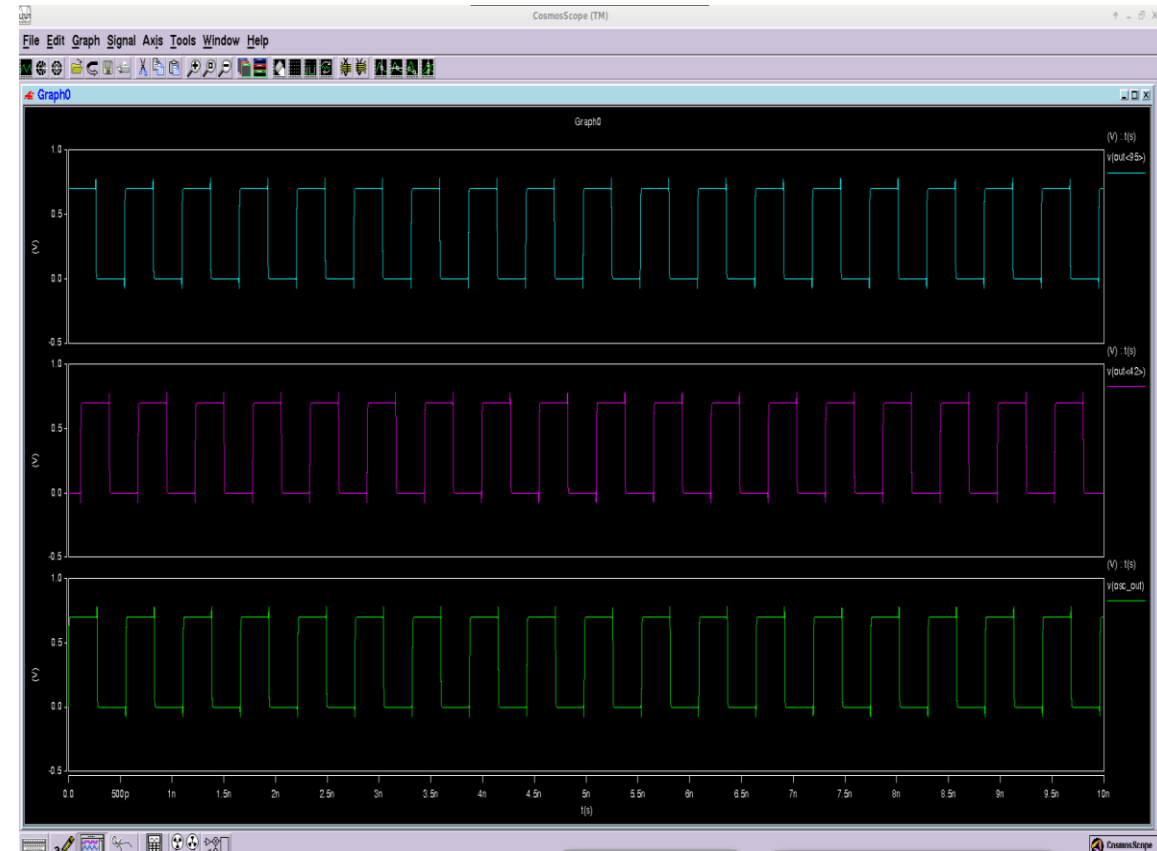


Fig 22: Process corner = TT (typical, i.e. nominal), VDD = 0.7V (-10% VDD), Temperature = 25°C (nominal),

```
File Edit View Search Terminal Help
** run inverter file

***** transient analysis tnom= 25.000 temp= 25.000 *****
period= 5.5464e-10 targ= 1.6636e-09 trig= 1.1090e-09
frequency= 1.8030e+09
iavg=-2.3484e-04 from= 0.0000e+00 to= 1.0000e-08
power=-1.6439e-04

***** job concluded
*****
** run inverter file

***** job statistics summary tnom= 25.000 temp= 25.000 *****
```

Fig 23: freq = 1.803 GHz , Power = -1.6439e-4 W

VDD= 0.7 , Process corner = tt, Temperature = 110

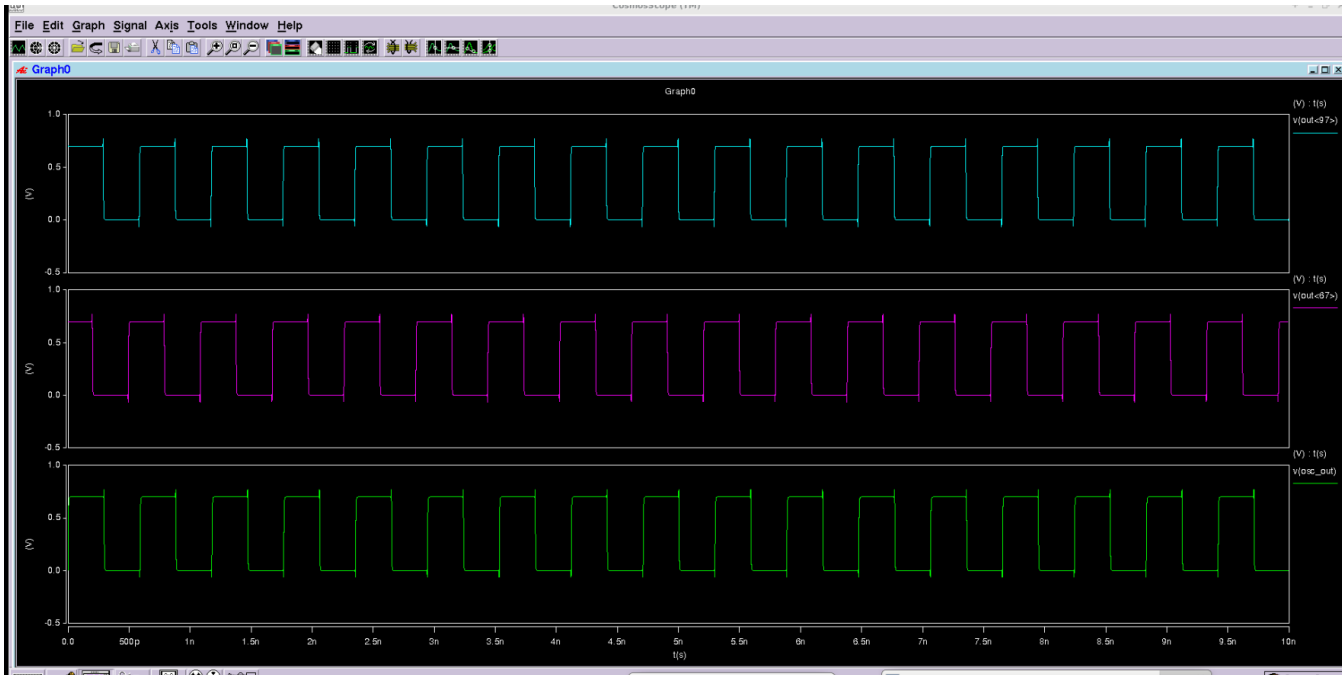


Fig 24: VDD= 0.7 , Process corner = tt, Temperature = 110

```
** run inverter file

***** transient analysis tnom= 25.000 temp= 110.000 *****
period= 5.9016e-10  targ= 1.7701e-09  trig= 1.1800e-09
frequency= 1.6945e+09
iavg=-2.2468e-04  from= 0.0000e+00  to= 1.0000e-08
power=-1.5728e-04

***** job concluded
*****
** run inverter file

***** job statistics summary tnom= 25.000 temp= 110.000 *****
```

Fig 25: freq = 1.6945 GHz , Power = -1.57282e-4 W

Process corner = Tt , VDD = 0.7 , Temperature = -40

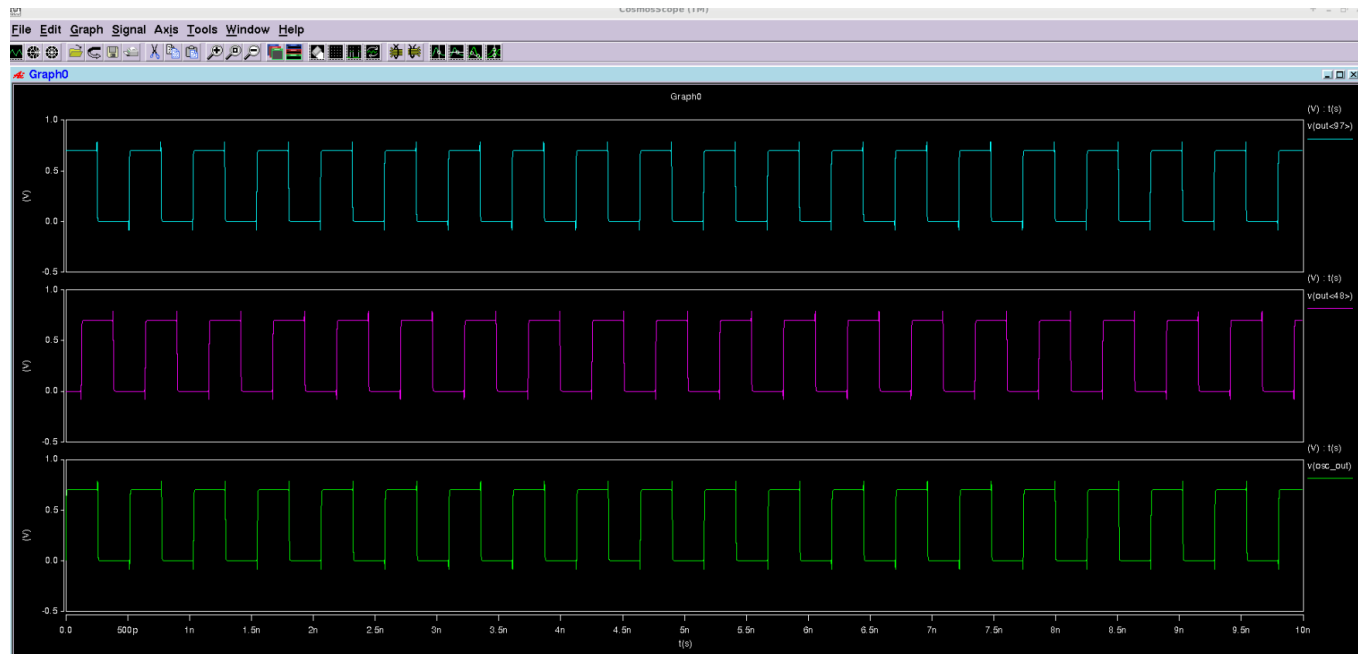


Fig 26: Process corner = Tt , VDD = 0.7 , Temperature = -40

```
File Edit View Search Terminal Help
** run inverter file

***** transient analysis tnom= 25.000 temp= -40.000 *****
period= 5.1684e-10 targ= 1.5503e-09 trig= 1.0335e-09
frequency= 1.9348e+09
iavg=-2.5120e-04 from= 0.0000e+00 to= 1.0000e-08
power=-1.7584e-04

***** job concluded
*****
** run inverter file

***** job statistics summary tnom= 25.000 temp= -40.000 *****

***** Machine Information *****
CPU:
model name      : Intel(R) Xeon(R) Silver 4208 CPU @ 2.10GHz
CPU MHz         : 700.000
```

Fig 27: freq = 1.9348GHz , Power = -1.7584e-4 W

Process corner = Tt, VDD = 0.63, Temperature = 25

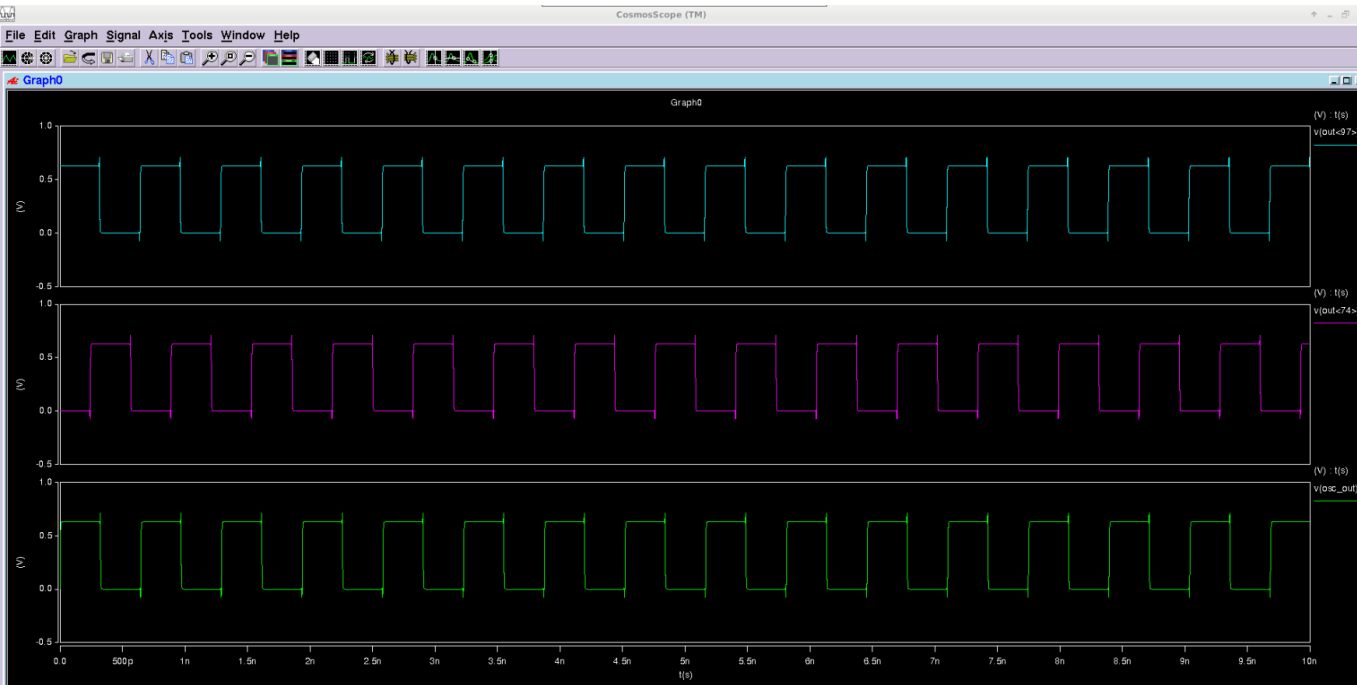


Fig 28: Process corner = Tt, VDD = 0.63, Temperature = 25

```
sawan050@ec
File Edit View Search Terminal Help
** run inverter file

***** transient analysis tnom= 25.000 temp= 25.000 *****
period= 6.4978e-10 targ= 1.9439e-09 trig= 1.2941e-09
frequency= 1.5390e+09
iavg=-1.7589e-04 from= 0.0000e+00 to= 1.0000e-08
power=-1.1081e-04

**** job concluded
*****
** run inverter file

***** job statistics summary tnom= 25.000 temp= 25.000 *****

***** Machine Information *****
CPU:
model name      : Intel(R) Xeon(R) Silver 4208 CPU @ 2.10GHz
cpu MHz         : 2983.886
```

Fig 29: freq = 1.539 GHz , Power = -1.1081e-4 W

Process corner = Tt, VDD = 0.77, Temperature = 25

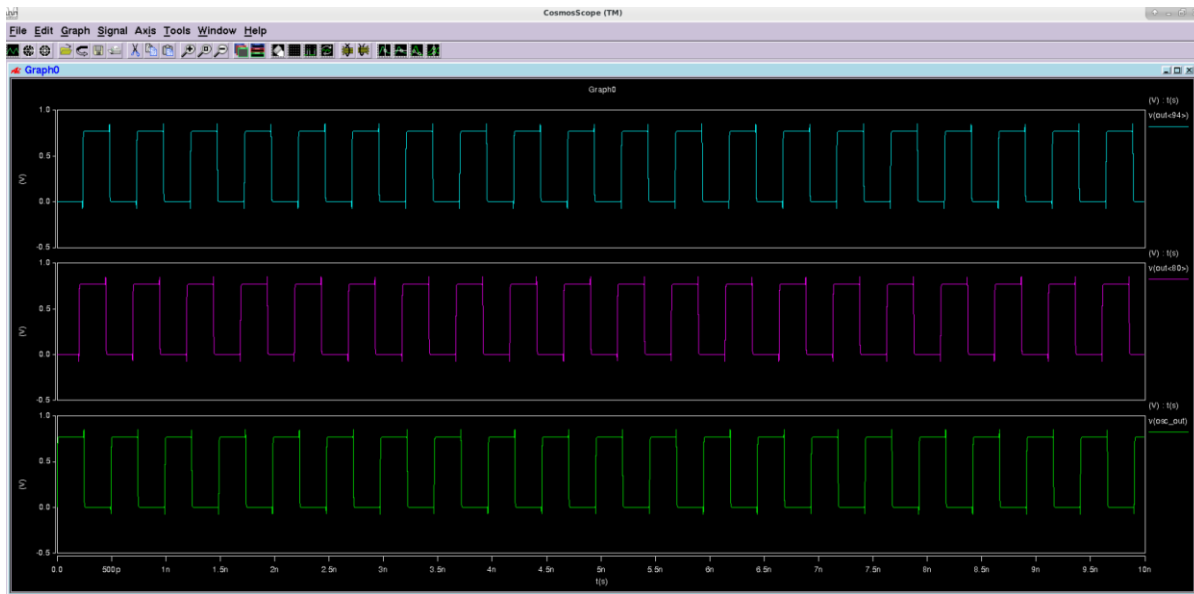


Fig 30: Process corner = Tt, VDD = 0.77, Temperature = 25

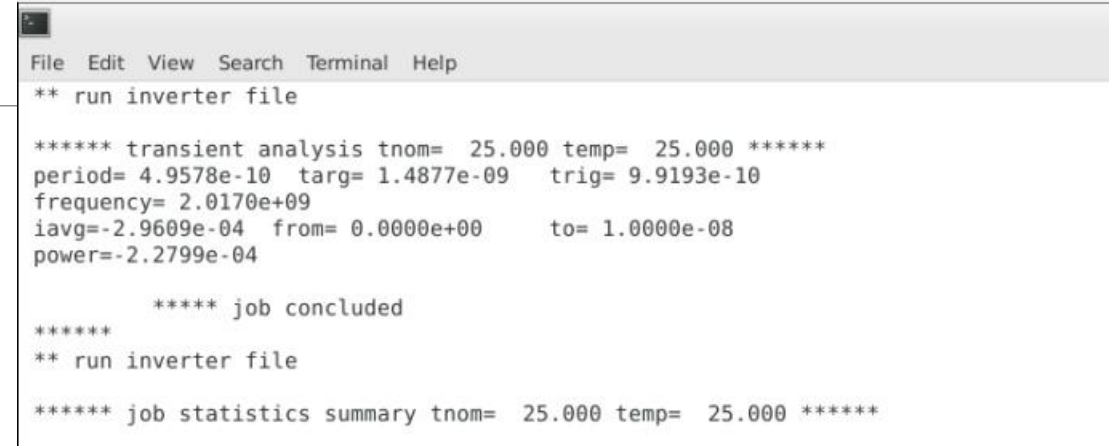


Fig 31: freq = 2.017 GHz , Power = -2.2799e-4 W

Process corner = Ss, VDD = 0.7, Temperature = 25

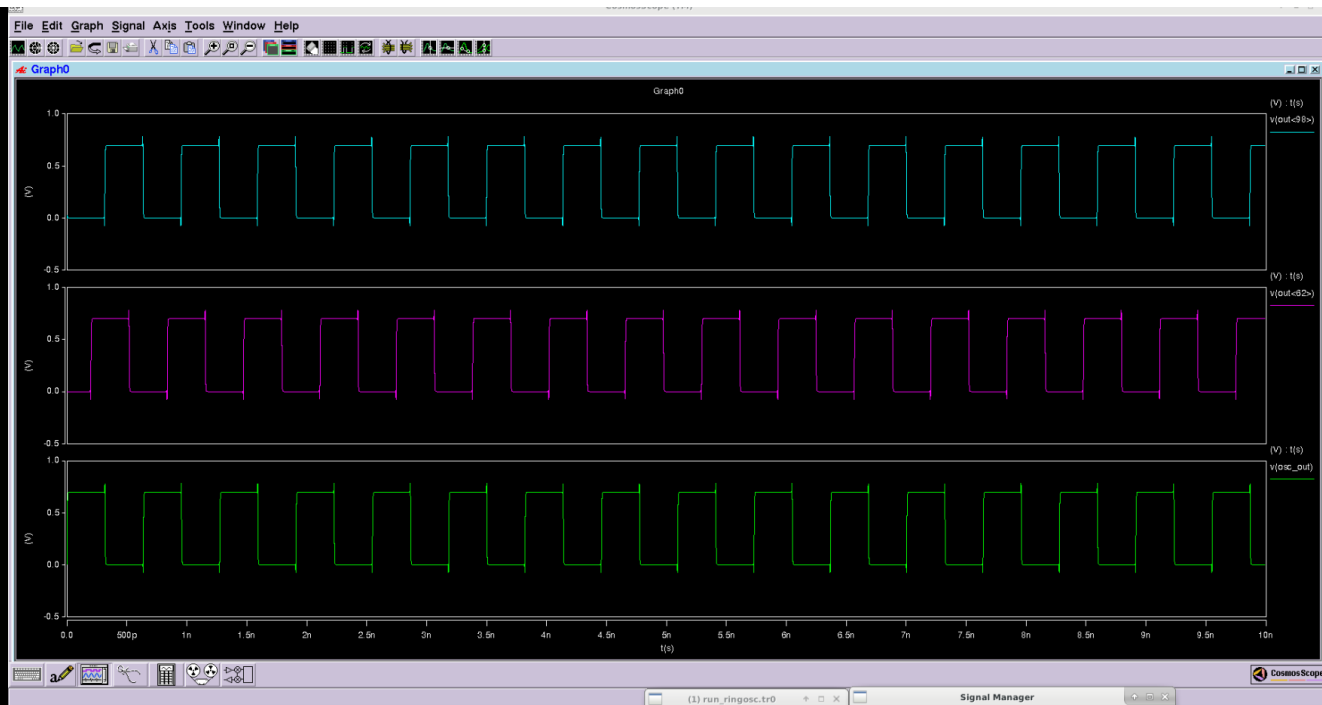


Fig 32 : Process corner = Ss, VDD = 0.7, Temperature = 25

```
File Edit View Search Terminal Help
** run inverter file

***** transient analysis tnom= 25.000 temp= 25.000 *****
period= 6.3808e-10 targ= 1.9140e-09 trig= 1.2759e-09
frequency= 1.5672e+09
iavg=-1.8279e-04 from= 0.0000e+00 to= 1.0000e-08
power=-1.2795e-04

***** job concluded
*****
** run inverter file

***** job statistics summary tnom= 25.000 temp= 25.000 *****
```

Fig 33 : freq = 1.5672 GHz, Power = -1.2795e-4 W

Process corner = Ff, VDD = 0.7, Temperature = 25

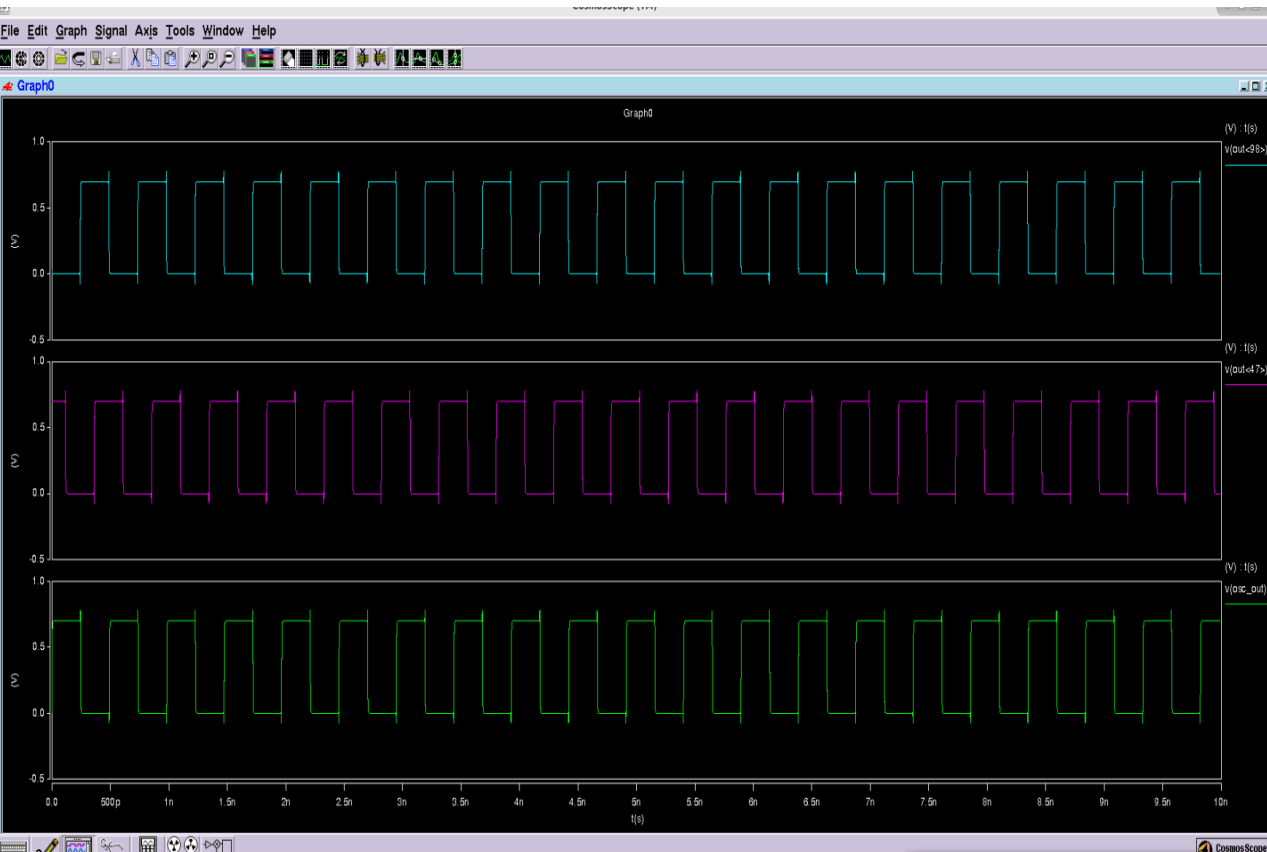


Fig 34: Process corner = Ff, VDD = 0.7, Temperature = 25

```
File Edit View Search Terminal Help
** run inverter file

***** transient analysis tnom= 25.000 temp= 25.000 *****
period= 4.9215e-10 targ= 1.4762e-09 trig= 9.8402e-10
frequency= 2.0319e+09
iavg=-3.0136e-04 from= 0.0000e+00 to= 1.0000e-08
power=-2.1095e-04

***** job concluded
*****
** run inverter file

***** job statistics summary tnom= 25.000 temp= 25.000 *****
***** Machine Information *****
```

Fig 35: freq = 2.0319 GHz, Power = -2.1095e-5 W

Analysis

Process Corner	Voltage	Temperature	Frequency and Power
ff	.7	25	$freq = 2.0319 \text{ GHz}$, $Power = -2.1095e-5 \text{ W}$
ss	.7	25	$freq = 1.5672 \text{ GHz}$, $Power = -1.2795e-4 \text{ W}$
tt	.77	25	$freq = 2.017 \text{ GHz}$, $Power = -2.2799e-4 \text{ W}$
tt	.63	25	$freq = 1.539 \text{ GHz}$, $Power = -1.1081e-4 \text{ W}$
tt	.7	-40	$freq = 1.9348 \text{ GHz}$, $Power = -1.7584e-4 \text{ W}$
tt	.7	110	$freq = 1.6945 \text{ GHz}$, $Power = -1.57282e-4 \text{ W}$
tt.	.7	25	$freq = 1.803 \text{ GHz}$, $Power = -1.6439e-4 \text{ W}$
ff	.77	-40	$freq = 2.4164 \text{ GHz}$, $Power = -3.1216e-4 \text{ W}$
ss	.63	110	$freq = 1.266 \text{ GHz}$, $Power = -8.3472e-5 \text{ W}$

Conclusion

The frequency and power characteristics of such an oscillator can vary at different process corners due to the following reasons:

- 1. Supply Voltage Variation:** At different process corners, the supply voltage can vary. In the low voltage corner (LL), the supply voltage is lower, which can result in slower operation and lower power consumption. In the high voltage corner (HH), the supply voltage is higher, which can lead to faster operation and higher power consumption.
 - 2. Temperature Variation:** Process corners also consider variations in temperature. Higher temperatures can lead to increased resistance and slower transistor operation, affecting the frequency and power consumption of the oscillator.
- The schematic corresponding to the INVx4_ASAP7_75t_R layout was successfully drawn in Virtuoso. This layout was used as a fundamental building block for the subsequent ring oscillator design.
 - Ring Oscillator Design: A 99-stage ring oscillator was designed in Virtuoso using the inverter symbol
 - This assignment allowed for practical experience in designing and analyzing digital circuits, considering the impact of variations in process, voltage, and temperature on circuit performance.