

EE 5323 Homework #2: Inverter and Ring Oscillator Layout

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INVx4_ASAP_75t_R Standard Inverter Layout

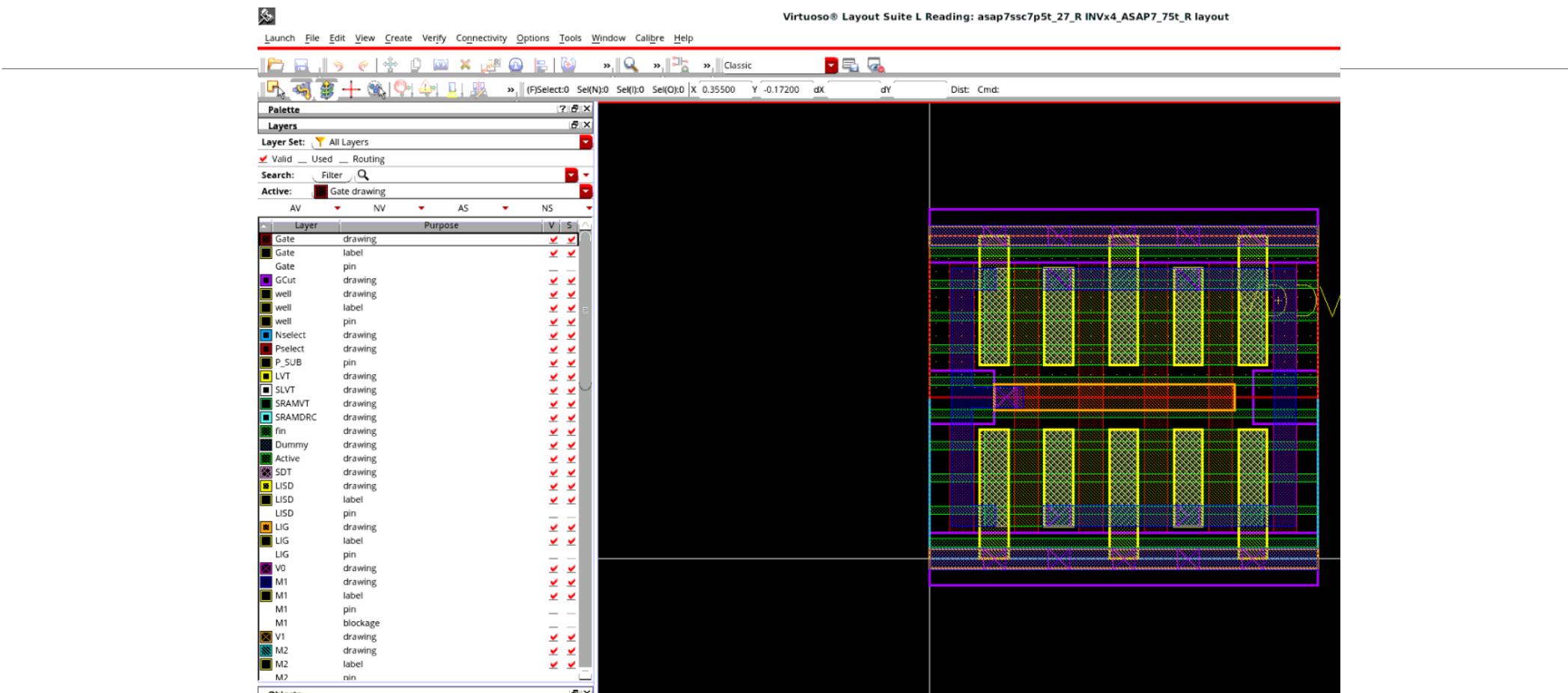


Fig 1: layout of an inverter in the ASAP7 standard cell library

Layers in Cadence Virtuoso Specified for Inverter

Layer	Purpose	Layer No	Priority No	Mask No.	Function	Description
Gate	Drawing	7	133	7	Poly	
Gate	Label	7	135	7	poly	Annotate
Gate	Pin	7	136	7	poly	Drawing
Gate Cut	Drawing	10	137		Recognition	
well		1	138		nwell	
well	Label	1	139		nwell	
well	Pin	1	140		nwell	
Nselect	Drawing	12	141		Recognition	
Pselect	Drawing	13	142		Recognition	
P_sub	pin	3	143			
LVT	Drawing	98	144			
SLVT	Drawing	97	145			
SRAMVT	Drawing	110	146			
SRAMDRC	Drawing	99	147			

Table1: Teardown the layout of an inverter in the ASAP7 standard cell library

Layers in Cadence Virtuoso Specified for Inverter

Layer	Purpose	Layer No	Priority No	Mask No.	Function	Description
Fin	Drawing	2	148		Recognition	
Dummy	Drawing	8	149		Recognition	
Active	Drawing	11	150		diff	
SDT	Drawing	88	151		cut	
LISD	Drawing	17	154		li	
LISD	label	17	158		li	
LISD	pin	17	159		li	
LIG	Drawing	16	160		li	
LIG	Label	16	164		li	
LIG	pin	16	165		li	
V0	Drawing	18	166		cut	
M1	Drawing	19	172		metal	
M1	Label	19	175		metal	
M1	pin	19	181		metal	
M1	blockage	19	182		metal	

Layers in Cadence Virtuoso Specified for Inverter

Layer	Purpose	Layer No	Priority No	Mask No.	Function	Description
V1	Drawing	21	183		cut	
M2	Drawing	20	189		metal	
M2	Label	20	192		metal	
M2	pin	20	198		metal	
M2	blockage	20	199		metal	
V2	Drawing	25	200		cut	
M3	Drawing	30	206		metal	
M3	Label	30	209		metal	
M3	pin	30	215		metal	
M3	blockage	30	216		metal	
V3	Drawing	35	217		cut	
M4	Drawing	40	223		metal	
M4	Label	40	226		metal	
M4	Mandrel	40	230		metal	
M4	trim	40	231		metal	

Layers in Cadence Virtuoso Specified for Inverter

Layer	Purpose	Layer No	Priority No	Mask No.	Function	Description
M4	pin	40	232		metal	
M4	blockage	40	233		metal	
V4	Drawing	45	234		cut	
M5	Drawing	50	240		metal	
M5	Label	50	243		metal	
M5	Mandrel	50	247		metal	
M5	trim	50	248		metal	
M5	pin	50	249		metal	
M5	blockage	50	250		metal	
V5	Drawing	55	251		cut	
M6	Drawing	60	257		metal	
M6	Label	60	260		metal	
M6	Mandrel	60	264		metal	
M6	trim	60	265		metal	
M6	pin	60	266		metal	

Layers in Cadence Virtuoso Specified for Inverter

Layer	Purpose	Layer No	Priority No	Mask No.	Function	Description
M6	blockage	60	267		metal	
V6	Drawing	65	268		cut	
M7	Drawing	70	274		metal	
M7	Label	70	277		metal	
M7	Mandrel	70	281		metal	
M7	trim	70	282		metal	
M7	pin	70	283		metal	
M7	blockage	70	284		metal	
V7	Drawing	75	285		cut	
M8	Drawing	80	291		metal	
M8	Label	80	294		metal	
M8	pin	80	300		metal	
M8	blockage	80	301		metal	
V8	Drawing	85	302		cut	
M9	Drawing	90	308		metal	
M9	label	90	311		metal	

Layers in Cadence Virtuoso Specified for Inverter

Layer	Purpose	Layer No	Priority No	Mask No.	Function	Description
M9	pin	90	317		metal	
M9	blockage	90	318		metal	
V9	Drawing	95	319		cut	
V9	color1	95	322		cut	
V9	color2	95	323		cut	
V9	color3	95	324		cut	
Pad	Drawing	96	325		metal	
Pad	Label	96	328		metal	
Pad	pin	96	329		metal	
Pad	blockage	96	330		metal	
Boundary	Drawing	100	331			
Text	label	101	332			

Inverter4 Schematic in ring_lib

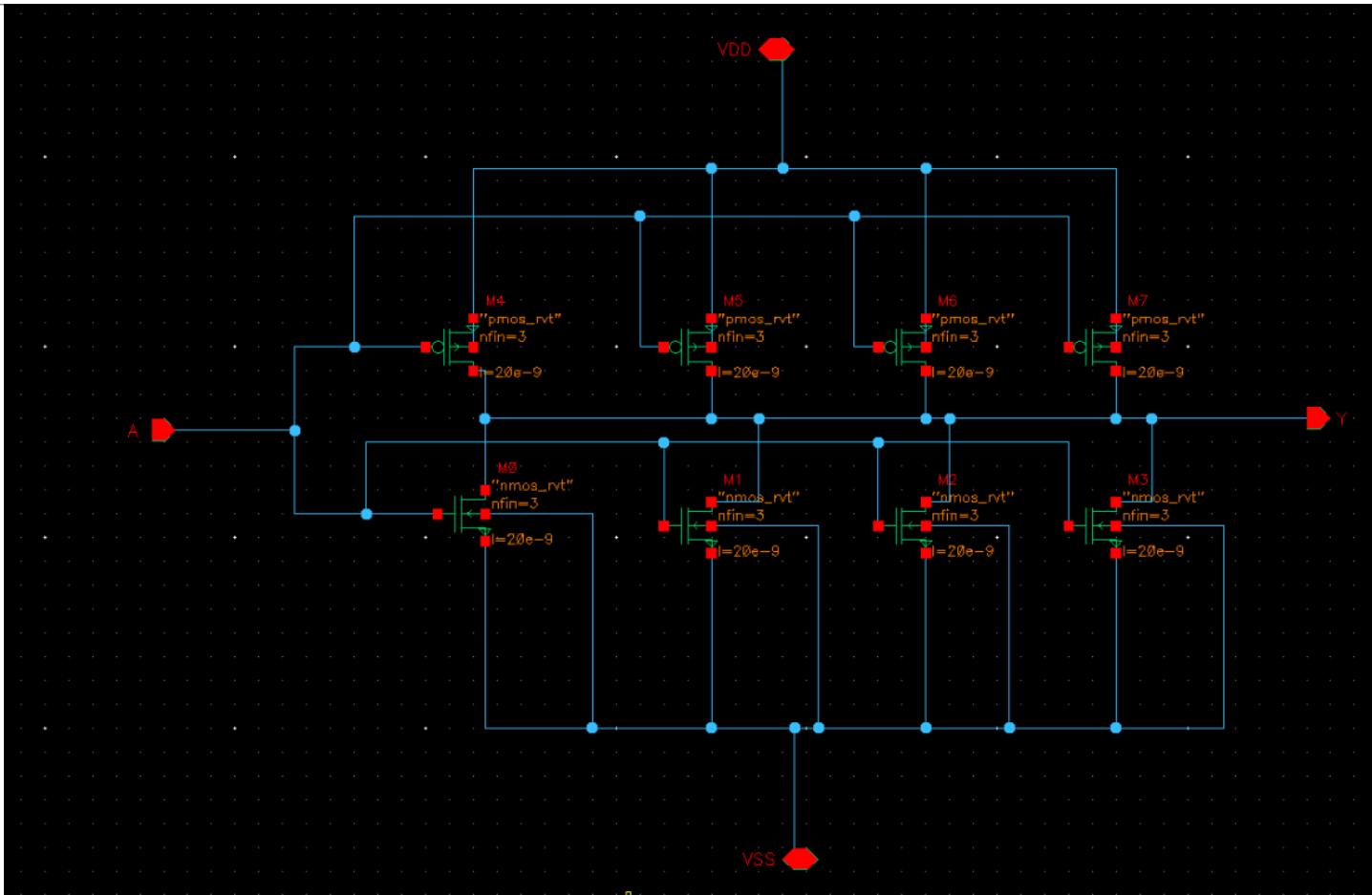


Fig 2: circuit schematic in Library ring_lib for inverter4

inverter4 symbol created earlier in ring_lib to use in ring_osc schematic

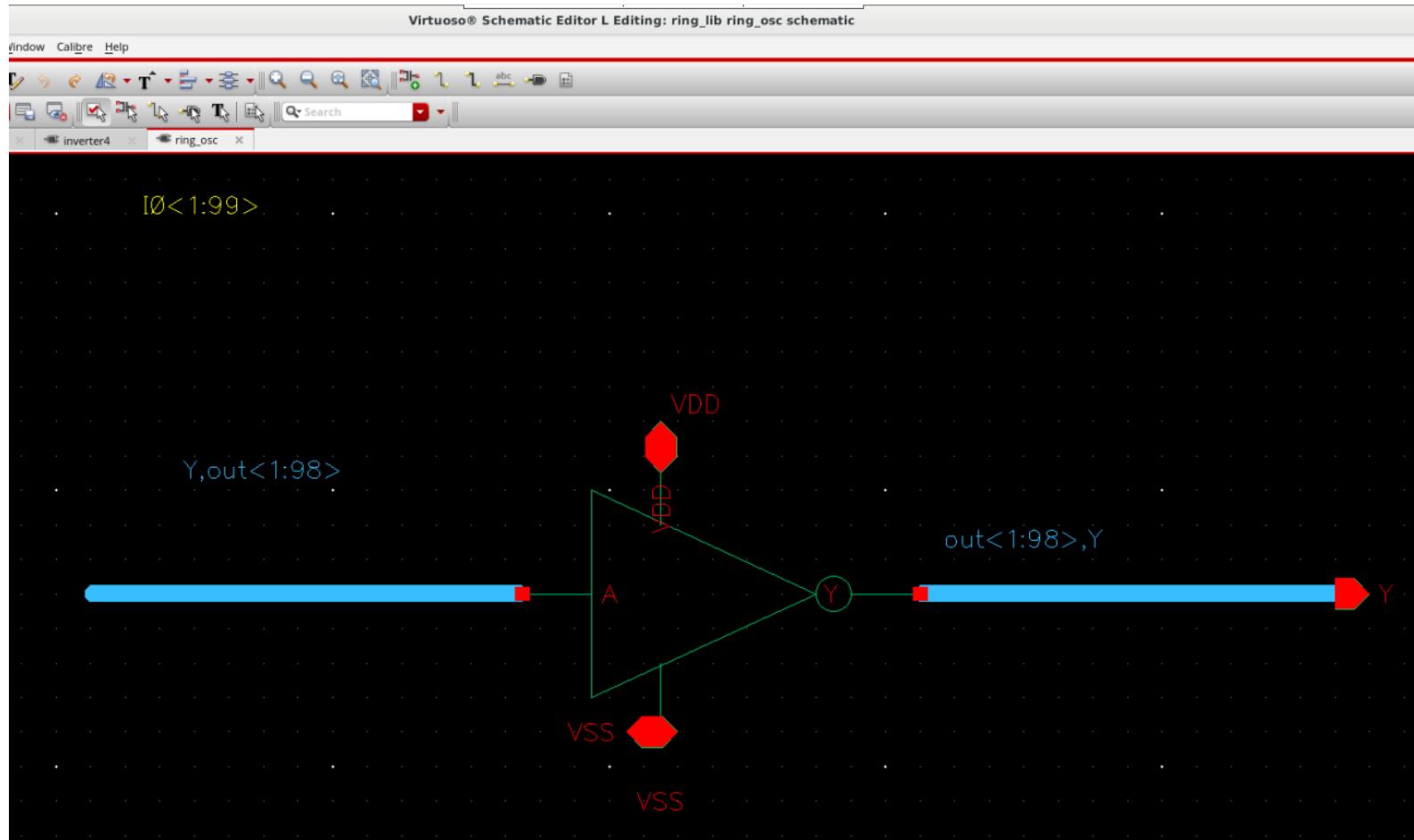


Fig 3: schematic of 99 stage ring oscillator in Library ring_lib

Layout of 99 stage ring oscillator with name trial in ring_lib



Fig 4: layout of 99 stage ring oscillator with name trial in Library ring_lib

Details of layout

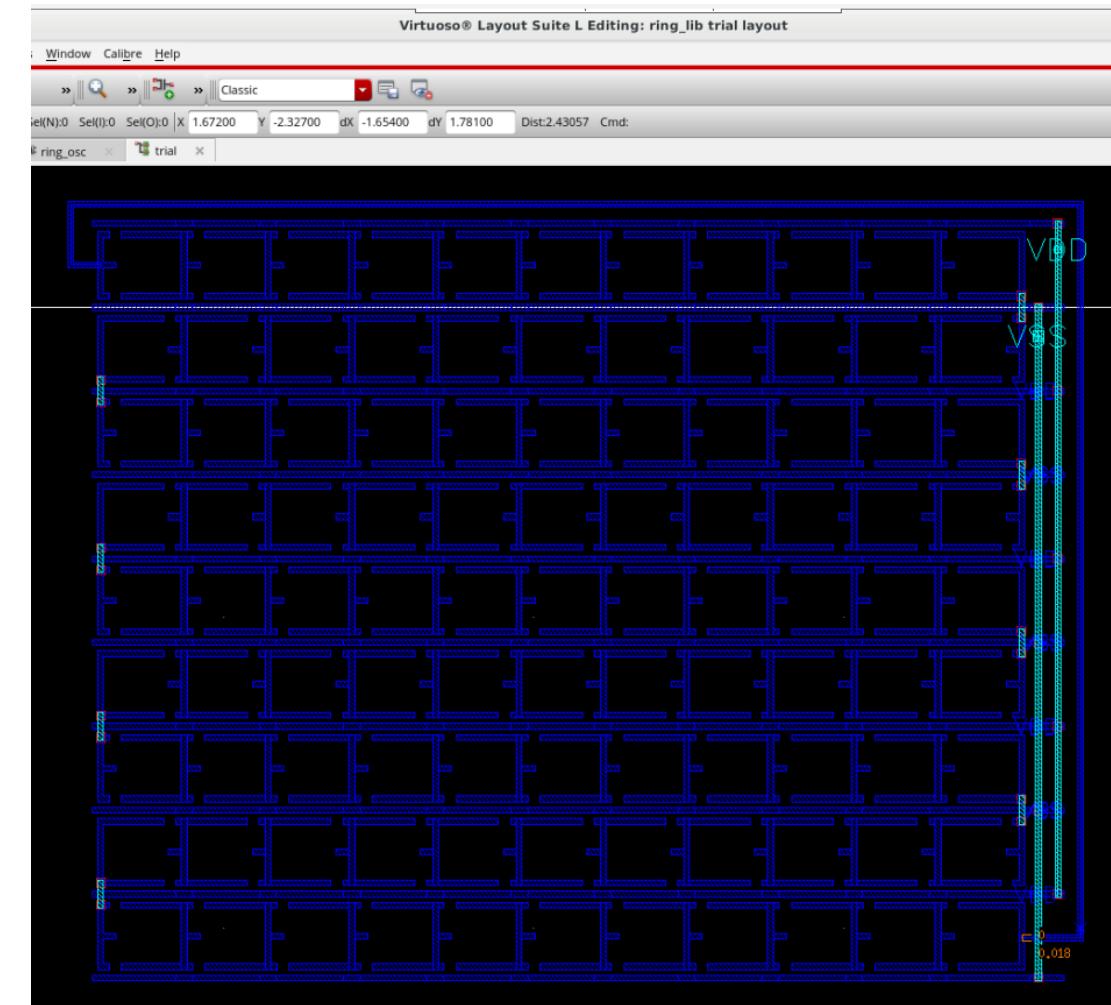


Fig 5: M2 layer to connect the respective inverter output to input of next oscillator , using M2 to short the VDD , VSS

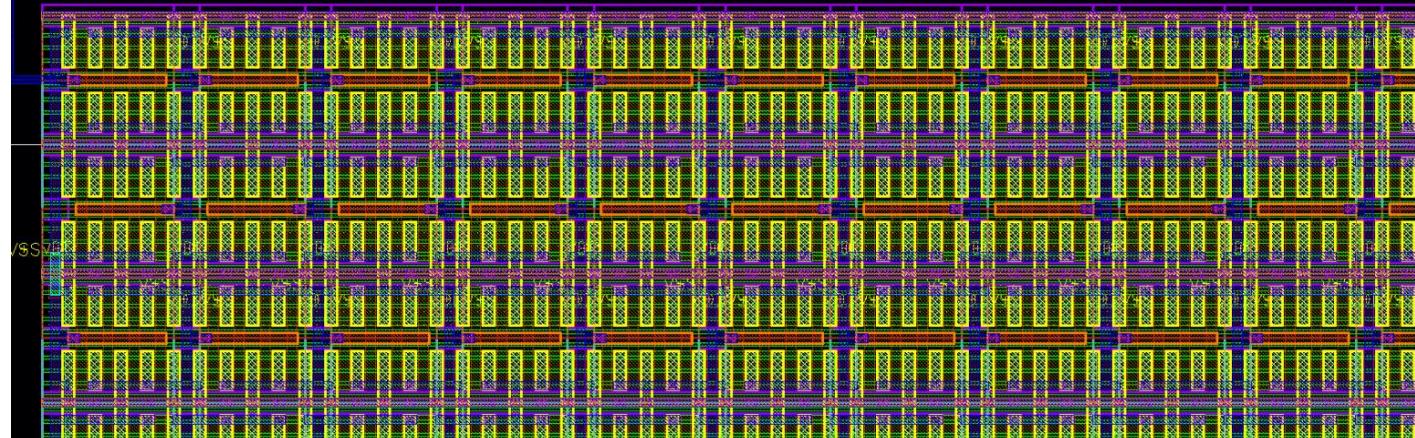
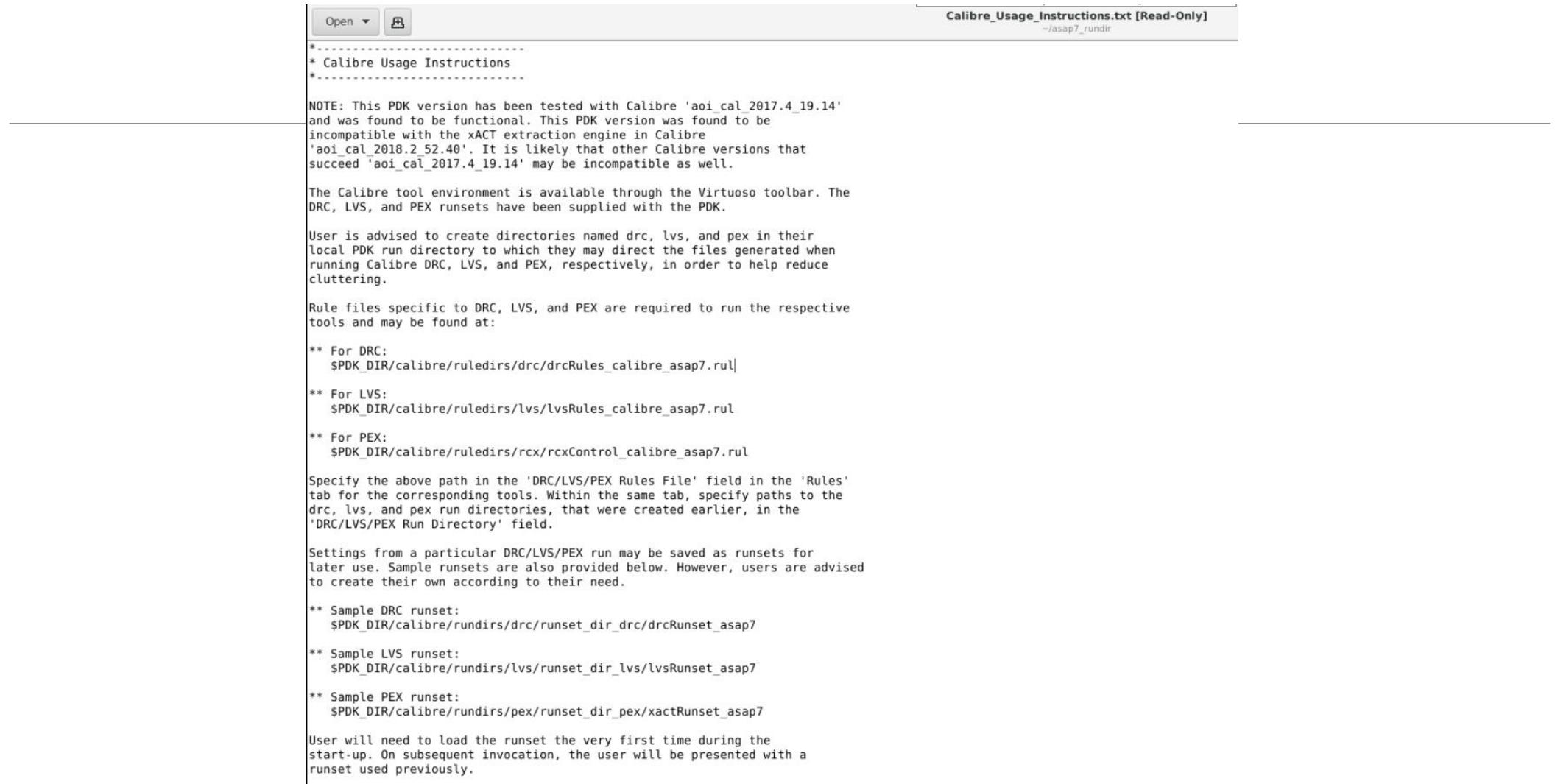


Fig 6: 11x 9 array of Inverter4 to create 99 stage ring oscillator

Instruction file for Calibre



The screenshot shows a text editor window with the title bar "Calibre_Usage_Instructions.txt [Read-Only]" and the path "-/asap7_rundir". The file content is as follows:

```
Open [X]
-----
* Calibre Usage Instructions
-----

NOTE: This PDK version has been tested with Calibre 'aoi_cal_2017.4_19.14'
and was found to be functional. This PDK version was found to be
incompatible with the xACT extraction engine in Calibre
'aoi_cal_2018.2_52.40'. It is likely that other Calibre versions that
succeed 'aoi_cal_2017.4_19.14' may be incompatible as well.

The Calibre tool environment is available through the Virtuoso toolbar. The
DRC, LVS, and PEX runsets have been supplied with the PDK.

User is advised to create directories named drc, lvs, and pex in their
local PDK run directory to which they may direct the files generated when
running Calibre DRC, LVS, and PEX, respectively, in order to help reduce
cluttering.

Rule files specific to DRC, LVS, and PEX are required to run the respective
tools and may be found at:

** For DRC:
$PDK_DIR/calibre/ruledirs/drc/drcRules_calibre_asap7.rul

** For LVS:
$PDK_DIR/calibre/ruledirs/lvs/lvsRules_calibre_asap7.rul

** For PEX:
$PDK_DIR/calibre/ruledirs/rcx/rcxControl_calibre_asap7.rul

Specify the above path in the 'DRC/LVS/PEX Rules File' field in the 'Rules'
tab for the corresponding tools. Within the same tab, specify paths to the
drc, lvs, and pex run directories, that were created earlier, in the
'DRC/LVS/PEX Run Directory' field.

Settings from a particular DRC/LVS/PEX run may be saved as runsets for
later use. Sample runsets are also provided below. However, users are advised
to create their own according to their need.

** Sample DRC runset:
$PDK_DIR/calibre/rundirs/drc/runset_dir_drc/drcRunset_asap7

** Sample LVS runset:
$PDK_DIR/calibre/rundirs/lvs/runset_dir_lvs/lvsRunset_asap7

** Sample PEX runset:
$PDK_DIR/calibre/rundirs/pex/runset_dir_pex/xactRunset_asap7

User will need to load the runset the very first time during the
start-up. On subsequent invocation, the user will be presented with a
runset used previously.
```

Fig 7: Instruction file for calibre

Drc steps

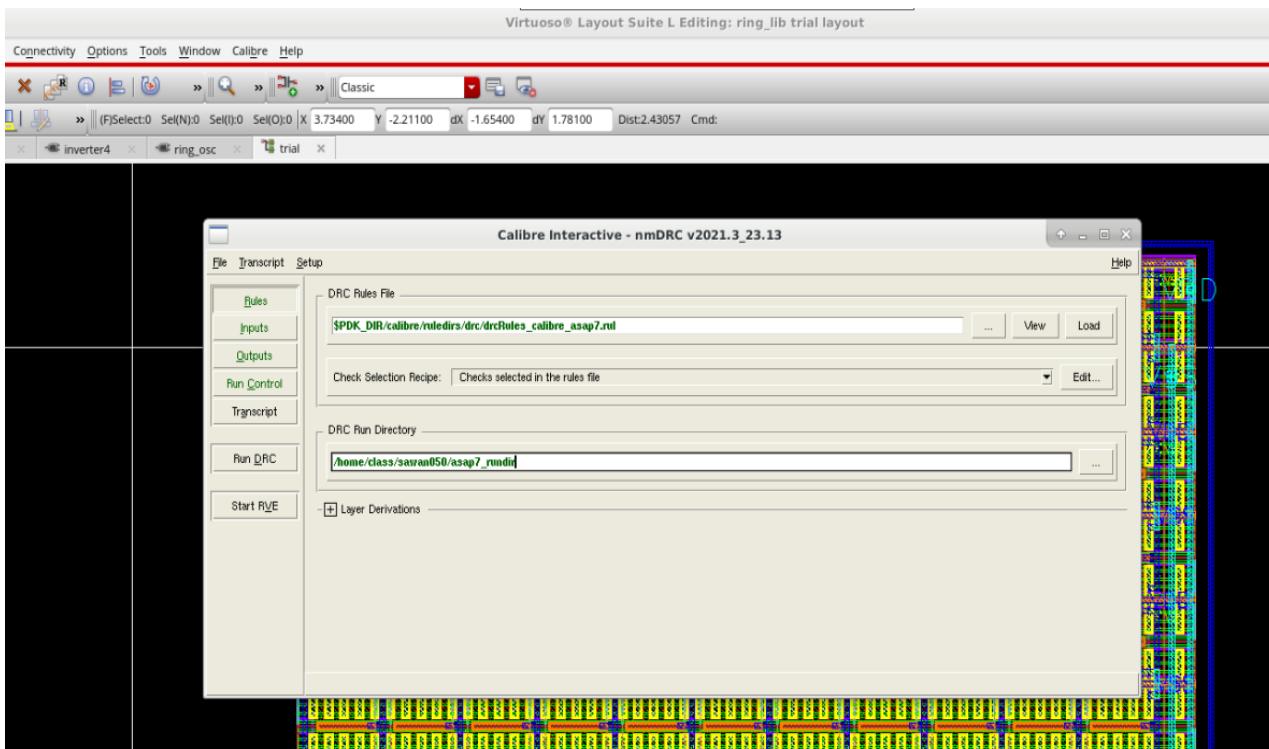


Fig 8: Drc rules file setting

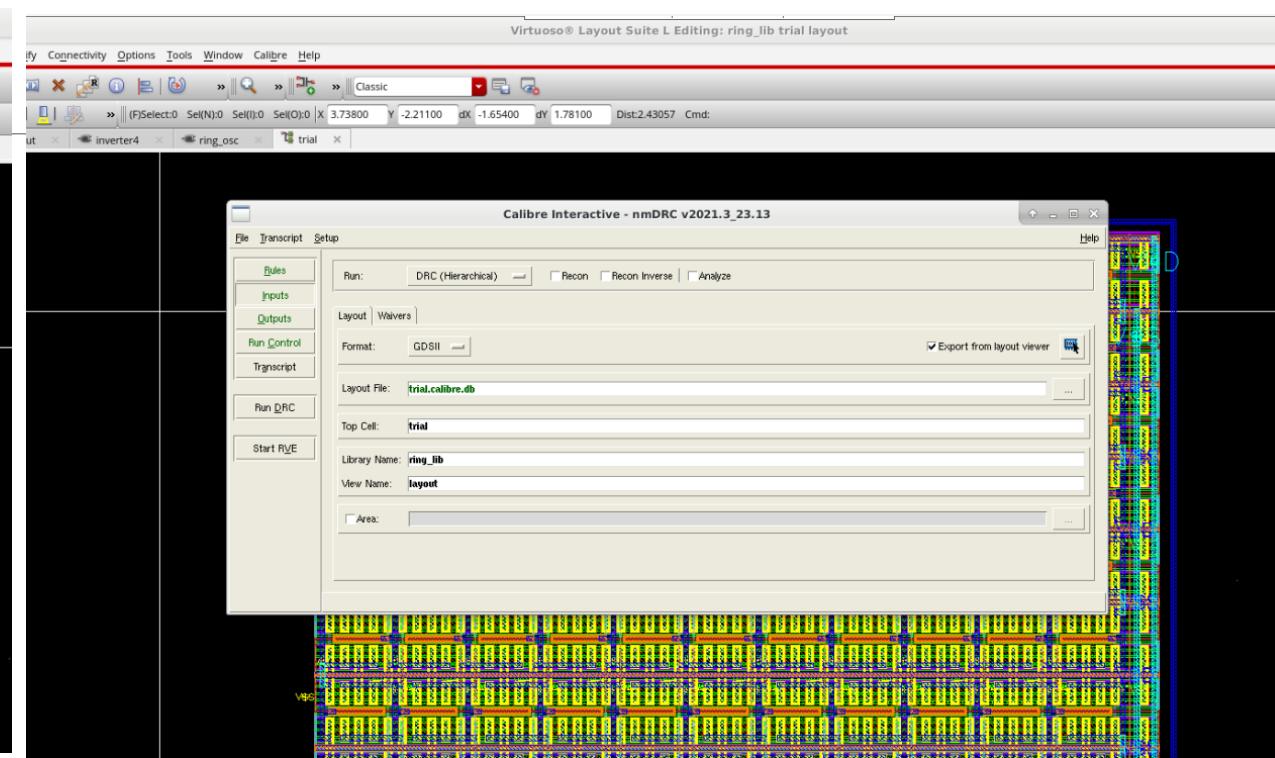


Fig 9: Drc layout file setting as input

DRC OUTPUT With all clear

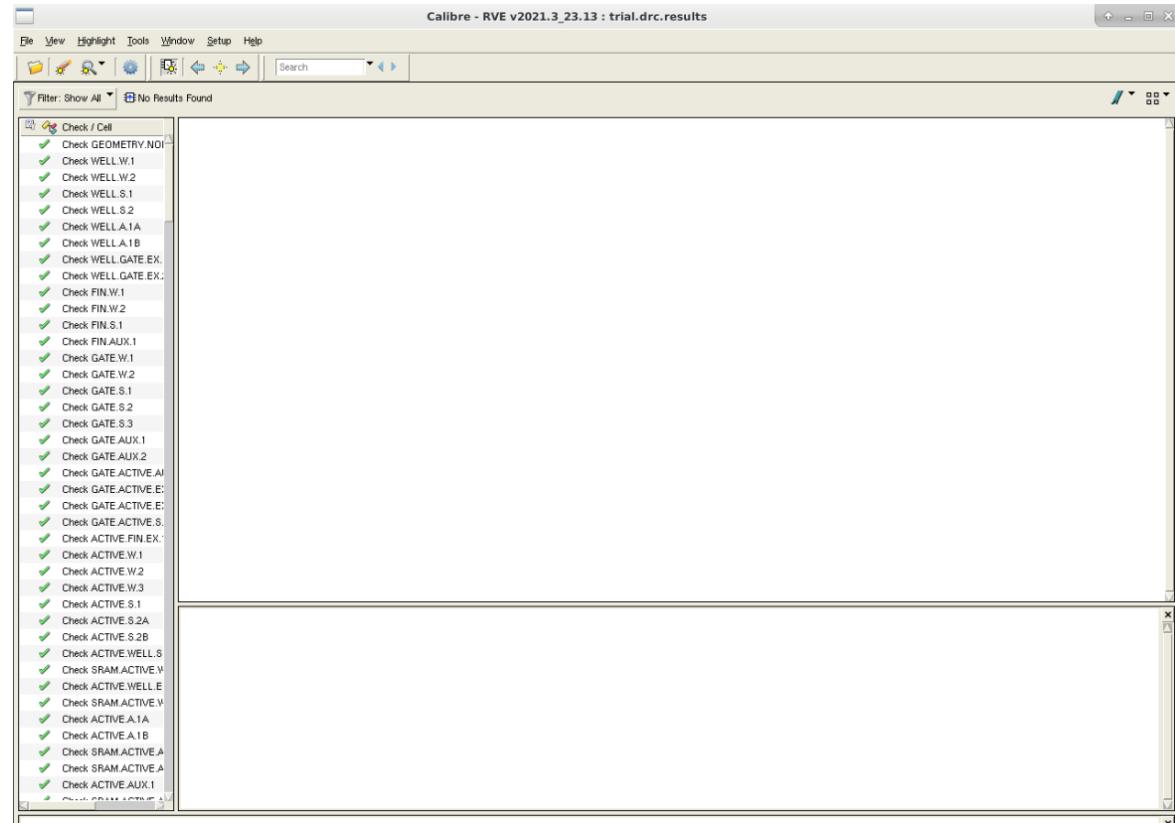


Fig 10: DRC clear

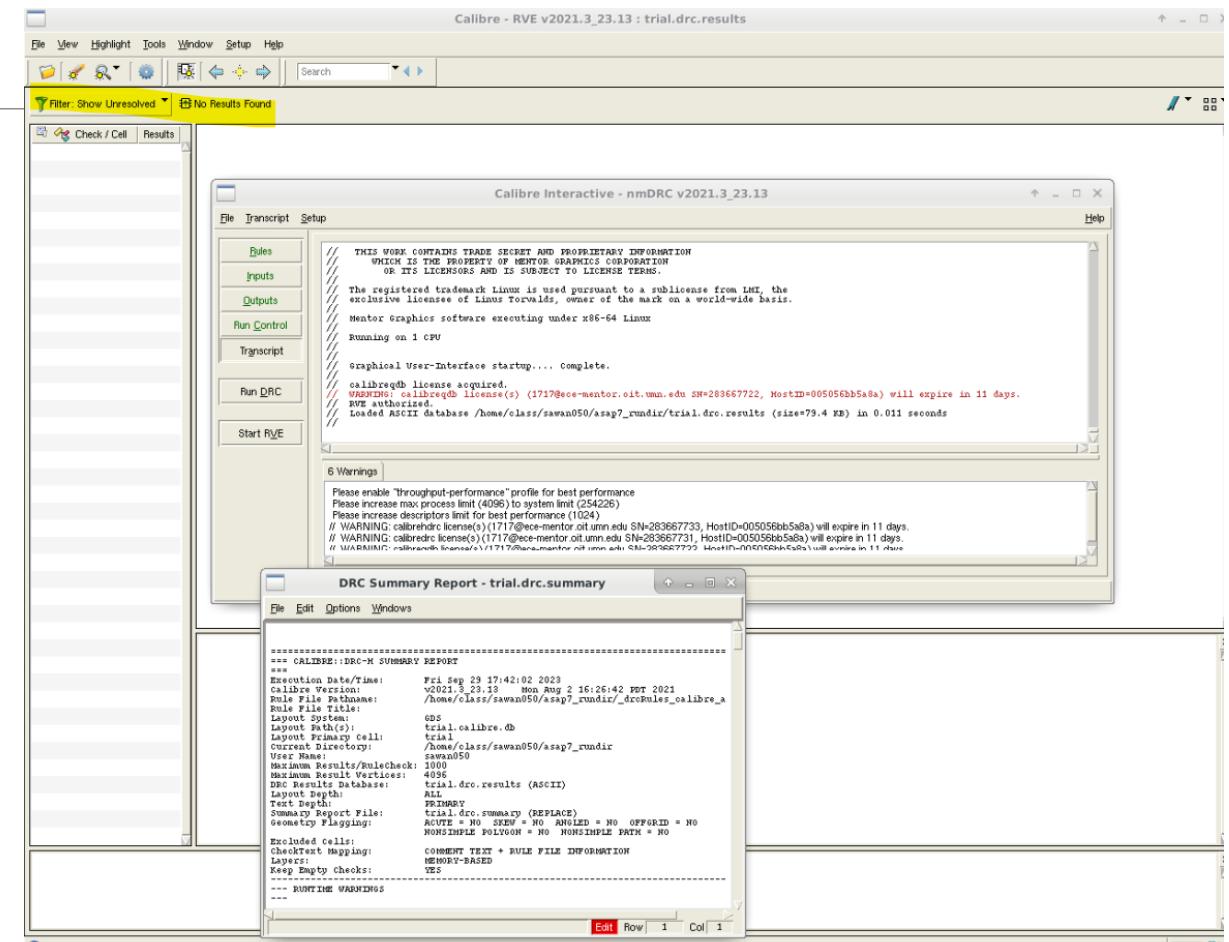


Fig 11: Drc clear for unresolved

Lvs steps

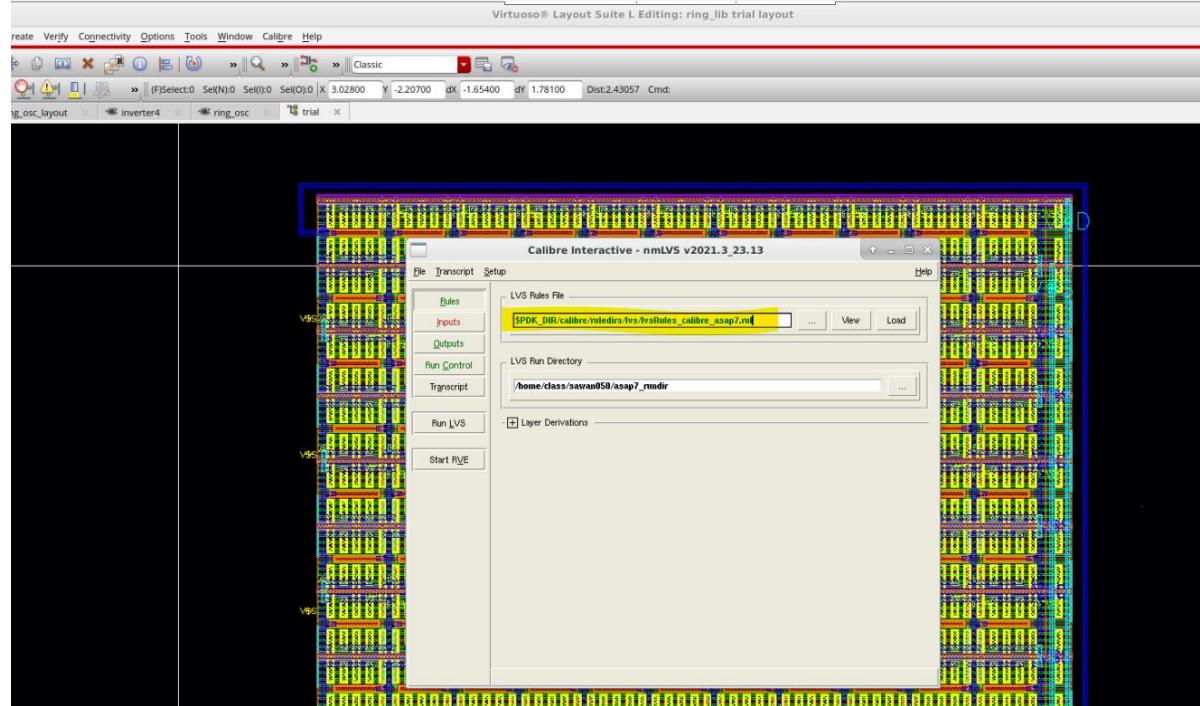


Fig 12: LVS rule file setting

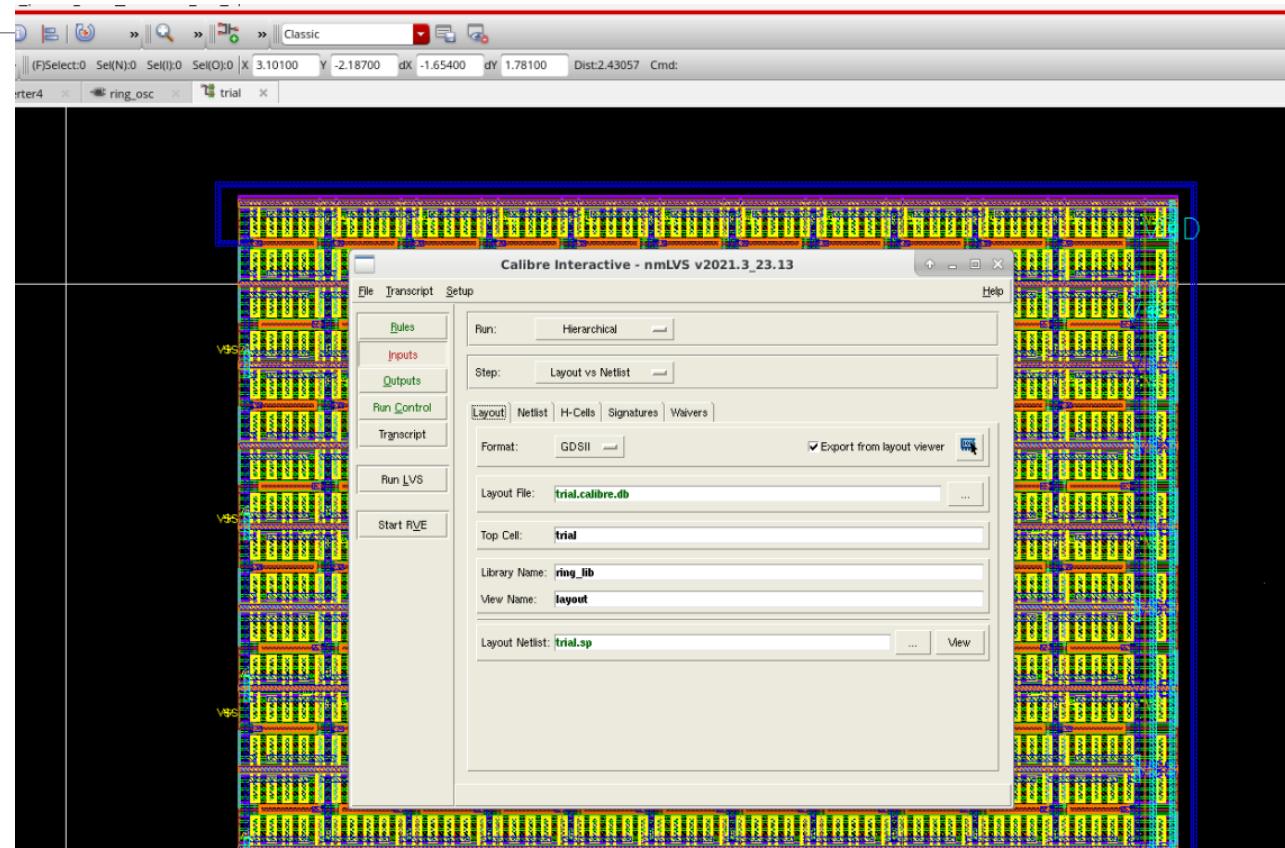


Fig 13: LVS input file layout setting path

LVS results with smiley face

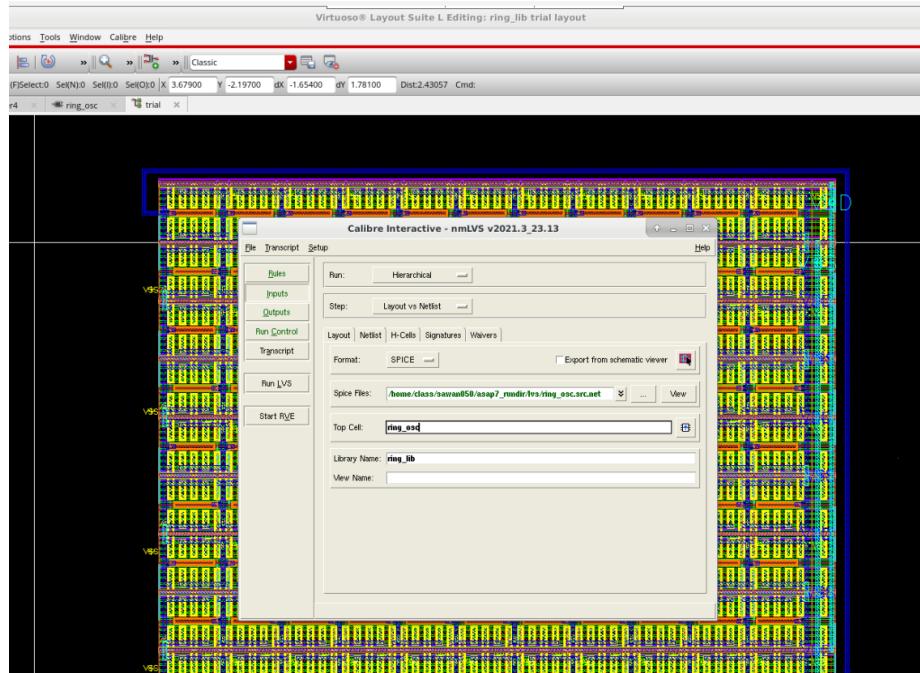


Fig 14: LVS input file netlist setting path

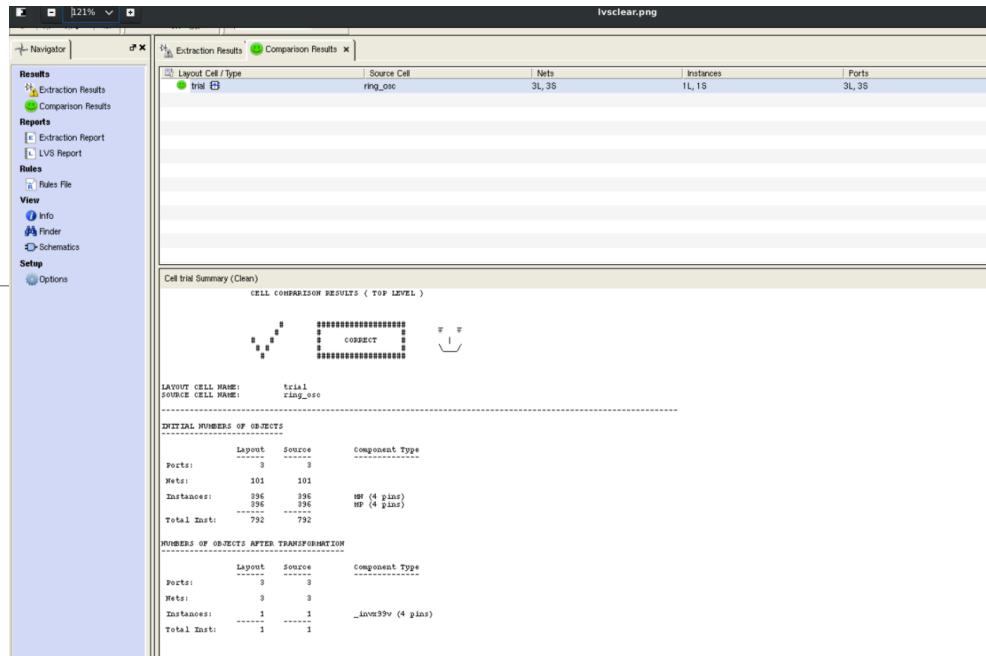


Fig 15: LVS clear with smiley face

```
File Edit Options Windows

#####
## C A L I B R E   S Y S T E M
## L V S   R E P O R T
##



REPORT FILE NAME: trial.lvs.report
LAYOUT NAME: /home/class/sawan050/asap7_rundir/trial.sp ('trial')
SOURCE NAME: /home/class/sawan050/asap7_rundir/_simulation/ring.sp (
RULE FILE: /home/class/sawan050/asap7_rundir/_lvsRules_calibre.as
RULE SET TITLE: LVS Rules File for ASAP7 PDK
CREATION TIME: Thu Sep 22 16:39:43 2023
CURRENT DIRECTORY: /home/class/sawan050/asap7_rundir
USER NAME: sawan050
CALIBRE VERSION: v2021.3_23.13 Mon Aug 2 16:26:42 PDT 2021

OVERALL COMPARISON RESULTS

Edit Row 1 Col 1
```

Fig 16: LVS report window

LVS smiley face result window

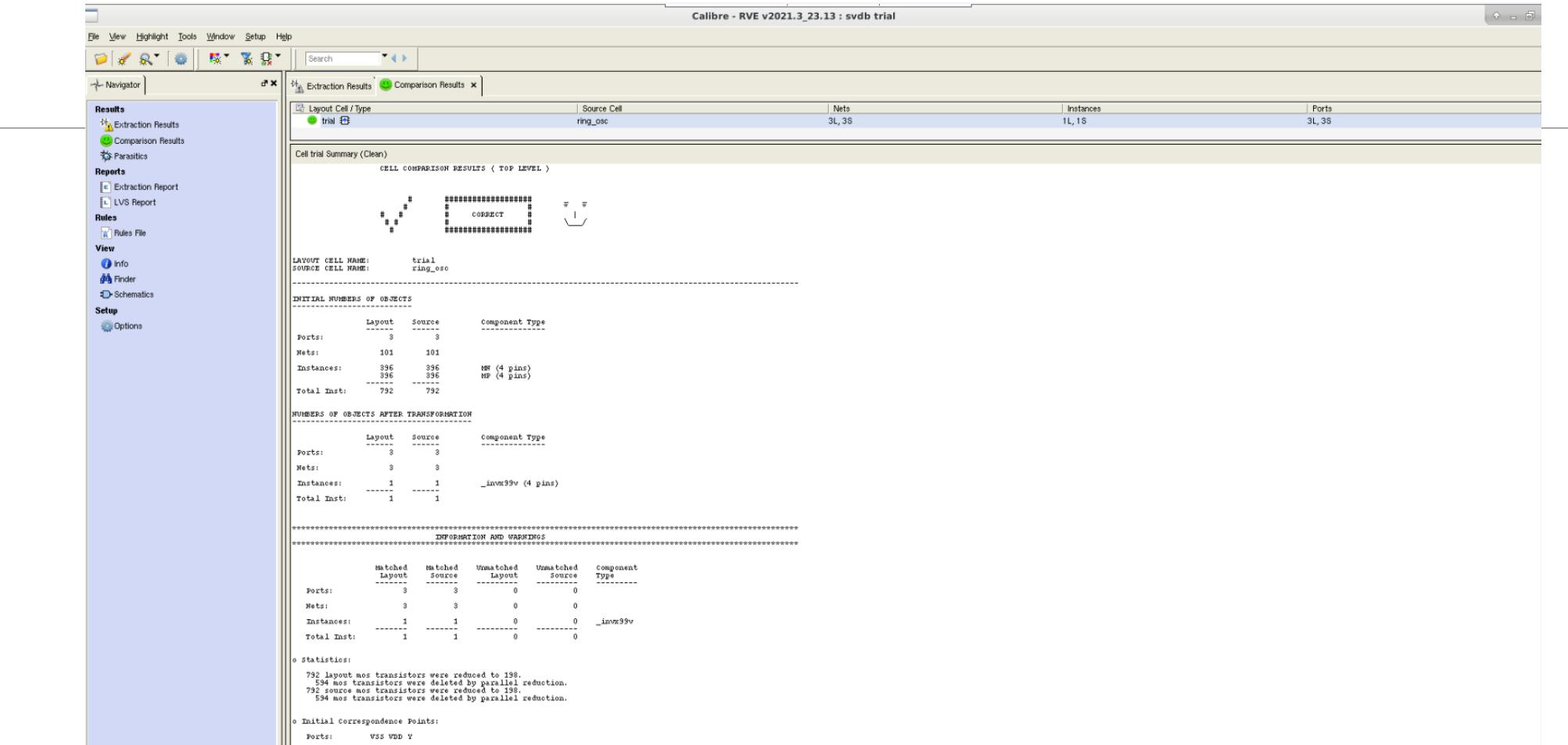


Fig 17: LVS result window with smiley

Pex file steps

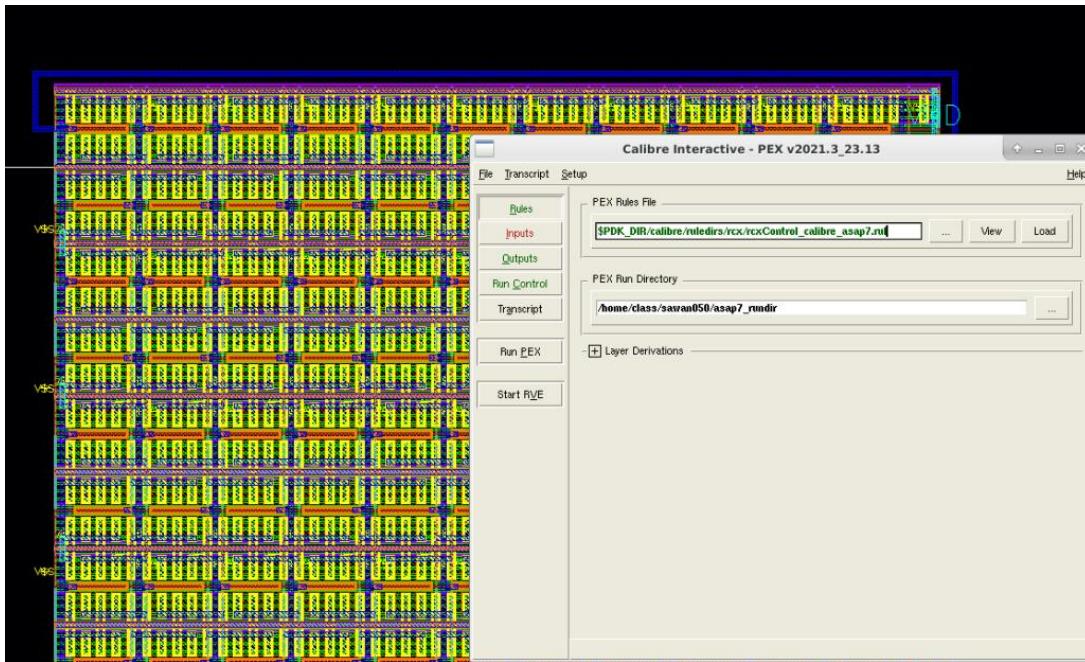


Fig 18: pex rule file setting the path

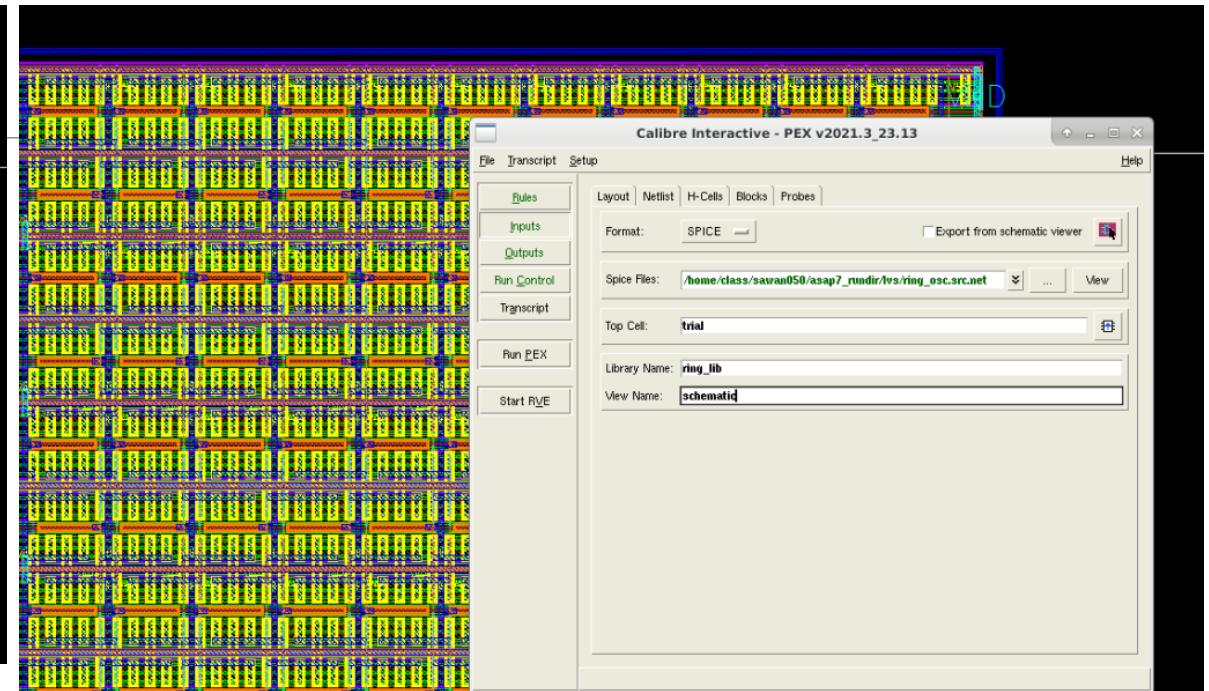


Fig 19: pex inputs to netlist file path setting

PEX file setting

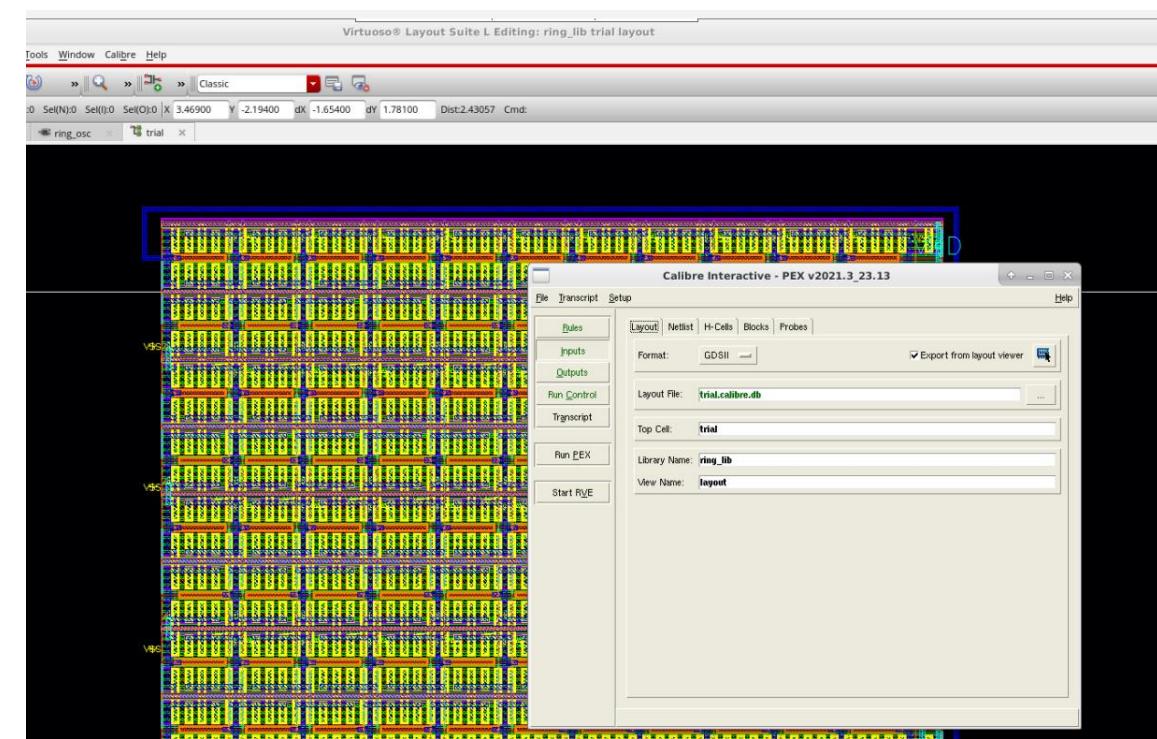


Fig 20: pex inputs to layout file path setting

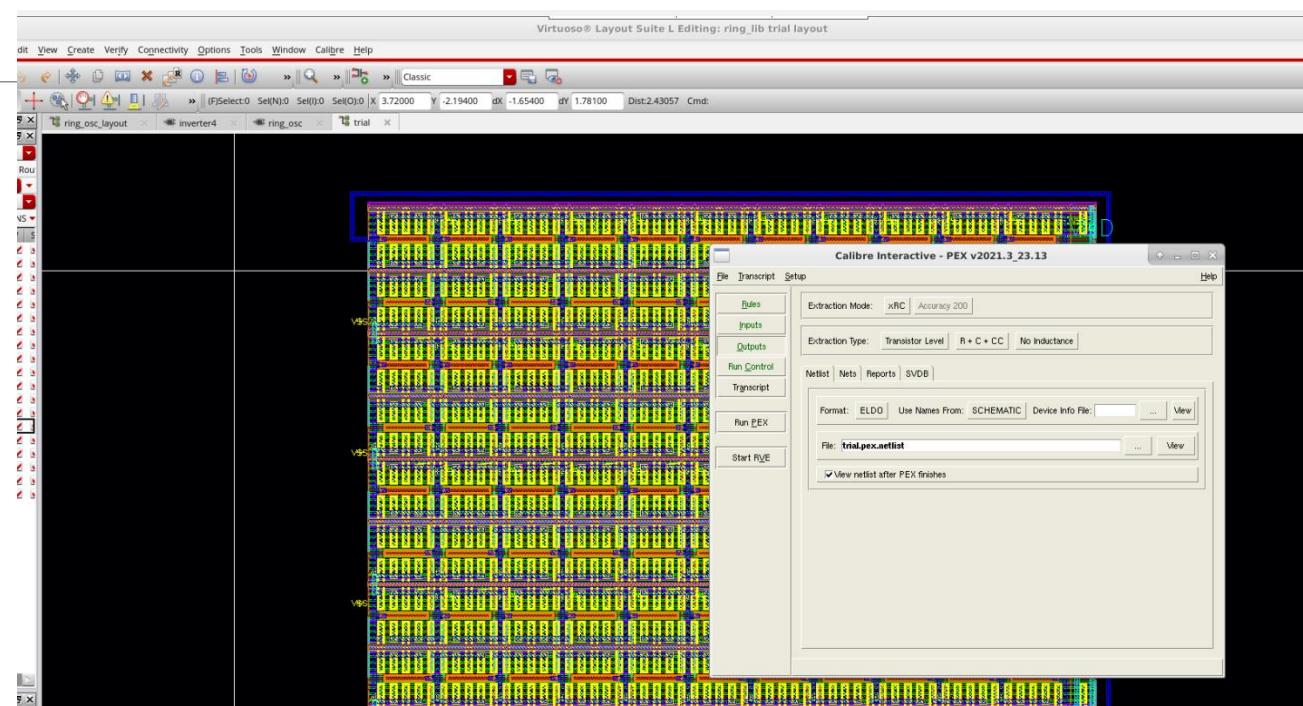
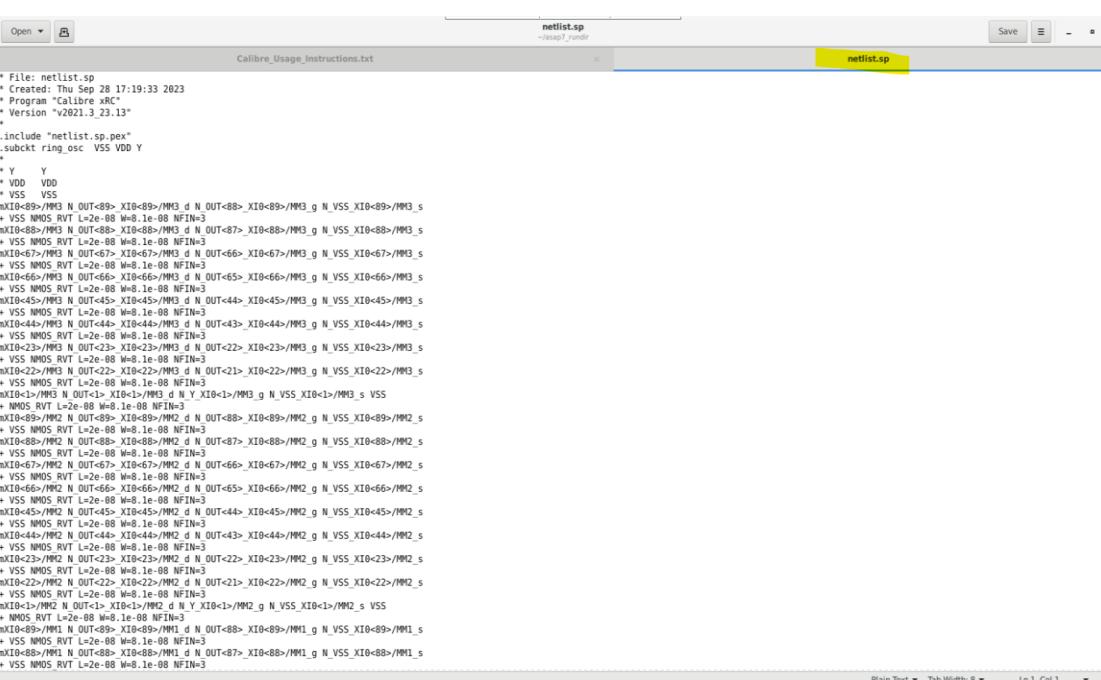


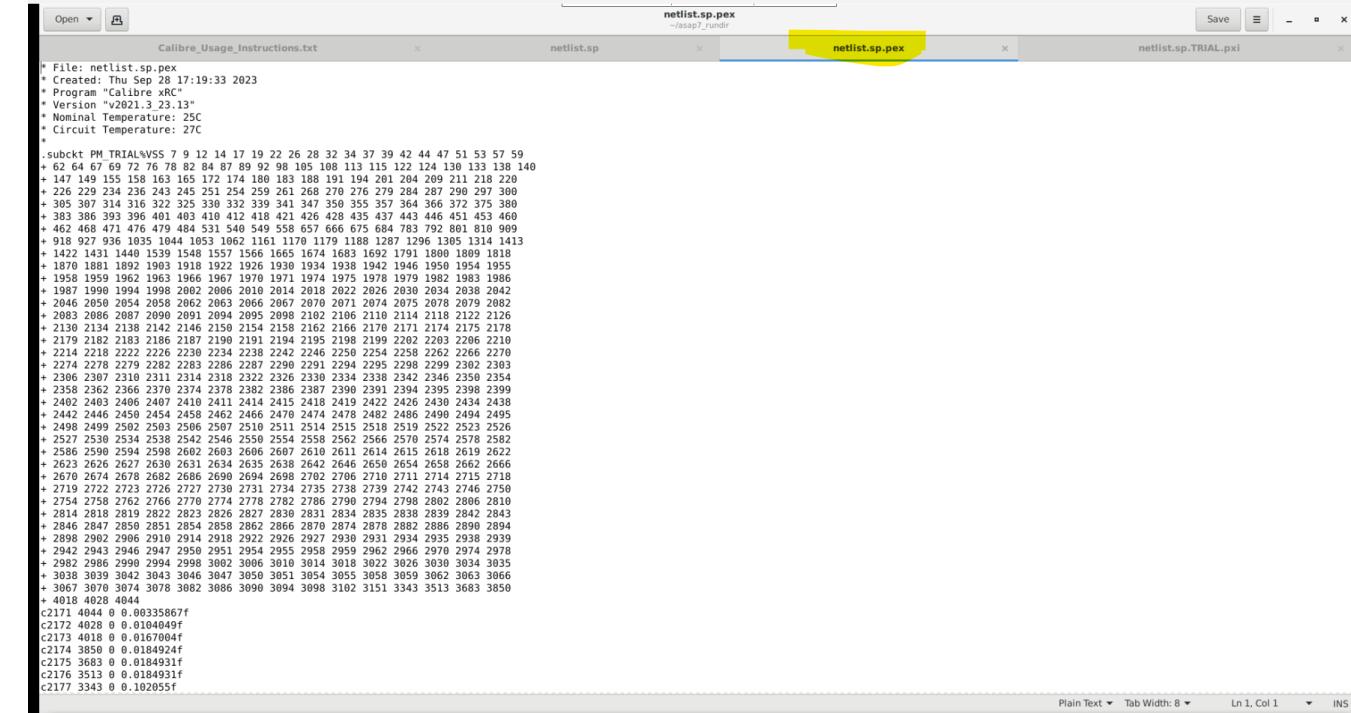
Fig 21: pex outputs file setting

PEX generated netlist.sp, netlist.sp.pex file before copying in simulation folder



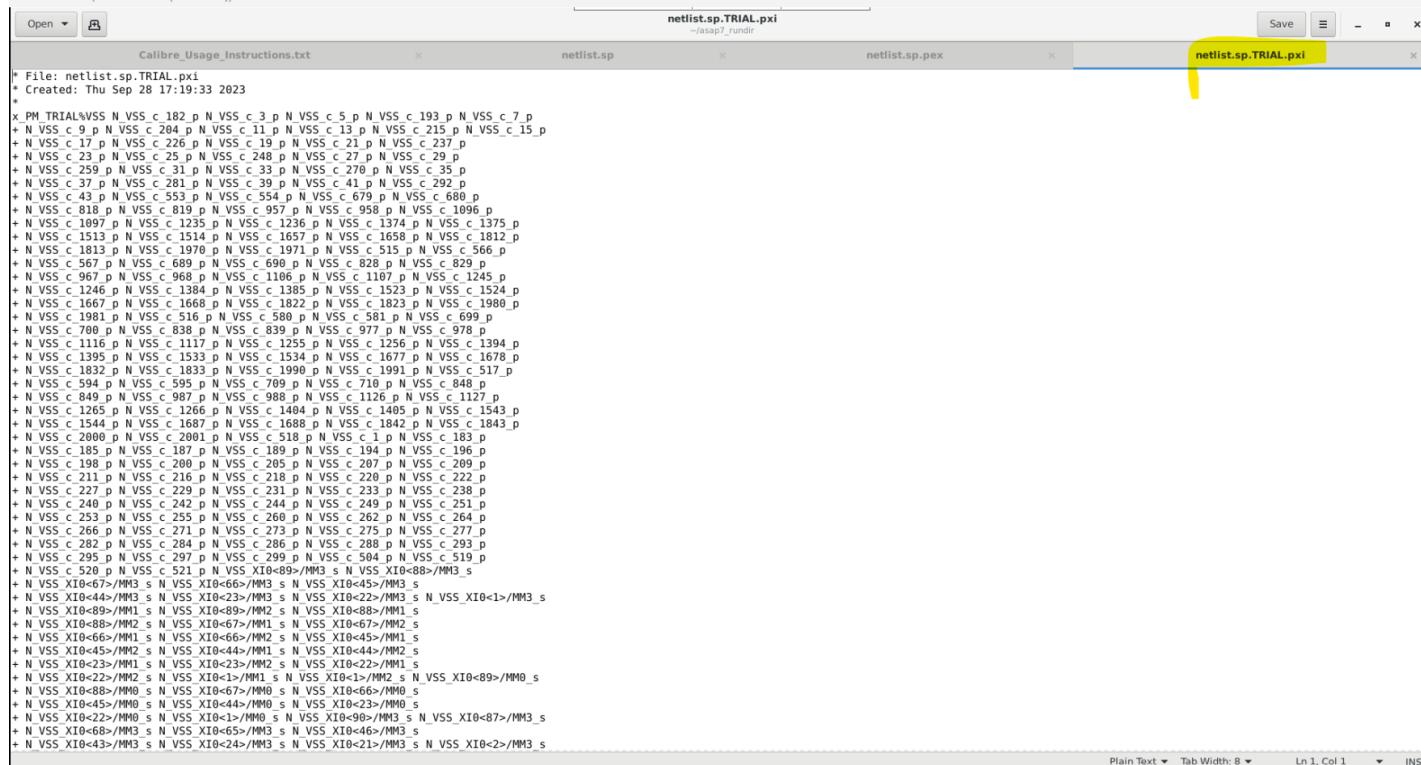
```
* File: netlist.sp
* Created: Thu Sep 28 17:19:33 2023
* Program "Calibre xrc"
* Version "v2021_3_23_13"
*
* include "netlist.sp.pex"
* subckt ring_osc VSS VDD Y
* Y
* VDD VDD
* VSS VSS
* VIO VIO
* VIO<88> N OUT<88> XIO<89>/MM3_d N OUT<88>_XIO<89>/MM3_g N_VSS_XIO<89>/MM3_s
* VSS NMOS RVT L=2e-08 W=8.1e-08 NFIN=3
* VIO<88>/MM3_d N OUT<88> XIO<88>/MM3_d N OUT<87> XIO<88>/MM3_g N_VSS_XIO<88>/MM3_s
* VSS NMOS RVT L=2e-08 W=8.1e-08 NFIN=3
* VIO<87>/MM3_d N OUT<87> XIO<87>/MM3_d N OUT<86> XIO<87>/MM3_g N_VSS_XIO<87>/MM3_s
* VSS NMOS RVT L=2e-08 W=8.1e-08 NFIN=3
* VIO<86>/MM3_d N OUT<86> XIO<86>/MM3_d N OUT<85> XIO<86>/MM3_g N_VSS_XIO<86>/MM3_s
* VSS NMOS RVT L=2e-08 W=8.1e-08 NFIN=3
* VIO<85>/MM3_d N OUT<85> XIO<85>/MM3_d N OUT<84> XIO<85>/MM3_g N_VSS_XIO<85>/MM3_s
* VSS NMOS RVT L=2e-08 W=8.1e-08 NFIN=3
* VIO<84>/MM3_d N OUT<84> XIO<84>/MM3_d N OUT<83> XIO<84>/MM3_g N_VSS_XIO<84>/MM3_s
* VIO<83>/MM3_d N OUT<83> XIO<83>/MM3_d N OUT<82> XIO<83>/MM3_g N_VSS_XIO<83>/MM3_s
* VSS NMOS RVT L=2e-08 W=8.1e-08 NFIN=3
* VIO<82>/MM3_d N OUT<82> XIO<82>/MM3_d N OUT<81> XIO<82>/MM3_g N_VSS_XIO<82>/MM3_s
* VSS NMOS RVT L=2e-08 W=8.1e-08 NFIN=3
* VIO<81>/MM3_d N OUT<81> XIO<81>/MM3_d N Y XIO<81>/MM3_g N_VSS_XIO<81>/MM3_s VSS
* NMOS RVT L=2e-08 W=8.1e-08 NFIN=3
* VIO<80>/MM3_d N OUT<80>/MM2_d N OUT<88> XIO<89>/MM2_g N_VSS_XIO<89>/MM2_s
* VSS NMOS RVT L=2e-08 W=8.1e-08 NFIN=3
* VIO<88>/MM2_d N OUT<88> XIO<88>/MM2_d N OUT<87> XIO<88>/MM2_g N_VSS_XIO<88>/MM2_s
* VSS NMOS RVT L=2e-08 W=8.1e-08 NFIN=3
* VIO<87>/MM2_d N OUT<87> XIO<87>/MM2_d N OUT<86> XIO<87>/MM2_g N_VSS_XIO<87>/MM2_s
* VSS NMOS RVT L=2e-08 W=8.1e-08 NFIN=3
* VIO<86>/MM2_d N OUT<86> XIO<86>/MM2_d N OUT<85> XIO<86>/MM2_g N_VSS_XIO<86>/MM2_s
* VSS NMOS RVT L=2e-08 W=8.1e-08 NFIN=3
* VIO<85>/MM2_d N OUT<85> XIO<85>/MM2_d N OUT<84> XIO<85>/MM2_g N_VSS_XIO<85>/MM2_s
* VSS NMOS RVT L=2e-08 W=8.1e-08 NFIN=3
* VIO<84>/MM2_d N OUT<84> XIO<84>/MM2_d N OUT<83> XIO<84>/MM2_g N_VSS_XIO<84>/MM2_s
* VSS NMOS RVT L=2e-08 W=8.1e-08 NFIN=3
* VIO<83>/MM2_d N OUT<83> XIO<83>/MM2_d N OUT<82> XIO<83>/MM2_g N_VSS_XIO<83>/MM2_s
* VSS NMOS RVT L=2e-08 W=8.1e-08 NFIN=3
* VIO<82>/MM2_d N OUT<82> XIO<82>/MM2_d N OUT<81> XIO<82>/MM2_g N_VSS_XIO<82>/MM2_s
* VSS NMOS RVT L=2e-08 W=8.1e-08 NFIN=3
* VIO<81>/MM2_d N OUT<81> XIO<81>/MM2_d N Y XIO<81>/MM2_g N_VSS_XIO<81>/MM2_s VSS
* NMOS RVT L=2e-08 W=8.1e-08 NFIN=3
* VIO<80>/MM2_d N OUT<80>/MM1_d N OUT<88> XIO<89>/MM1_g N_VSS_XIO<89>/MM1_s
* VSS NMOS RVT L=2e-08 W=8.1e-08 NFIN=3
* VIO<88>/MM1_d N OUT<88> XIO<88>/MM1_d N OUT<87> XIO<88>/MM1_g N_VSS_XIO<88>/MM1_s
* VSS NMOS RVT L=2e-08 W=8.1e-08 NFIN=3
```

Fig 22: pex generate netlist.sp file



```
* File: netlist_sp.pex
* Created: Thu Sep 28 17:19:33 2023
* Program "Calibre xrc"
* Version "v2021_3_23_13"
* Nominal Temperature: 25C
* Circuit Temperature: 27C
*
* subckt PM TRIAL\WVS 7 9 12 14 17 19 22 26 28 32 34 37 39 42 44 47 51 53 57 59
* 62 64 67 69 72 76 78 82 84 87 89 92 98 105 108 113 115 122 124 130 133 138 140
* 147 148 155 158 163 165 172 174 180 183 188 191 194 201 204 209 211 218 220
* 226 229 234 236 243 245 251 254 259 261 268 270 276 279 284 287 299 297 300
* 305 307 314 316 322 325 338 332 339 341 347 350 355 357 364 366 372 375 380
* 383 386 393 396 401 403 418 412 418 421 426 428 435 437 443 446 451 453 460
* 462 468 471 476 479 483 531 540 549 554 558 567 666 675 688 783 792 801 810 999
* 918 927 936 1033 1044 1053 1062 1161 1170 1178 1287 1296 1305 1313 1413
* 1522 1531 1541 1551 1561 1571 1581 1591 1601 1611 1621 1631 1641 1651 1661 1671
* 1681 1691 1701 1711 1721 1731 1741 1751 1761 1771 1781 1791 1801 1811
* 1870 1881 1892 1903 1918 1922 1928 1930 1934 1938 1942 1946 1950 1954 1955
* 1958 1959 1962 1963 1966 1967 1970 1971 1974 1975 1978 1979 1982 1983 1986
* 1987 1990 1994 1998 2002 2006 2010 2014 2018 2022 2026 2030 2034 2038 2042
* 2046 2050 2054 2058 2062 2063 2066 2067 2070 2071 2074 2075 2078 2079 2082
* 2083 2086 2087 2093 2091 2094 2095 2099 2102 2106 2110 2114 2118 2122 2126
* 2130 2134 2138 2142 2146 2150 2154 2158 2162 2166 2170 2171 2174 2175 2178
* 2179 2182 2183 2186 2187 2190 2193 2194 2195 2198 2199 2202 2203 2206 2210
* 2214 2218 2220 2224 2228 2234 2238 2244 2248 2252 2256 2261 2264 2268 2270
* 2279 2280 2282 2283 2284 2285 2286 2291 2294 2295 2298 2300 2302 2303
* 2306 2307 2310 2311 2314 2318 2322 2326 2330 2334 2342 2346 2358 2354
* 2358 2362 2366 2370 2374 2378 2382 2386 2387 2399 2391 2394 2395 2398 2399
* 2402 2403 2406 2407 2410 2411 2414 2415 2418 2419 2422 2426 2430 2434 2438
* 2442 2446 2450 2454 2458 2462 2466 2474 2474 2478 2482 2486 2494 2494 2495
* 2494 2499 2508 2503 2506 2507 2510 2514 2514 2515 2518 2519 2522 2523 2526
* 2527 2530 2534 2538 2542 2546 2550 2554 2558 2562 2566 2570 2574 2578 2582
* 2583 2587 2591 2595 2599 2603 2607 2611 2615 2619 2623 2627 2631 2635 2639 2644
* 2645 2654 2658 2662 2666 2670 2674 2678 2682 2690 2694 2698 2702 2706 2711 2714 2715 2718
* 2719 2722 2723 2726 2727 2730 2734 2735 2738 2739 2742 2743 2746 2750
* 2754 2758 2762 2766 2770 2774 2778 2782 2786 2790 2794 2798 2802 2808
* 2814 2818 2819 2822 2823 2826 2827 2830 2831 2834 2834 2835 2838 2842 2843
* 2844 2847 2850 2851 2854 2858 2862 2866 2870 2874 2878 2882 2886 2898 2894
* 2898 2902 2906 2910 2914 2918 2922 2927 2930 2931 2934 2935 2938 2939
* 2942 2945 2946 2947 2949 2951 2952 2955 2958 2959 2962 2966 2970 2974 2978
* 2981 2986 2994 2998 3003 3006 3010 3014 3018 3022 3026 3030 3034 3035
* 3038 3039 3042 3043 3046 3047 3051 3054 3055 3056 3063 3066
* 3067 3070 3074 3078 3082 3086 3098 3102 3104 3108 3112 3116 3120 3124
* 3127 3131 3135 3137 3141 3145 3149 3153 3157 3161 3165 3169 3173 3177
* 3179 3183 3187 3191 3195 3199 3203 3207 3211 3215 3219 3223 3227 3231
* 3235 3239 3243 3247 3251 3255 3259 3263 3267 3271 3275 3279 3283
* 3287 3291 3295 3299 3303 3307 3311 3315 3319 3323 3327 3331 3335
* 3339 3343 3347 3351 3355 3359 3363 3367 3371 3375 3379 3383 3387
* 3391 3395 3399 3403 3407 3411 3415 3419 3423 3427 3431 3435 3439
* 3443 3447 3451 3455 3459 3463 3467 3471 3475 3479 3483 3487 3491
* 3495 3499 3503 3507 3511 3515 3519 3523 3527 3531 3535 3539 3543 3547
* 3551 3555 3559 3563 3567 3571 3575 3579 3583 3587 3591 3595 3599 3603
* 3607 3611 3615 3619 3623 3627 3631 3635 3639 3643 3647 3651 3655 3659
* 3663 3667 3671 3675 3679 3683 3687 3691 3695 3699 3703 3707 3711
* 3715 3719 3723 3727 3731 3735 3739 3743 3747 3751 3755 3759 3763 3767
* 3771 3775 3779 3783 3787 3791 3795 3799 3803 3807 3811 3815 3819 3823
* 3827 3831 3835 3839 3843 3847 3851 3855 3859 3863 3867 3871 3875
* 3879 3883 3887 3891 3895 3899 3903 3907 3911 3915 3919 3923 3927
* 3931 3935 3939 3943 3947 3951 3955 3959 3963 3967 3971 3975 3979
* 3983 3987 3991 3995 3999 4003 4007 4011 4015 4019 4023 4027 4031
* 4035 4039 4043 4047 4051 4055 4059 4063 4067 4071 4075 4079 4083
* 4087 4091 4095 4099 4103 4107 4111 4115 4119 4123 4127 4131 4135
* 4139 4143 4147 4151 4155 4159 4163 4167 4171 4175 4179 4183 4187
* 4191 4195 4199 4203 4207 4211 4215 4219 4223 4227 4231 4235 4239
* 4243 4247 4251 4255 4259 4263 4267 4271 4275 4279 4283 4287
* 4291 4295 4299 4303 4307 4311 4315 4319 4323 4327 4331 4335 4339
* 4343 4347 4351 4355 4359 4363 4367 4371 4375 4379 4383 4387 4391
* 4395 4399 4403 4407 4411 4415 4419 4423 4427 4431 4435 4439 4443
* 4447 4451 4455 4459 4463 4467 4471 4475 4479 4483 4487 4491 4495
* 4499 4503 4507 4511 4515 4519 4523 4527 4531 4535 4539 4543 4547
* 4551 4555 4559 4563 4567 4571 4575 4579 4583 4587 4591 4595 4599
* 4603 4607 4611 4615 4619 4623 4627 4631 4635 4639 4643 4647
* 4651 4655 4659 4663 4667 4671 4675 4679 4683 4687 4691 4695 4699
* 4703 4707 4711 4715 4719 4723 4727 4731 4735 4739 4743 4747 4751
* 4755 4759 4763 4767 4771 4775 4779 4783 4787 4791 4795 4799 4803
* 4807 4811 4815 4819 4823 4827 4831 4835 4839 4843 4847 4851 4855
* 4859 4863 4867 4871 4875 4879 4883 4887 4891 4895 4899 4903 4907
* 4911 4915 4919 4923 4927 4931 4935 4939 4943 4947 4951 4955 4959
* 4963 4967 4971 4975 4979 4983 4987 4991 4995 4999 5003 5007
* 5011 5015 5019 5023 5027 5031 5035 5039 5043 5047 5051 5055 5059
* 5063 5067 5071 5075 5079 5083 5087 5091 5095 5099 5103 5107 5111
* 5115 5119 5123 5127 5131 5135 5139 5143 5147 5151 5155 5159 5163
* 5167 5171 5175 5179 5183 5187 5191 5195 5199 5203 5207 5211 5215
* 5219 5223 5227 5231 5235 5239 5243 5247 5251 5255 5259 5263 5267
* 5271 5275 5279 5283 5287 5291 5295 5299 5303 5307 5311 5315 5319
* 5323 5327 5331 5335 5339 5343 5347 5351 5355 5359 5363 5367 5371
* 5375 5379 5383 5387 5391 5395 5399 5403 5407 5411 5415 5419 5423
* 5427 5431 5435 5439 5443 5447 5451 5455 5459 5463 5467 5471 5475
* 5479 5483 5487 5491 5495 5499 5503 5507 5511 5515 5519 5523 5527
* 5531 5535 5539 5543 5547 5551 5555 5559 5563 5567 5571 5575 5579
* 5583 5587 5591 5595 5599 5603 5607 5611 5615 5619 5623 5627 5631
* 5635 5639 5643 5647 5651 5655 5659 5663 5667 5671 5675 5679 5683
* 5687 5691 5695 5699 5703 5707 5711 5715 5719 5723 5727 5731 5735
* 5739 5743 5747 5751 5755 5759 5763 5767 5771 5775 5779 5783 5787
* 5791 5795 5799 5803 5807 5811 5815 5819 5823 5827 5831 5835 5839
* 5843 5847 5851 5855 5859 5863 5867 5871 5875 5879 5883 5887 5891
* 5895 5899 5903 5907 5911 5915 5919 5923 5927 5931 5935 5939 5943
* 5947 5951 5955 5959 5963 5967 5971 5975 5979 5983 5987 5991 5995
* 5999 6003 6007 6011 6015 6019 6023 6027 6031 6035 6039 6043 6047
* 6051 6055 6059 6063 6067 6071 6075 6079 6083 6087 6091 6095 6099
* 6103 6107 6111 6115 6119 6123 6127 6131 6135 6139 6143 6147 6151
* 6155 6159 6163 6167 6171 6175 6179 6183 6187 6191 6195 6199 6203
* 6207 6211 6215 6219 6223 6227 6231 6235 6239 6243 6247 6251 6255
* 6259 6263 6267 6271 6275 6279 6283 6287 6291 6295 6299 6303 6307
* 6311 6315 6319 6323 6327 6331 6335 6339 6343 6347 6351 6355 6359
* 6363 6367 6371 6375 6379 6383 6387 6391 6395 6399 6403 6407 6411
* 6415 6419 6423 6427 6431 6435 6439 6443 6447 6451 6455 6459 6463
* 6467 6471 6475 6479 6483 6487 6491 6495 6499 6503 6507 6511 6515
* 6519 6523 6527 6531 6535 6539 6543 6547 6551 6555 6559 6563 6567
* 6571 6575 6579 6583 6587 6591 6595 6599 6603 6607 6611 6615 6619
* 6623 6627 6631 6635 6639 6643 6647 6651 6655 6659 6663 6667 6671
* 6675 6679 6683 6687 6691 6695 6699 6703 6707 6711 6715 6719 6723
* 6727 6731 6735 6739 6743 6747 6751 6755 6759 6763 6767 6771 6775
* 6779 6783 6787 6791 6795 6799 6803 6807 6811 6815 6819 6823 6827
* 6829 6833 6837 6841 6845 6849 6853 6857 6861 6865 6869 6873 6877
* 6881 6885 6889 6893 6897 6901 6905 6909 6913 6917 6921 6925 6929
* 6933 6937 6941 6945 6949 6953 6957 6961 6965 6969 6973 6977 6981
* 6985 6989 6993 6997 6999 7003 7007 7011 7015 7019 7023 7027 7031
* 7035 7039 7043 7047 7051 7055 7059 7063 7067 7071 7075 7079 7083
* 7087 7091 7095 7099 7103 7107 7111 7115 7119 7123 7127 7131 7135
* 7139 7143 7147 7151 7155 7159 7163 7167 7171 7175 7179 7183 7187
* 7191 7195 7199 7203 7207 7211 7215 7219 7223 7227 7231 7235 7239
* 7243 7247 7251 7255 7259 7263 7267 7271 7275 7279 7283 7287 7291
* 7295 7299 7303 7307 7311 7315 7319 7323 7327 7331 7335 7339 7343
* 7347 7351 7355 7359 7363 7367 7371 7375 7379 7383 7387 7391 7395
* 7399 7403 7407 7411 7415 7419 7423 7427 7431 7435 7439 7443 7447
* 7451 7455 7459 7463 7467 7471 7475 7479 7483 7487 7491 7495 7499
* 7503 7507 7511 7515 7519 7523 7527 7531 7535 7539 7543 7547 7551
* 7555 7559 7563 7567 7571 7575 7579 7583 7587 7591 7595 7599 7603
* 7607 7611 7615 7619 7623 7627 7631 7635 7639 7643 7647 7651 7655
* 7659 7663 7667 7671 7675 7679 7683 7687 7691 7695 7699 7703 7707
* 7711 7715 7719 7723 7727 7731 7735 7739 7743 7747 7751 7755 7759
* 7763 7767 7771 7775 7779 7783 7787 7791 7795 7799 7803 7807 7811
* 7815 7
```

PEX generated netlist.sp.TRIAL.pkl before copying in simulation folder



```
* File: netlist.sp.TRIAL.pkl
* Created: Thu Sep 28 17:19:33 2023
*
+ P0 TRIAL%VSS N VSS c_182 p N VSS c_3_p N VSS c_5_p N VSS c_193 p N VSS c_7_p
+ N VSS c_9_p N VSS c_284 p N VSS c_11_p N VSS c_13_p N VSS c_215 p N VSS c_15_p
+ N VSS c_17_p N VSS c_226_p N VSS c_19_p N VSS c_21_p N VSS c_237_p
+ N VSS c_23_p N VSS c_25_p N VSS c_248_p N VSS c_27_p N VSS c_29_p
+ N VSS c_259_p N VSS c_31_p N VSS c_33_p N VSS c_278_p N VSS c_35_p
+ N VSS c_37_p N VSS c_281_p N VSS c_39_p N VSS c_41_p N VSS c_292_p
+ N VSS c_43_p N VSS c_553_p N VSS c_555_p N VSS c_679_p N VSS c_688_p
+ N VSS c_818_p N VSS c_818_p N VSS c_957_p N VSS c_958_p N VSS c_1096_p
+ N VSS c_1099_p N VSS c_1235_p N VSS c_1236_p N VSS c_1374_p N VSS c_1375_p
+ N VSS c_152_p N VSS c_1512_p N VSS c_1651_p N VSS c_1658_p N VSS c_1812_p
+ N VSS c_1813_p N VSS c_1970_p N VSS c_1971_p N VSS c_515_p N VSS c_566_p
+ N VSS c_567_p N VSS c_689_p N VSS c_690_p N VSS c_828_p N VSS c_829_p
+ N VSS c_967_p N VSS c_968_p N VSS c_1106_p N VSS c_1107_p N VSS c_1245_p
+ N VSS c_1246_p N VSS c_1384_p N VSS c_1385_p N VSS c_1523_p N VSS c_1524_p
+ N VSS c_1667_p N VSS c_1668_p N VSS c_1822_p N VSS c_1823_p N VSS c_1980_p
+ N VSS c_1981_p N VSS c_516_p N VSS c_580_p N VSS c_581_p N VSS c_699_p
+ N VSS c_790_p N VSS c_838_p N VSS c_839_p N VSS c_977_p N VSS c_978_p
+ N VSS c_1116_p N VSS c_1117_p N VSS c_1255_p N VSS c_1256_p N VSS c_1394_p
+ N VSS c_1395_p N VSS c_1533_p N VSS c_1534_p N VSS c_1677_p N VSS c_1678_p
+ N VSS c_1832_p N VSS c_1833_p N VSS c_1994_p N VSS c_1991_p N VSS c_517_p
+ N VSS c_594_p N VSS c_595_p N VSS c_709_p N VSS c_718_p N VSS c_848_p
+ N VSS c_849_p N VSS c_987_p N VSS c_988_p N VSS c_1126_p N VSS c_1127_p
+ N VSS c_1265_p N VSS c_1266_p N VSS c_1404_p N VSS c_1495_p N VSS c_1543_p
+ N VSS c_1544_p N VSS c_1687_p N VSS c_1688_p N VSS c_1842_p N VSS c_1843_p
+ N VSS c_2000_p N VSS c_2001_p N VSS c_518_p N VSS c_1_p N VSS c_183_p
+ N VSS c_185_p N VSS c_187_p N VSS c_189_p N VSS c_194_p N VSS c_196_p
+ N VSS c_193_p N VSS c_208_p N VSS c_205_p N VSS c_207_p N VSS c_209_p
+ N VSS c_211_p N VSS c_216_p N VSS c_218_p N VSS c_220_p N VSS c_222_p
+ N VSS c_227_p N VSS c_228_p N VSS c_231_p N VSS c_233_p N VSS c_238_p
+ N VSS c_240_p N VSS c_242_p N VSS c_243_p N VSS c_251_p N VSS c_253_p
+ N VSS c_253_p N VSS c_255_p N VSS c_266_p N VSS c_262_p N VSS c_264_p
+ N VSS c_266_p N VSS c_271_p N VSS c_273_p N VSS c_275_p N VSS c_277_p
+ N VSS c_282_p N VSS c_284_p N VSS c_286_p N VSS c_288_p N VSS c_293_p
+ N VSS c_295_p N VSS c_297_p N VSS c_299_p N VSS c_504_p N VSS c_519_p
+ N VSS c_520_p N VSS c_521_p N VSS XI0<89>/MM3_s N VSS XI0<88>/MM3_s
+ N VSS XI0<67>/MM3_s N VSS XI0<66>/MM3_s N VSS XI0<23>/MM3_s N VSS XI0<1>/MM3_s
+ N VSS XI0<44>/MM3_s N VSS XI0<23>/MM3_s N VSS XI0<22>/MM3_s N VSS XI0<1>/MM3_s
+ N VSS XI0<89>/MM1_s N VSS XI0<89>/MM2_s N VSS XI0<88>/MM1_s
+ N VSS XI0<88>/MM2_s N VSS XI0<67>/MM1_s N VSS XI0<67>/MM2_s
+ N VSS XI0<66>/MM1_s N VSS XI0<66>/MM2_s N VSS XI0<45>/MM1_s
+ N VSS XI0<45>/MM2_s N VSS XI0<44>/MM1_s N VSS XI0<44>/MM2_s
+ N VSS XI0<23>/MM1_s N VSS XI0<23>/MM2_s N VSS XI0<22>/MM1_s
+ N VSS XI0<22>/MM2_s N VSS XI0<1>/MM1_s N VSS XI0<1>/MM2_s N VSS XI0<89>/MM0_s
+ N VSS XI0<88>/MM0_s N VSS XI0<67>/MM0_s N VSS XI0<66>/MM0_s
+ N VSS XI0<45>/MM0_s N VSS XI0<44>/MM0_s N VSS XI0<23>/MM0_s
+ N VSS XI0<22>/MM0_s N VSS XI0<1>/MM0_s N VSS XI0<98>/MM3_s N VSS XI0<87>/MM3_s
+ N VSS XI0<68>/MM3_s N VSS XI0<65>/MM3_s N VSS XI0<46>/MM3_s
+ N VSS XI0<43>/MM3_s N VSS XI0<24>/MM3_s N VSS XI0<21>/MM3_s N VSS XI0<2>/MM3_s
```

Fig 24: pex generated netlist.sp.TRIAL.pkl

Copied pex generated from this path
`/home/class/sawan050/asap7_rundir/` to simulation folder and
commented the netlist.sp .subckt and .End part in the file

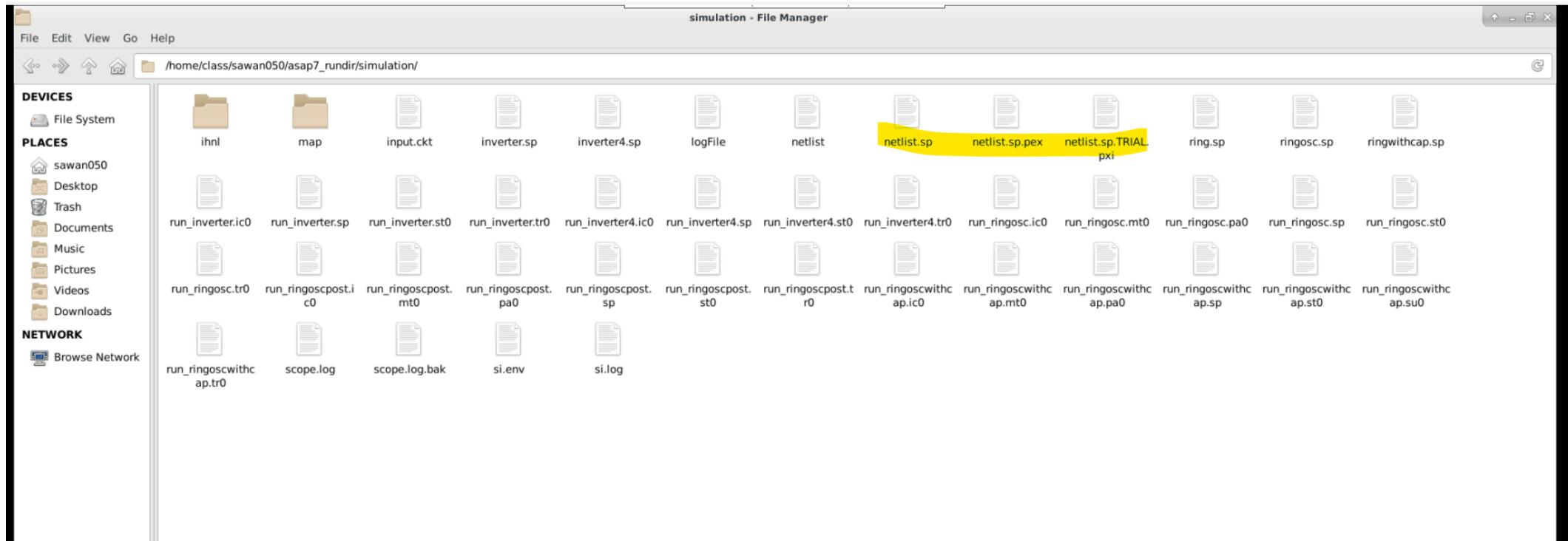


Fig 25: pex saving in the simulation folder and editing the code

Pre layout Analysis

Process corner = TT (typical, i.e. nominal), VDD = 0.7V (-10% VDD),
Temperature = 25°C (nominal),

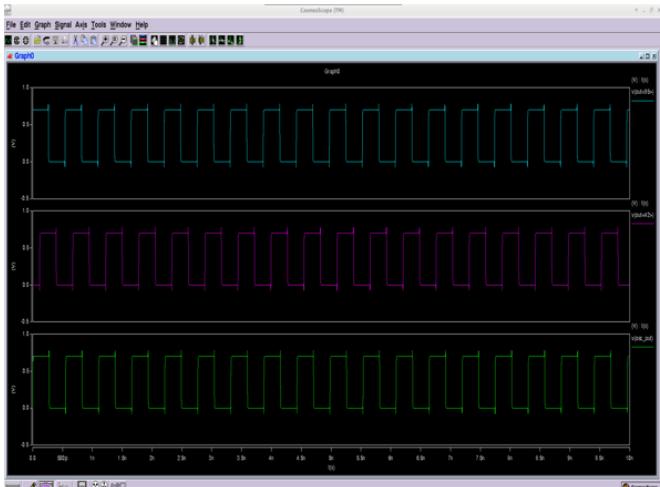


Fig 22: Process corner = TT (typical, i.e. nominal), VDD = 0.7V (-10% VDD), Temperature = 25°C (nominal),

```
File Edit View Search Terminal Help  
** run inverter file  
  
***** transient analysis tnom= 25.000 temp= 25.000 *****  
period= 5.5464e-10 targ= 1.6636e-09 trig= 1.1090e-09  
frequency= 1.8030e+09  
iave=-2.3484e-04 from= 0.0000e+00 to= 1.0000e-08  
power=-1.6439e-04  
  
***** job concluded  
  
***** job statistics summary tnom= 25.000 temp= 25.000 *****
```

Fig 23: freq = 1.803 GHz , Power = -1.6439e-4 W

Using the inverter4 symbol created earlier in ring_lib to use in ring_osc schematic

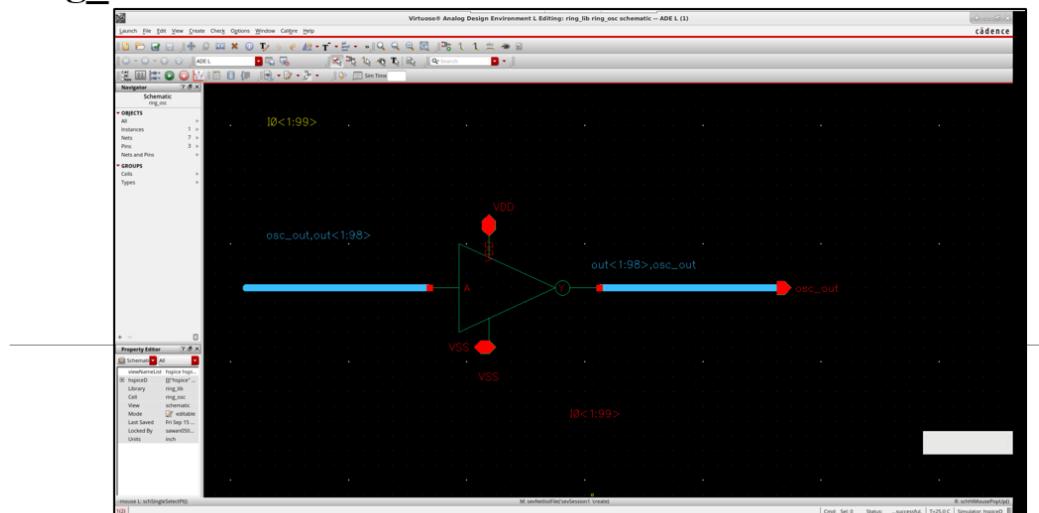
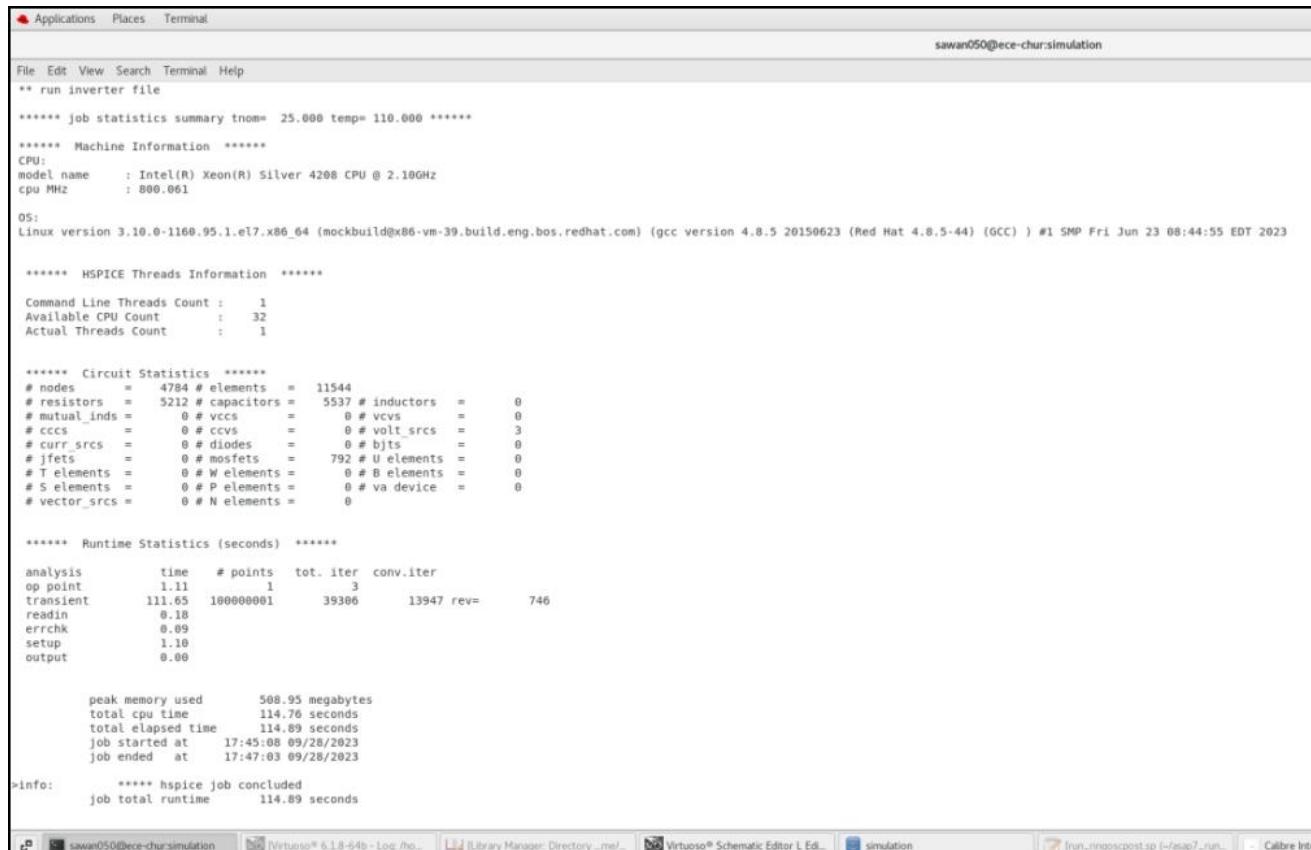


Fig 6: Creating in Library ring.lib schematic for 99 stage ring oscillator

Hspice ran for simulating



The screenshot shows a terminal window titled "sawan050@ece-chur:simulation". The window displays the output of a Hspice simulation command. The output includes job statistics, machine information, HSPICE threads information, circuit statistics, runtime statistics, and memory usage details. The simulation concluded successfully after 114.89 seconds.

```
** run inverter file
***** job statistics summary tnom= 25.000 temp= 110.000 *****
***** Machine Information *****
CPU:
model name      : Intel(R) Xeon(R) Silver 4208 CPU @ 2.10GHz
cpu MHz         : 800.061

OS:
Linux version 3.10.0-1160.95.1.el7.x86_64 (mockbuild@x86-vm-39.build.eng.bos.redhat.com) (gcc version 4.8.5 20150623 (Red Hat 4.8.5-44) (GCC) ) #1 SMP Fri Jun 23 08:44:55 EDT 2023

***** HSPICE Threads Information *****
Command Line Threads Count : 1
Available CPU Count        : 32
Actual Threads Count       : 1

***** Circuit Statistics *****
# nodes      = 4784 # elements = 11544
# resistors = 5212 # capacitors = 5537 # inductors = 0
# mutual_inds = 0 # vccs = 0 # vcs = 0
# cccs       = 0 # ccvs = 0 # volt_srcs = 3
# curr_srcs = 0 # diodes = 0 # bjts = 0
# jfets      = 0 # mosfets = 792 # U elements = 0
# T elements = 0 # W elements = 0 # B elements = 0
# S elements = 0 # P elements = 0 # va device = 0
# vector_srcs = 0 # N elements = 0

***** Runtime Statistics (seconds) *****
analysis      time    # points tot. iter conv.riter
op point     1.11      1          3
transient    111.65  180000001   39306    13947 rev=    746
readin       0.18
errchk       0.09
setup        1.10
output       0.00

peak memory used      508.95 megabytes
total cpu time        114.76 seconds
total elapsed time    114.89 seconds
job started at        17:45:08 09/28/2023
job ended at          17:47:03 09/28/2023

>info:      ***** hspice job concluded
job total runtime     114.89 seconds
```

Fig 26: in terminal executing the hspice command to analysis the layout frequency

Ring oscillator post layout netlist and simulation file

```

Open ▾ B run_ringoscpost.sp
~/asap7_rundir/simulation

/* Run Inverter file
* Worst case temperature of 110C
.TEMP 110
.OPTION INGOLD=2 ARTIST=2 PSF=2 MEASOUT=1 PARHIER=LOCAL PROBE=0 MARCH=2 ACCURACY=1 POST RUNLVL=5

* Typical NMOS, typical PMOS process corner model file
.INCLUDE /home/class/ee5323ta/ASAP7_PDKandLIB.vip6/asap7PDK_r1p6/models/hspice/7nm_TT.pm
* Slow NMOS, slow PMOS process corner model file
.INCLUDE /home/class/ee5323ta/ASAP7_PDKandLIB.vip6/asap7PDK_r1p6/models/hspice/7nm_SS.pm
* Fast NMOS, fast PMOS process corner model file
.INCLUDE /home/class/ee5323ta/ASAP7_PDKandLIB.vip6/asap7PDK_r1p6/models/hspice/7nm_FF.pm
*.INCLUDE netlist.sp
V1 0 10V 0.7V 10p 10p 40p 100p)
V2 VDD 0 0.63V
V3 VSS 0 0V
* Small lff output capacitance for realistic simulation
C1 Y 0 1fF
.OV

.ic V(y) = 0

.MEASURE tran period TRIG V(y) VAL = 0.5 TD = 10p RISE = 2 TARG V(y) VAL = 0.6 TD = 10p RISE = 3
.MEASURE tran frequency param = '(1/period)'
*.MEASURE tran power avg 'frequency*CL*(VDD)^2'
.MEASURE tran savg avg I(V2)
.MEASURE tran power param = '(V(VDD))^avg'
*.Measure tran power P(VDD)
*.MEASURE tran power avg POWER
.TRAN 0.0001p 10ns

.END

```

Fig 27: run file run_ringoscpost.sp for post layout analysis

```
* File: netlist.sp
* Created: Thu Sep 28 17:19:33 2023
* Program: Calibre xRC
* Version: v2021.3_23.13

*.include "netlist.sp.pex"
*.subckt ring_osc VSS VDD Y
*
* V
* VDD VDD
* VSS VSS

mX10<-89>/M93 N OUT<-89> X10<-89>/M93 d N OUT<-88> X10<-89>/M93_g N VSS X10<-89>/M93_s
+ VSS NMOS_RVT L=2e-08 W=0.1e-08 NFIN=3
mX10<-88>/M93 N OUT<-88> X10<-88>/M93 d N OUT<-87> X10<-88>/M93_g N VSS X10<-88>/M93_s
+ VSS NMOS_RVT L=2e-08 W=0.1e-08 NFIN=3
mX10<-67>/M93 N OUT<-67> X10<-67>/M93 d N OUT<-66> X10<-67>/M93_g N VSS X10<-67>/M93_s
+ VSS NMOS_RVT L=2e-08 W=0.1e-08 NFIN=3
mX10<-66>/M93 N OUT<-66> X10<-66>/M93 d N OUT<-65> X10<-66>/M93_g N VSS X10<-66>/M93_s
+ VSS NMOS_RVT L=2e-08 W=0.1e-08 NFIN=3
mX10<-44>/M93 N OUT<-44> X10<-44>/M93 d N OUT<-43> X10<-44>/M93_g N VSS X10<-44>/M93_s
+ VSS NMOS_RVT L=2e-08 W=0.1e-08 NFIN=3
mX10<-43>/M93 N OUT<-43> X10<-43>/M93 d N OUT<-22> X10<-23>/M93_g N VSS X10<-23>/M93_s
+ VSS NMOS_RVT L=2e-08 W=0.1e-08 NFIN=3
mX10<-22>/M93 N OUT<-22> X10<-22>/M93 d N OUT<-21> X10<-22>/M93_g N VSS X10<-22>/M93_s
+ VSS NMOS_RVT L=2e-08 W=0.1e-08 NFIN=3
mX10<-1>/M93 N OUT<-1> X10<-1>/M93 d N _Y_X10<-1>/M93_g N VSS X10<-1>/M93_s VSS
+ VSS NMOS_RVT L=2e-08 W=0.1e-08 NFIN=3
mX10<-89>/M92 N OUT<-89> X10<-89>/M92 d N OUT<-88> X10<-89>/M92_g N VSS X10<-89>/M92_s
+ VSS NMOS_RVT L=2e-08 W=0.1e-08 NFIN=3
mX10<-88>/M92 N OUT<-88> X10<-88>/M92 d N OUT<-87> X10<-88>/M92_g N VSS X10<-88>/M92_s
+ VSS NMOS_RVT L=2e-08 W=0.1e-08 NFIN=3
mX10<-67>/M92 N OUT<-67> X10<-67>/M92 d N OUT<-66> X10<-67>/M92_g N VSS X10<-67>/M92_s
+ VSS NMOS_RVT L=2e-08 W=0.1e-08 NFIN=3
mX10<-66>/M92 N OUT<-66> X10<-66>/M92 d N OUT<-65> X10<-66>/M92_g N VSS X10<-66>/M92_s
+ VSS NMOS_RVT L=2e-08 W=0.1e-08 NFIN=3
mX10<-45>/M92 N OUT<-45> X10<-45>/M92 d N OUT<-44> X10<-45>/M92_g N VSS X10<-45>/M92_s
+ VSS NMOS_RVT L=2e-08 W=0.1e-08 NFIN=3
mX10<-44>/M92 N OUT<-44> X10<-44>/M92 d N OUT<-43> X10<-44>/M92_g N VSS X10<-44>/M92_s
+ VSS NMOS_RVT L=2e-08 W=0.1e-08 NFIN=3
mX10<-23>/M92 N OUT<-23> X10<-23>/M92 d N OUT<-22> X10<-23>/M92_g N VSS X10<-23>/M92_s
+ VSS NMOS_RVT L=2e-08 W=0.1e-08 NFIN=3
mX10<-22>/M92 N OUT<-22> X10<-22>/M92 d N OUT<-21> X10<-22>/M92_g N VSS X10<-22>/M92_s
+ VSS NMOS_RVT L=2e-08 W=0.1e-08 NFIN=3
mX10<-1>/M92 N OUT<-1> X10<-1>/M92 d N _Y_X10<-1>/M92_g N VSS X10<-1>/M92_s VSS
+ NMOS_RVT L=2e-08 W=0.1e-08 NFIN=3
mX10<-89>/M91 N OUT<-89> X10<-89>/M91 d N OUT<-88> X10<-89>/M91_g N VSS X10<-89>/M91_s
+ VSS NMOS_RVT L=2e-08 W=0.1e-08 NFIN=3
mX10<-88>/M91 N OUT<-88> X10<-88>/M91 d N OUT<-87> X10<-88>/M91_g N VSS X10<-88>/M91_s
+ VSS NMOS_RVT L=2e-08 W=0.1e-08 NFIN=3
mX10<-67>/M91 N OUT<-67> X10<-67>/M91 d N OUT<-66> X10<-67>/M91_g N VSS X10<-67>/M91_s
```

Fig 28: netlist file for post layout netlist.sp

Post layout frequency for process corner TT, 0.7 V, 25 temp

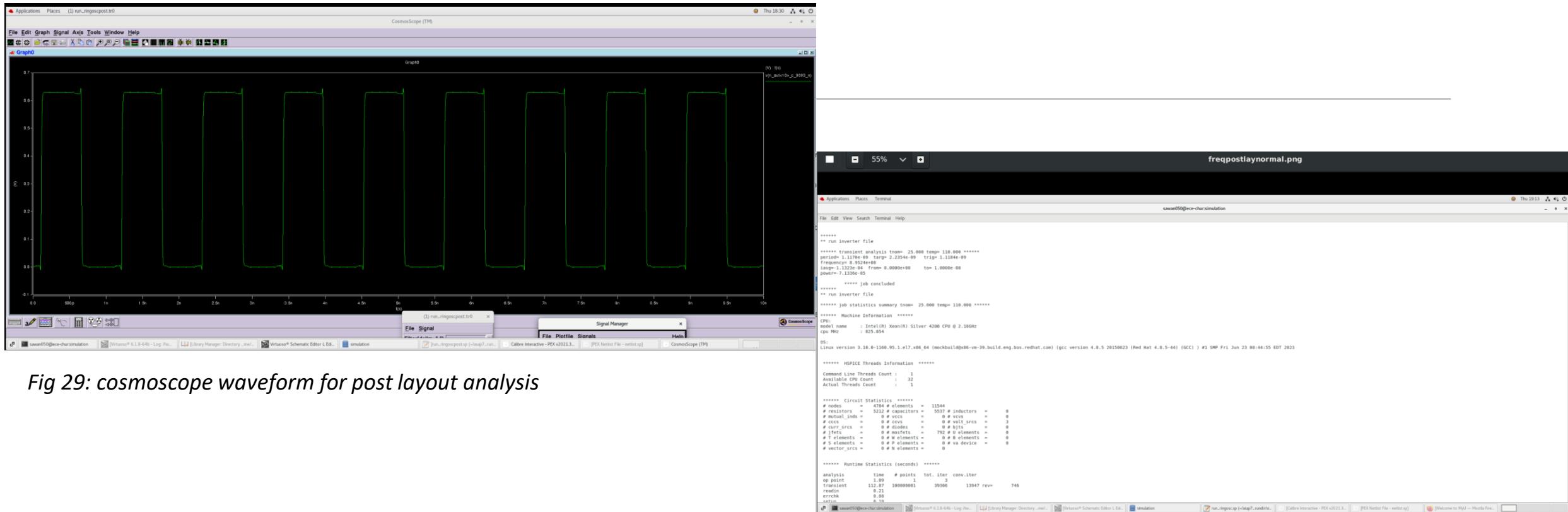


Fig 29: cosmoscope waveform for post layout analysis

Fig 30:frequency = .89524 GHz , power = -7.1336e-5 W for process corner TT, 0.7 V, 25 temp

With capacitance added to the schematic of ring oscillator

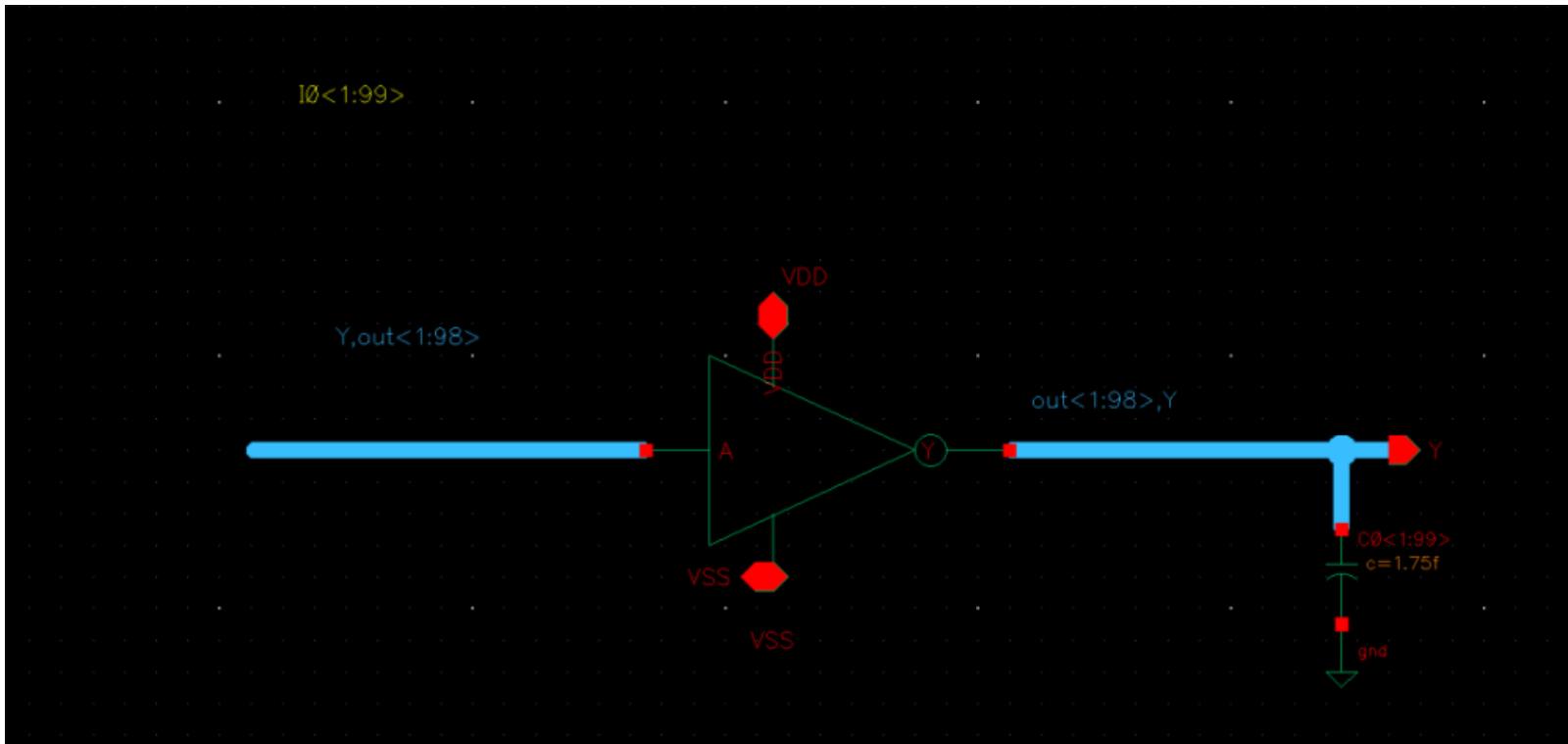
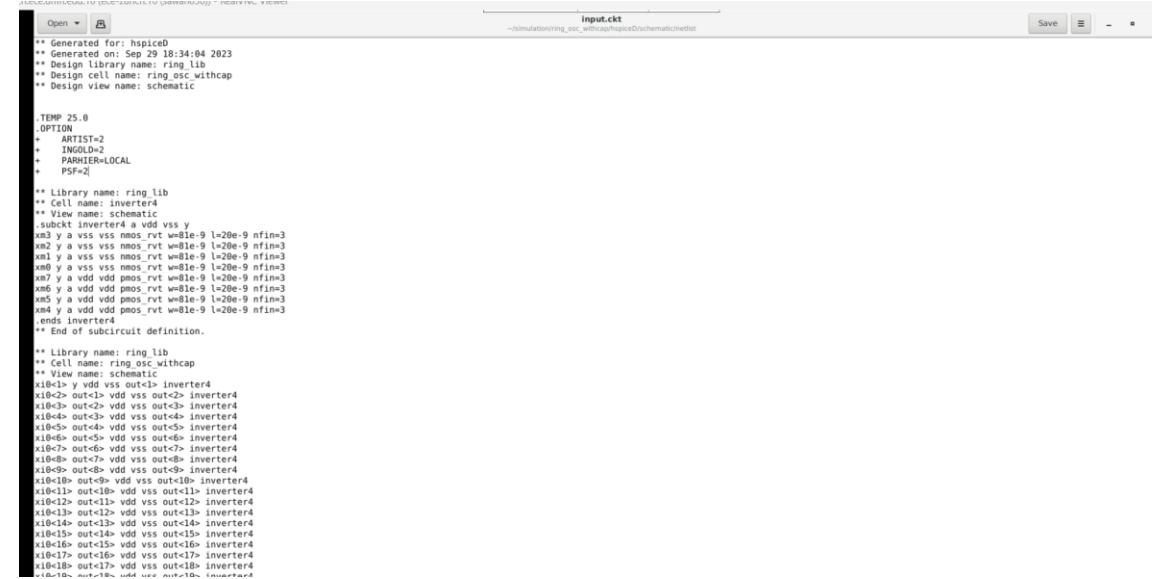


Fig 31: capacitance added to the schematic

Ring oscillator netlist with cap w/o modification of files



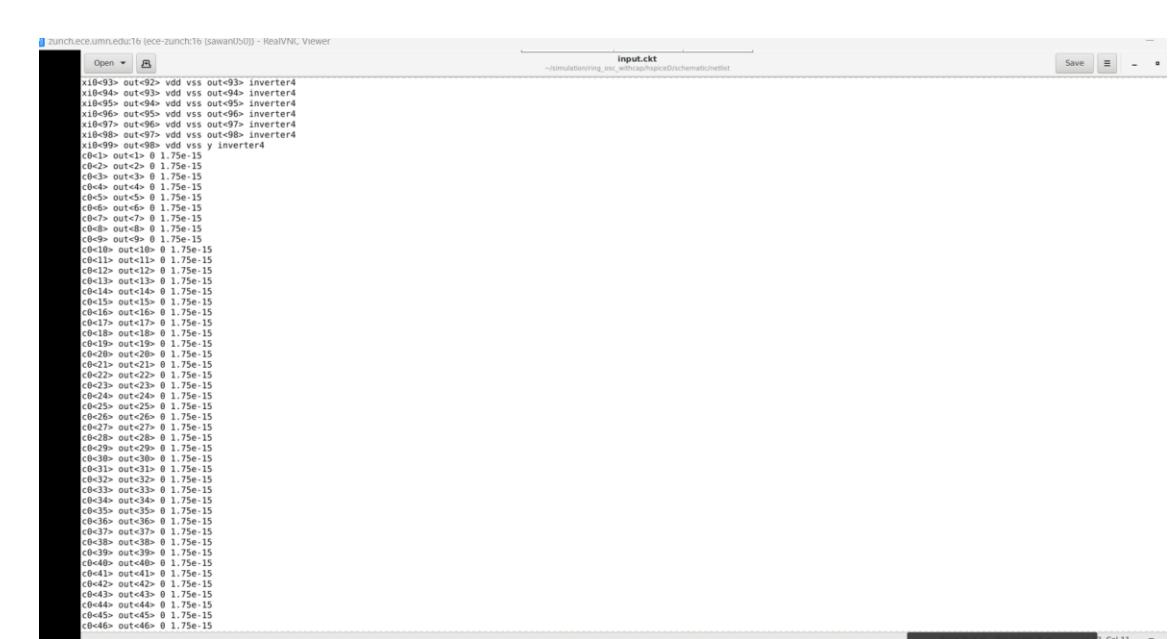
```
** Generated on: Sep 29 18:34:04 2023
** Generated by: hspice0
** Design library name: ring.lib
** Design cell name: ring_osc_wthcap
** Design view name: schematic

TEMP 25.0
OPTION
+ ARTIST=2
+ INGOLD=2
+ PARHIER=LOCAL
+ PSF=2

** Library name: ring.lib
** Cell name: inverter4
** View name: schematic
.subckt inverter4 a vdd vss y
x#3 y a vss vss nmos rvt w=8l=1e-9 l=20e-9 nfin=3
x#2 y a vss vss nmos rvt w=8l=1e-9 l=20e-9 nfin=3
x#1 y a vss vss nmos rvt w=8l=1e-9 l=20e-9 nfin=3
x#0 y a vss vss nmos rvt w=8l=1e-9 l=20e-9 nfin=3
x#7 y a vdd vdd pmos rvt w=8l=1e-9 l=20e-9 nfin=3
x#6 y a vdd vdd pmos rvt w=8l=1e-9 l=20e-9 nfin=3
x#5 y a vdd vdd pmos rvt w=8l=1e-9 l=20e-9 nfin=3
x#4 y a vdd vdd pmos rvt w=8l=1e-9 l=20e-9 nfin=3
.ends inverter4
** End of subcircuit definition.

** Library name: ring.lib
** Cell name: ring_osc_wthcap
** View name: schematic
x#0<2> out<1> vdd vss out<2> inverter4
x#0<3> out<2> vdd vss out<3> inverter4
x#0<4> out<3> vdd vss out<4> inverter4
x#0<5> out<4> vdd vss out<5> inverter4
x#0<6> out<5> vdd vss out<6> inverter4
x#0<7> out<6> vdd vss out<7> inverter4
x#0<8> out<7> vdd vss out<8> inverter4
x#0<9> out<8> vdd vss out<9> inverter4
x#0<10> out<9> vdd vss out<10> inverter4
x#0<11> out<10> vdd vss out<11> inverter4
x#0<12> out<11> vdd vss out<12> inverter4
x#0<13> out<12> vdd vss out<13> inverter4
x#0<14> out<13> vdd vss out<14> inverter4
x#0<15> out<14> vdd vss out<15> inverter4
x#0<16> out<15> vdd vss out<16> inverter4
x#0<17> out<16> vdd vss out<17> inverter4
x#0<18> out<17> vdd vss out<18> inverter4
x#0<19> out<18> vdd vss out<19> inverter4
```

Fig 32: netlist with cap without modification



```
x#0<33> out<92> vdd vss out<93> inverter4
x#0<44> out<93> vdd vss out<94> inverter4
x#0<55> out<94> vdd vss out<95> inverter4
x#0<66> out<95> vdd vss out<96> inverter4
x#0<77> out<96> vdd vss out<97> inverter4
x#0<88> out<97> vdd vss out<98> inverter4
x#0<99> out<98> vdd vss out<99> inverter4
x#0<100> out<99> vdd vss out<100> inverter4
x#0<1> out<1> 0 1.75e-15
x#0<2> out<2> 0 1.75e-15
x#0<3> out<3> 0 1.75e-15
x#0<4> out<4> 0 1.75e-15
x#0<5> out<5> 0 1.75e-15
x#0<6> out<6> 0 1.75e-15
x#0<7> out<7> 0 1.75e-15
x#0<8> out<8> 0 1.75e-15
x#0<9> out<9> 0 1.75e-15
x#0<10> out<10> 0 1.75e-15
x#0<11> out<11> 0 1.75e-15
x#0<12> out<12> 0 1.75e-15
x#0<13> out<13> 0 1.75e-15
x#0<14> out<14> 0 1.75e-15
x#0<15> out<15> 0 1.75e-15
x#0<16> out<16> 0 1.75e-15
x#0<17> out<17> 0 1.75e-15
x#0<18> out<18> 0 1.75e-15
x#0<19> out<19> 0 1.75e-15
x#0<20> out<20> 0 1.75e-15
x#0<21> out<21> 0 1.75e-15
x#0<22> out<22> 0 1.75e-15
x#0<23> out<23> 0 1.75e-15
x#0<24> out<24> 0 1.75e-15
x#0<25> out<25> 0 1.75e-15
x#0<26> out<26> 0 1.75e-15
x#0<27> out<27> 0 1.75e-15
x#0<28> out<28> 0 1.75e-15
x#0<29> out<29> 0 1.75e-15
x#0<30> out<30> 0 1.75e-15
x#0<31> out<31> 0 1.75e-15
x#0<32> out<32> 0 1.75e-15
x#0<33> out<33> 0 1.75e-15
x#0<34> out<34> 0 1.75e-15
x#0<35> out<35> 0 1.75e-15
x#0<36> out<36> 0 1.75e-15
x#0<37> out<37> 0 1.75e-15
x#0<38> out<38> 0 1.75e-15
x#0<39> out<39> 0 1.75e-15
x#0<40> out<40> 0 1.75e-15
x#0<41> out<41> 0 1.75e-15
x#0<42> out<42> 0 1.75e-15
x#0<43> out<43> 0 1.75e-15
x#0<44> out<44> 0 1.75e-15
x#0<45> out<45> 0 1.75e-15
x#0<46> out<46> 0 1.75e-15
```

Fig 33: netlist with cap without modification

Ring oscillator netlist and run file with cap with modification of files

```
** Generated for: hispiceD
** Generated on: Sep 29 18:34:04 2023
** Design library name: ring.lib
** Design cell name: ring_osc_withcap
** Design view name: schematic

** Library name: ring.lib
** Cell name: inverter4
** View name: schematic
** subcircuit inverter4 a vdd vss y
m3 y a vss vss nmos rvt w=8l=9 l=28e-9 nfin=3
m2 y a vss vss nmos rvt w=8l=9 l=28e-9 nfin=3
m1 y a vss vss nmos rvt w=8l=9 l=28e-9 nfin=3
m0 y a vdd vdd pmos rvt w=8l=9 l=28e-9 nfin=3
m3 y a vdd vdd pmos rvt w=8l=9 l=28e-9 nfin=3
m2 y a vdd vdd pmos rvt w=8l=9 l=28e-9 nfin=3
m1 y a vdd vdd pmos rvt w=8l=9 l=28e-9 nfin=3
m0 y a vdd vdd pmos rvt w=8l=9 l=28e-9 nfin=3
.ends inverter4
** End of subcircuit definition.

** Library name: ring.lib
** Cell name: ring_osc_withcap
** View name: schematic
** subcircuit ring_osc_withcap a vdd vss y
x10<2> out<1> vdd vss out<2> inverter4
x10<2> out<1> vdd vss out<2> inverter4
x10<3> out<2> vdd vss out<3> inverter4
x10<4> out<3> vdd vss out<4> inverter4
x10<5> out<4> vdd vss out<5> inverter4
x10<6> out<5> vdd vss out<6> inverter4
x10<7> out<6> vdd vss out<7> inverter4
x10<8> out<7> vdd vss out<8> inverter4
x10<9> out<8> vdd vss out<9> inverter4
x10<10> out<9> vdd vss out<10> inverter4
x10<11> out<10> vdd vss out<11> inverter4
x10<12> out<11> vdd vss out<12> inverter4
x10<13> out<12> vdd vss out<13> inverter4
x10<14> out<13> vdd vss out<14> inverter4
x10<15> out<14> vdd vss out<15> inverter4
x10<16> out<15> vdd vss out<16> inverter4
x10<17> out<16> vdd vss out<17> inverter4
x10<18> out<17> vdd vss out<18> inverter4
x10<19> out<18> vdd vss out<19> inverter4
x10<20> out<19> vdd vss out<20> inverter4
x10<21> out<20> vdd vss out<21> inverter4
```

```
Open ▾ A Save ▾ x
run_ringoscwithcap.sp
--asap7_runder/simulation

** Run Inverter file
* Worst case temperature of 110C
.TEMP 25
.OPTION INGOLD=2 ARTIST=2 PSF=2 MEASOUT=1 PARHIER=LOCAL PROBE=0 MARCH=2 ACCURACY=1 POST RUNLVL=5

* Typical NMOS, typical PMOS process corner model file
.INCLUDE /home/class/ee5323ta/ASAP7_PDKandLIB_v1p6/asap7PDK_r1p6/models/hspice/7nm_TT.pm
* Slow NMOS, slow PMOS process corner model file
*.INCLUDE /home/class/ee5323ta/ASAP7_PDKandLIB_v1p6/asap7PDK_r1p6/models/hspice/7nm_SS.pm
* Fast NMOS, fast PMOS process corner model file
*.INCLUDE /home/class/ee5323ta/ASAP7_PDKandLIB_v1p6/asap7PDK_r1p6/models/hspice/7nm_FF.pm
.INCLUDE ringwithcap.sp
V1 A 0 PULSE(0 0.7V 10p 10p 10p 40p 100p)
V2 VDD 0 1.7V
V3 VSS 0 0V
* Small LFF output capacitance for realistic simulation
C1 Y 0 lff
.OP

.ic V(Y) = 0

.MEASURE tran period TRIG V(Y) VAL = 0.5 TD = 10p RISE = 2 TARG V(Y) VAL = 0.6 TD = 10p RISE = 3
.MEASURE tran frequency param = '(1/period)'
*.MEASURE tran power avg 'frequency*C1*((VDD)^2)'
*.MEASURE tran iavg avg I(V2)
*.MEASURE tran power param = 'V(VDD)*iavg'
*.Measure tran power P(VDD)
*.MEASURE tran power avg POWER
.TRAN 0.001p 10ns

.END
```

Fig 34: netlist with cap with modification

Fig 35: run file with cap with modification

Checking freq for different Capacitance= 0.5f F

```
sawan050@ece-zurich:simulation
File Edit View Search Terminal Help
cgd 3.214e-17 3.214e-17

*****
** run inverter file

***** transient analysis tnom= 25.000 temp= 25.000 *****
period= 7.2021e-10 targ= 2.1611e-09 trig= 1.4409e-09
frequency= 1.3885e+09
iavg=-2.3100e-04 from= 0.0000e+00 to= 1.0000e-08
power=-1.6170e-04

***** job concluded

** run inverter file

***** job statistics summary tnom= 25.000 temp= 25.000 *****

***** Machine Information *****
CPU:
model name : Intel(R) Xeon(R) Silver 4208 CPU @ 2.10GHz
cpu MHz : 2834.948

OS:
Linux version 3.10.0-1160.95.1.el7.x86_64 (mockbuild@x86-vm-39.build.eng.bos.redhat.com) (gcc version 4.8.5 20150623 (Red Hat 4.8.5-44) (GCC) ) #1 SMP Fri Jun 23 08:44:55 EDT 2023

***** HSPICE Threads Information *****

Command Line Threads Count : 1
Available CPU Count : 32
Actual Threads Count : 1

***** Circuit Statistics *****
# nodes = 103 # elements = 895
# resistors = 0 # capacitors = 100 # inductors = 0
# mutual_inds = 0 # vccs = 0 # vcvs = 0
# cccs = 0 # ccvs = 0 # volt_srcs = 3
# curr_srcs = 0 # diodes = 0 # bjts = 0
# jfets = 0 # mosfets = 792 # U elements = 0
# T elements = 0 # W elements = 0 # B elements = 0
# S elements = 0 # P elements = 0 # va device = 0
# vector_srcs = 0 # N elements = 0

***** Runtime Statistics (seconds) *****
analysis time # points tot. iter conv. iter
op point 0.17 1 2
transient 36.23 10000001 68868 25648 rev= 759
readin 0.03
errchk 0.06
```

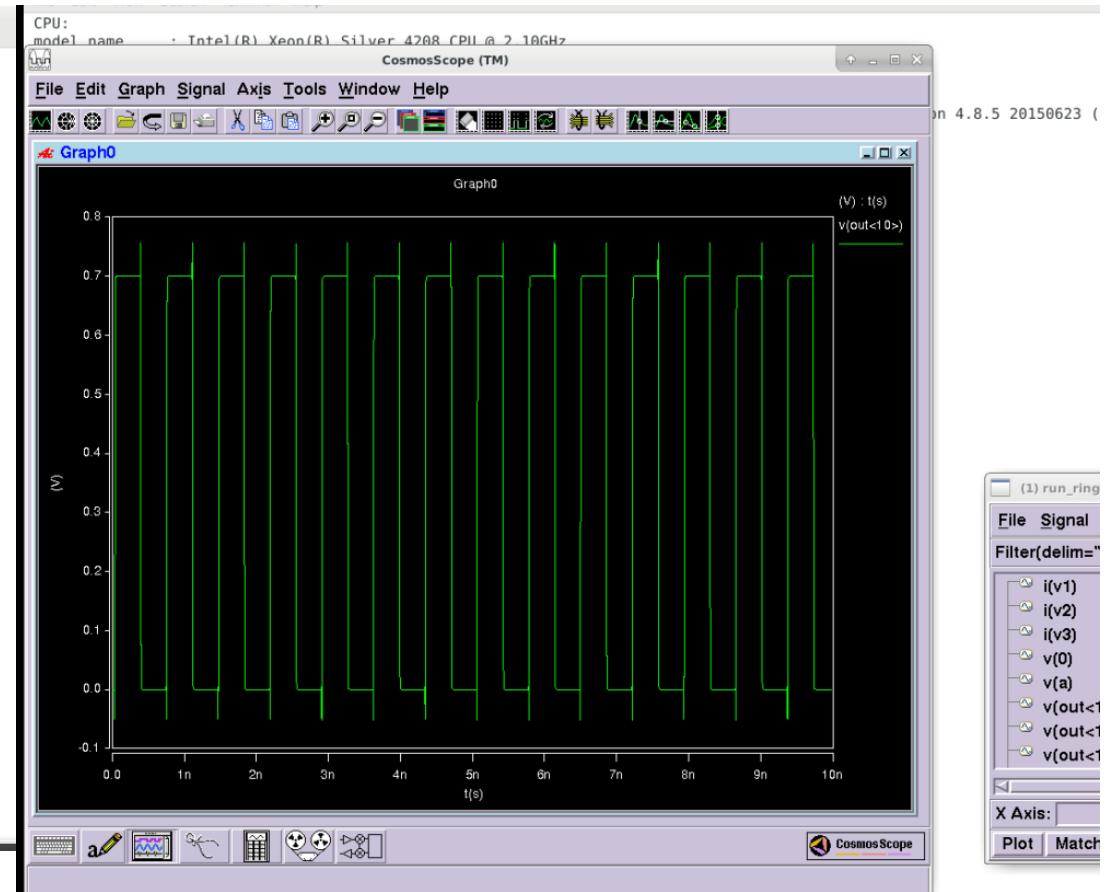


Fig 36: for process corner = tt , 0.7 v, 25 temp, freq = 1.385GHz , Power = -1.617e-4

Fig 37: waveform in cosmoscope for for process corner = tt , 0.7 v, 25 temp with capacitance

Checking freq for different Freq with cap value = 1f F

```
Applications Places Terminal sawan050@ece-chur:simulation
File Edit View Search Terminal Help

*****
** run inverter file
*****
***** transient analysis tnom= 25.000 temp= 25.000 *****
period= 8.8080e-10 targ= 2.6431e-09 trig= 1.7623e-09
frequency= 1.1353e+09
iavg=-2.2862e-04 from= 0.0000e+00 to= 1.0000e-08
power=-1.6004e-04

***** job concluded
*****
** run inverter file
*****
***** job statistics summary tnom= 25.000 temp= 25.000 *****
***** Machine Information *****
CPU:
model name      : Intel(R) Xeon(R) Silver 4208 CPU @ 2.10GHz
cpu MHz         : 799.932

OS:
Linux version 3.10.0-1160.95.1.el7.x86_64 (mockbuild@x86-vm-39.build.eng.bos.redhat.com) (gcc version 4.8.5 20150623 (Red Hat 4.8.5-44) (GCC) ) #1 SMP Fri Jun 23 08:44:55 EDT 2023

***** HSPICE Threads Information *****
Command Line Threads Count : 1
Available CPU Count       : 32
Actual Threads Count      : 1

***** Circuit Statistics *****
# nodes      = 103 # elements = 895
# resistors  = 0 # capacitors = 100 # inductors = 0
# mutual_inds = 0 # vccs = 0 # vcvs = 0
# cccs       = 0 # ccvs = 0 # volt_srcs = 3
# curr_srcs  = 0 # diodes = 0 # bjt = 0
# jfets       = 0 # mosfets = 792 # U elements = 0
# T elements = 0 # W elements = 0 # B elements = 0
# S elements = 0 # P elements = 0 # va device = 0
# vector_srcs = 0 # N elements = 0

***** Runtime Statistics (seconds) *****
analysis      time   # points tot. iter conv.riter
op point     0.37          1        2
transient    22.15 10000001    52434    19198 rev= 555
readin       0.03
errchk       0.08
kernin      0.0K

sawan050@ece-chu ~ Virtuoso® 6.1.8-64... Library Manager: Dir... Virtuoso® Schematic... Downloads ringwithcap.sp (~/as... Calibre Interactive - PEX Netlist File - ne... Web Login Service ...
```

Fig 38: for process corner = tt , 0.7 v, 25 temp, freq = 1.353GHz , Power = -1.6004e-4



Fig 39: waveform in cosmoscope for for process corner = tt , 0.7 v, 25 temp with capacitance

Checking freq for different Cap= 1.5fF

```
sawan050@ece-zurich:simulation
File Edit View Search Terminal Help
** run inverter file
***** transient analysis tnom= 25.000 temp= 25.000 *****
period= 1.8406e-09 targe 3.1230e-09 trig= 2.0823e-09
frequency 9.6095e+08
iavg= 2.2704e-04 from= 0.0000e+00 to= 1.0000e-08
power= -1.5893e-04

***** job concluded
** run inverter file
***** job statistics summary tnom= 25.000 temp= 25.000 *****
***** Machine Information *****
CPU:
model name      : Intel(R) Xeon(R) Silver 4208 CPU @ 2.10GHz
cpu MHz         : 799.932
OS:
Linux version 3.10.0-1160.95.1.el7.x86_64 (mockbuild@x86-vm-39.build.eng.bos.redhat.com) (gcc version 4.8.5 20150623 (Red Hat 4.8.5-44) (GCC) ) #1 SMP Fri Jun 23 08:44:55 EDT 2023

***** HSPICE Threads Information *****
Command Line Threads Count : 1
Available CPU Count       : 32
Actual Threads Count      : 1

***** Circuit Statistics *****
# nodes      = 103 # elements = 895
# resistors  = 0 # capacitors = 100 # inductors = 0
# mutual_inds = 0 # vccs      = 0 # vcvs      = 0
# cccs       = 0 # ccvs      = 0 # volt_srcs = 3
# curr_srcs  = 0 # diodes    = 0 # bjt      = 0
# jfets       = 0 # mosfets   = 792 # U elements = 0
# T elements = 0 # W elements = 0 # B elements = 0
# S elements = 0 # P elements = 0 # va device = 0
# vector_srcs = 0 # N elements = 0

***** Runtime Statistics (seconds) *****
analysis      time    # points tot. iter conv.riter
op point     0.29          1      2
transient    20.75 10000001    43085      15707 rev= 489
readin       0.03
errchk       0.06
setup        0.01
output       0.00

peak memory used 476.43 megabytes
```

Fig 40: for process corner = tt , 0.7 v, 25 temp, freq = .96095GHz , Power = -1.5893e-4

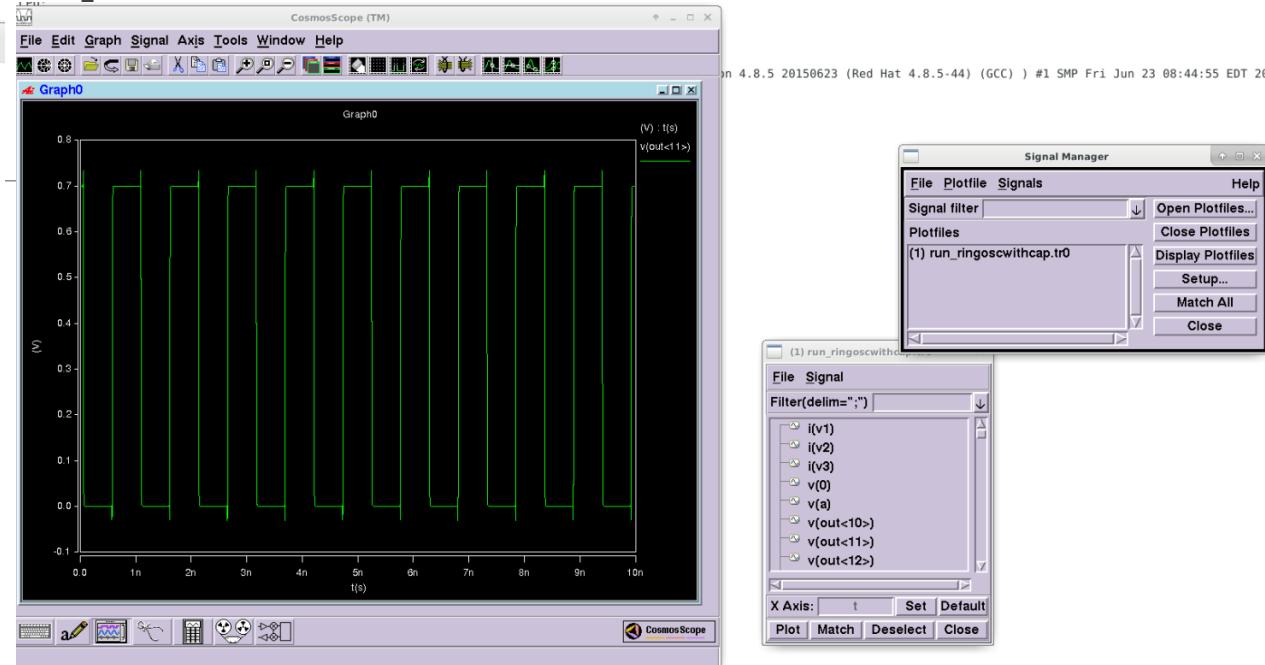


Fig 41: waveform in cosmoscope for for process corner = tt , 0.7 v, 25 temp with capacitance

Scope with cap =1.75f F this capacitance value gives within 1%

```
sawan050@ece-zurich:simulation
File Edit View Search Terminal Help

*****
** run inverter file
*****
transient analysis tnom= 25.000 temp= 25.000 *****
period= 1.1204e-09 targ= 3.3623e-09 trig= 2.2420e-09
frequency= 8.9256e+08
iavg=2.2643e-04 frome 0.0000e+00 to= 1.0000e-08
power=-1.5850e-04

***** job concluded
** run inverter file
*****
job statistics summary tnom= 25.000 temp= 25.000 *****
***** Machine Information *****
CPU:
model name      : Intel(R) Xeon(R) Silver 4208 CPU @ 2.10GHz
cpu MHz         : 800.317
OS:
Linux version 3.10.0-1160.95.1.el7.x86_64 (mockbuild@x86-vm-39.build.eng.bos.redhat.com) (gcc version 4.8.5 20150623 (Red Hat 4.8.5-44) (GCC) ) #1 SMP Fri Jun 23 08:44:55 EDT 2023

***** HSPICE Threads Information *****
Command Line Threads Count : 1
Available CPU Count        : 32
Actual Threads Count       : 1

***** Circuit Statistics *****
# nodes          103 # elements     = 895
# resistors      = 0 # capacitors   = 100 # inductors   = 0
# mutual_inds    = 0 # vccs          = 0 # vcvs         = 0
# cccs           = 0 # ccvs          = 0 # volt_srcs    = 0
# curr_srcs      = 0 # diodes         = 0 # bjts          = 0
# jfets           = 0 # mosfets        = 792 # U elements  = 0
# T elements     = 0 # W elements    = 0 # B elements    = 0
# S elements     = 0 # P elements    = 0 # va device     = 0
# vector_srcs    = 0 # N elements    = 0

***** Runtime Statistics (seconds) *****
analysis          time   # points tot. iter conv.riter
op point          0.19          1      2
transient         19.99 10000001    39514    14373 rev= 522
readin            0.03
errchk            0.04
setup             0.01
output            0.00
```

Fig 42: for process corner = tt , 0.7 v, 25 temp, freq = 0.8925GHz , Power = -1.585e-4

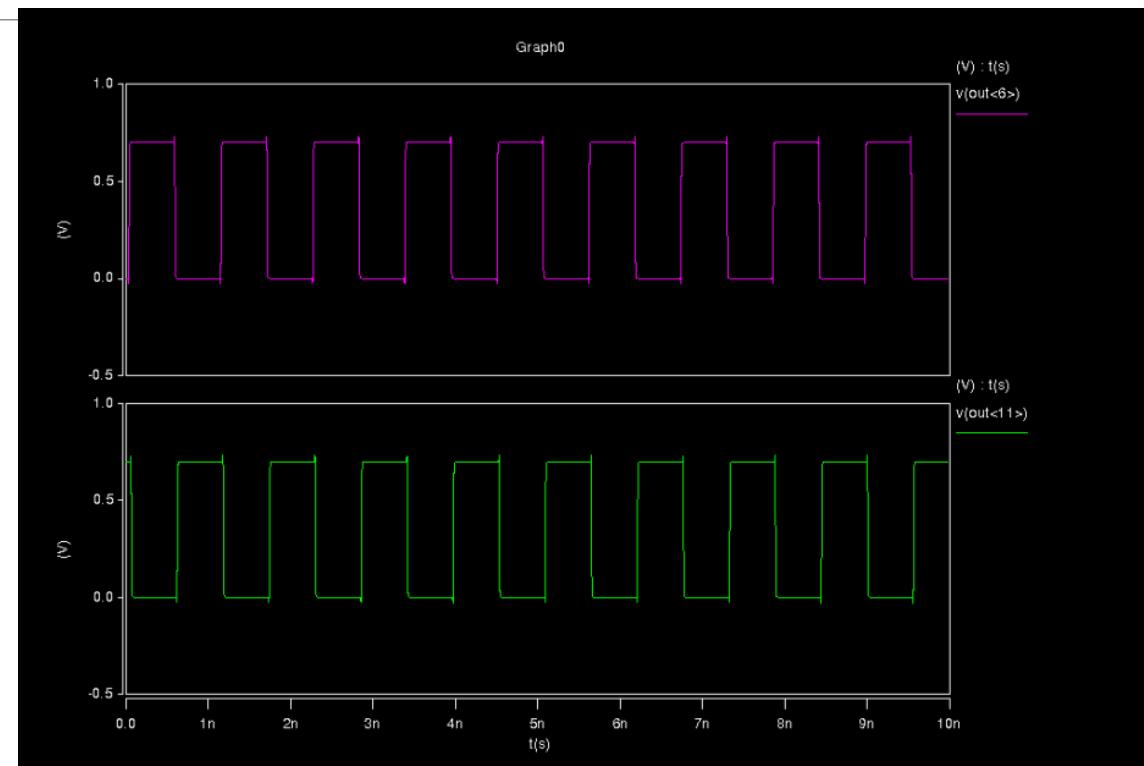


Fig 43: waveform in cosmoscope for for process corner = tt , 0.7 v, 25 temp with capacitance

What is the % frequency difference between the schematic and the extracted layout?

Schematic w/o cap	Layout
freq = 1.803 GHz	freq = 0.8952 GHz
<hr/>	
diff % =	$\frac{1.803 - 0.8952}{1.803} \times 100 = 50.3\%$

How much load capacitance should be added to each stage of the ring oscillator schematic for the schematic and layout frequencies to be within 1% of each other?

Capacitance value to be selected is 1.75 fF which results in 0.3 %

① $C = 0.5 \text{ fF}$
 $f = 1.38 \text{ GHz}$
 $\therefore \text{change} = \frac{1.38 - 0.8952}{0.8952} = 54\%$.

② $C = 1 \text{ fF}$
 $f = 1.135 \text{ GHz}$
 $\therefore \text{change} = \frac{1.135 - 0.8952}{0.8952} = \cancel{26\%}, 26\%$.

③ $C = 1.5 \text{ fF}$
 $f = 0.96 \text{ GHz}$
 $\therefore \text{change} = 7.2\%$.

④ $C = 1.75 \text{ fF}$
 $f = 0.8925 \text{ GHz}$
 $\therefore \text{change} = 0.3\%$.

Analysis for process corner = tt , 0.7v, 25 temp

	Schematic without cap	Post Layout	Schematic with cap
Frequency	1.803GHz	0.8952GHz	0.8925GHz
power	-1.6439e-4W	0.71336e-4W	-1.585e-4W

Conclusion

A comprehensive understanding of the design process, simulation techniques, and layout extraction was gained. Achieving a design where the schematic and layout frequencies are within 1% of each other demonstrates the precision and accuracy of the design process.