EE 5323 Homework #1: Ring Oscillator Schematic Design

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Setting Up Cadence

- Created a working directory in home folder (/home/class/sawan050) using mkdir command: mkdir asap7_rundir

- Going to the working directory: cd ~/asap7_rundir

- Setting the environment variable PDK_DIR using the following command, so that it points to the ASAP 7nm PDK directory:
  setenv PDK_DIR /home/class/ee5323ta/ASAP7_PDKandLIB_v1p6/asap7PDK_r1p6

- Sourcing the PDK configuration file to copy all necessary files in the run directory to copy all necessary files to the working directory
  source $PDK_DIR/cdslib/setup/config_asap7.csh

- Running Cadence virtuoso using
  source setup.csh

Creating Library as ring_lib

- From the virtuoso CIW box, File -> New -> Library -> ring_lib
- Selecting the “Attach to an existing technology library” option, click OK.
- Now, in the pop-up window, selecting asap7_TechLib library and click OK. Created library “ring_lib” as “/home/class/sawan050/asap7_rundir/ring_lib”
- Create a new cell From the Virtuoso CIW, File -> New -> Cellview -> with cell name inverter4

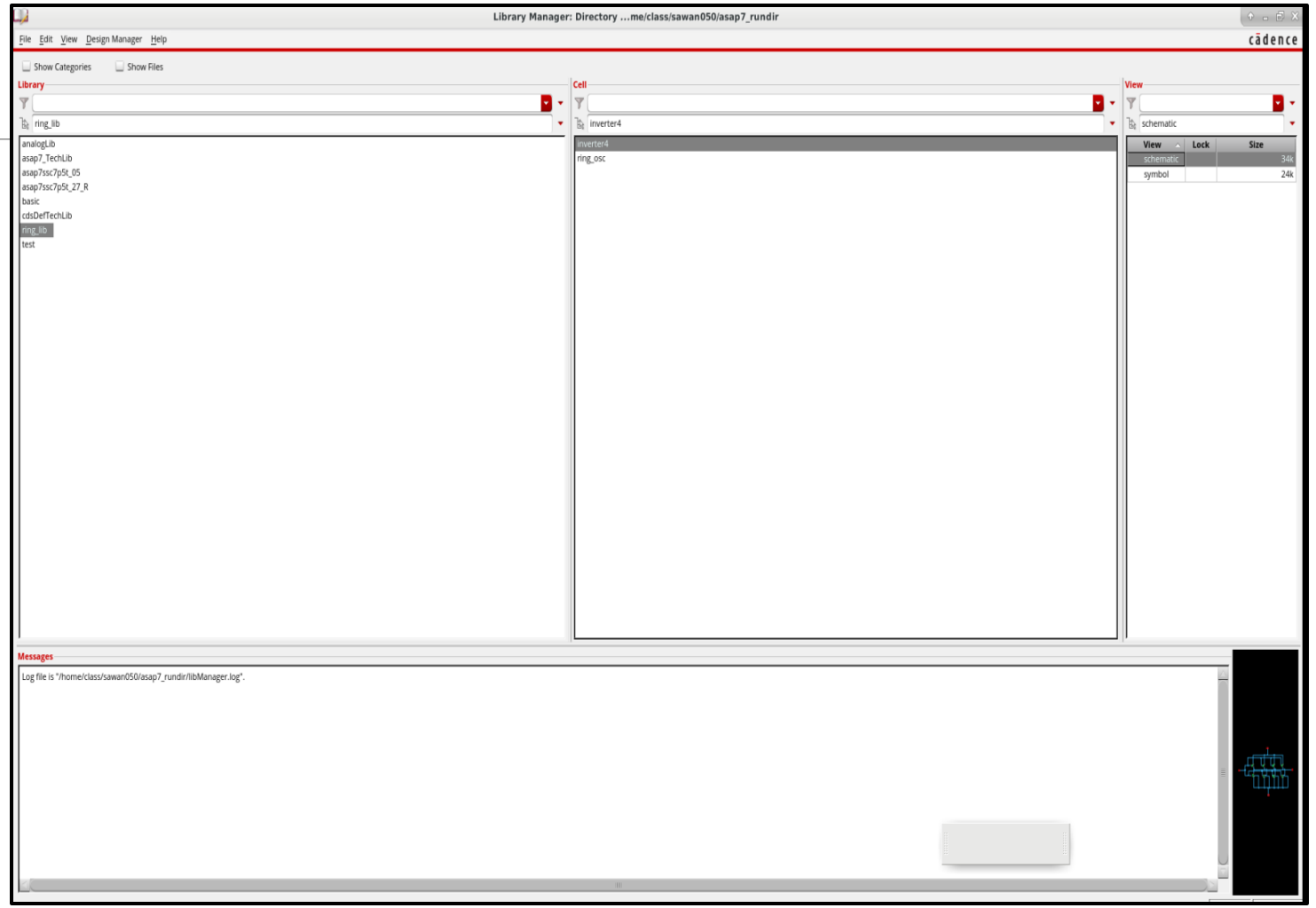


Fig 1: Creating Library ring_lib and cell name as inverter4

Creating Inverter4 Schematic in ring_lib

- Using asap7_TechLib library to browser for nmos_rvt and pmos_rvt, symbol view.
  - No of fin = 3
  - Fin width = 27nm.
  - Length = 20nm
  - Transistor width = 81nm
- And respective pins and wires to complete the circuit
- Here A is input pin , Y is output pin, VDD ,VSS are power and ground respectively
- Output is taken from drain terminal of mosfets.

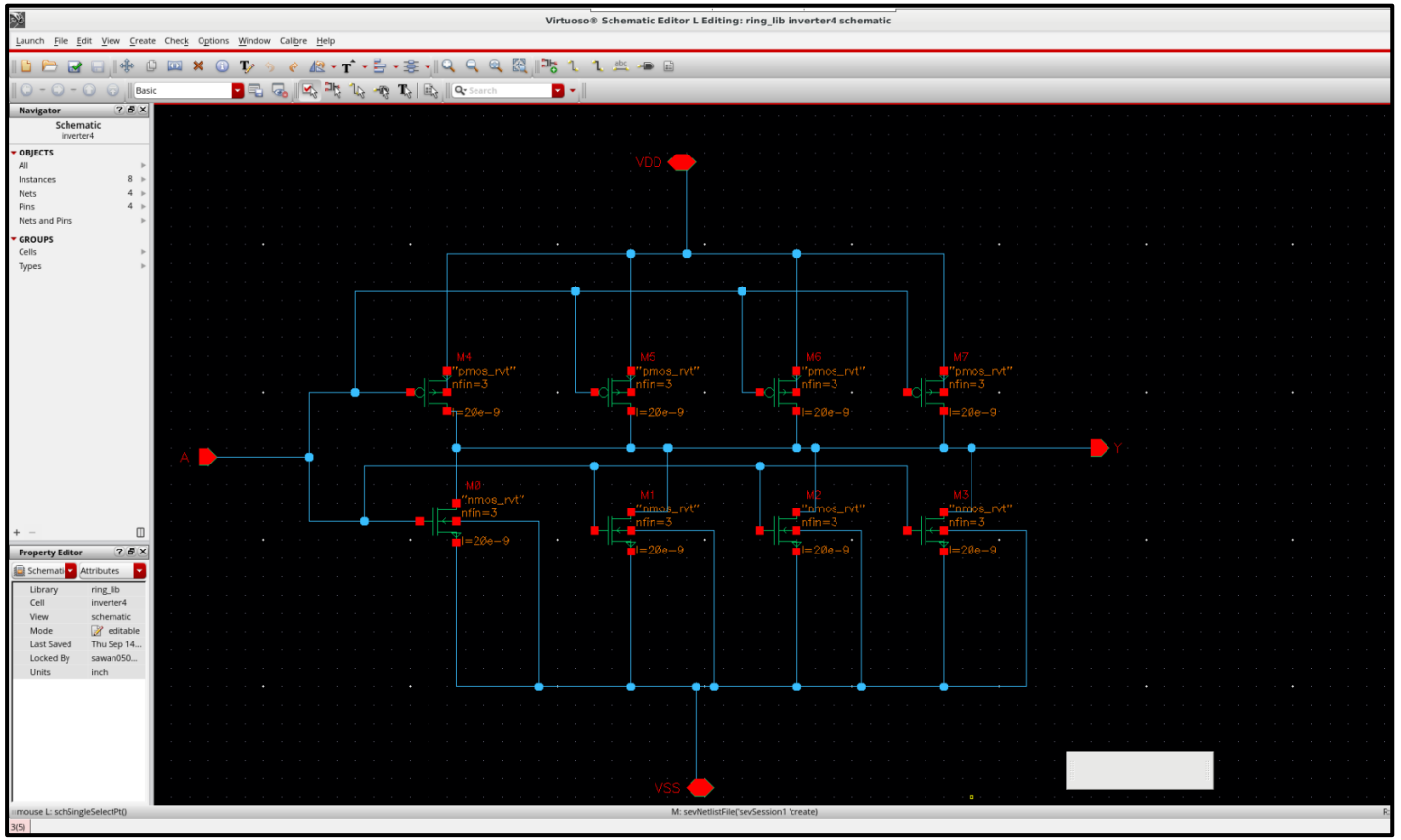


Fig 2: Creating schematic in Library ring_lib for inverter4

Setting up ADL , Creating Netlist , Waveforms in Cosmoscope

- Setting up Simulator and the environment in ADL to Hspice .
- Creating netlist for inverter4 to run in cosmoscope.
- The image shows output Y is in the inverted form from input signal A.

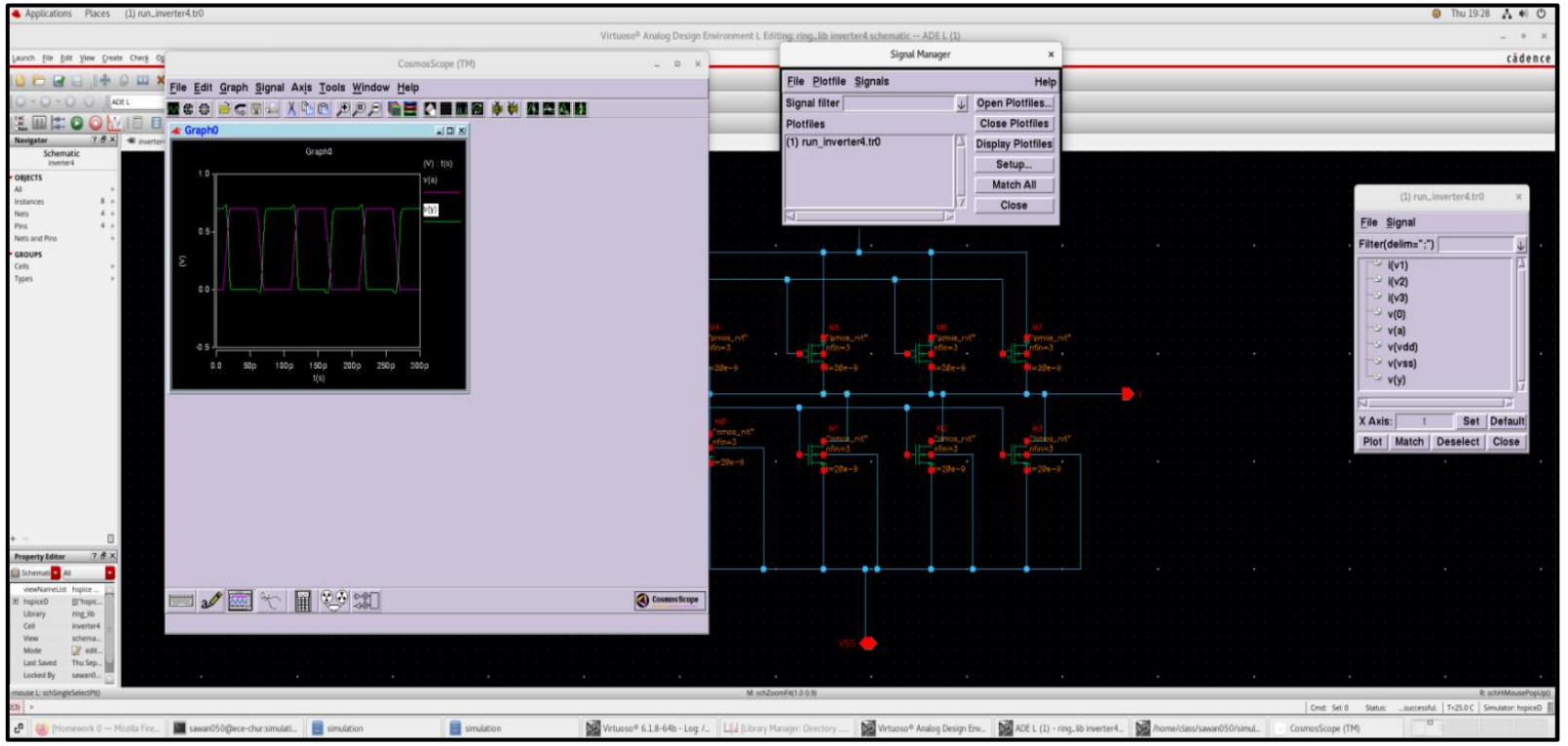


Fig 3: Creating waveforms in cosmoscope for inverter4

Creating a new symbol

- Saving the schematic before creating its symbol: File->Check and Save
- Create->Cellview->From Cellview, click OK.
- From View Name should be schematic and To View Name should be symbol.
- Tool /Data Type should be set to schematicSymbol. Click on OK.
- This symbol of inverter4 to be used in creating schematic of ring oscillator

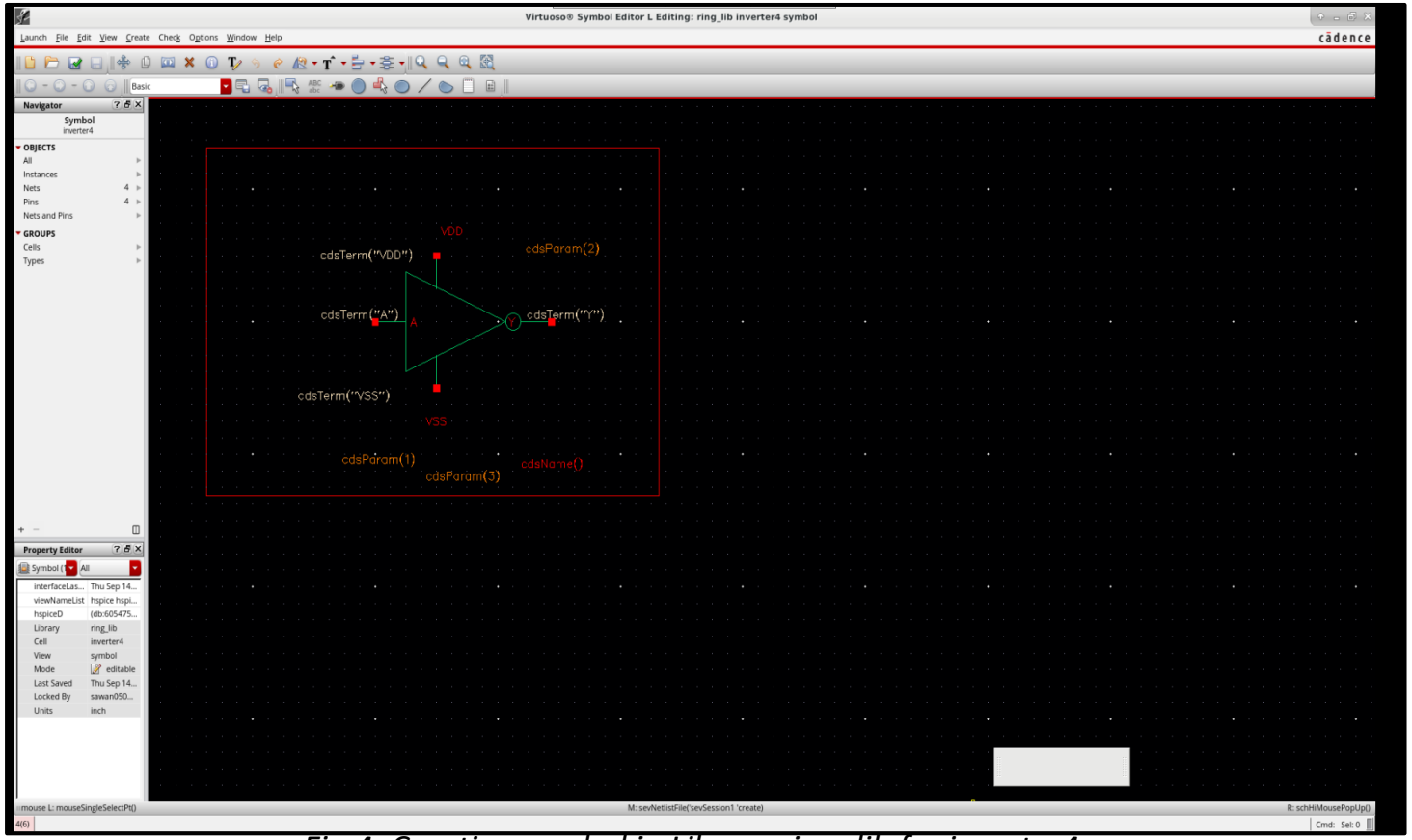


Fig 4: Creating symbol in Library ring_lib for inverter4

Creating cell name ring_osc for 99 stage ring oscillator schematic

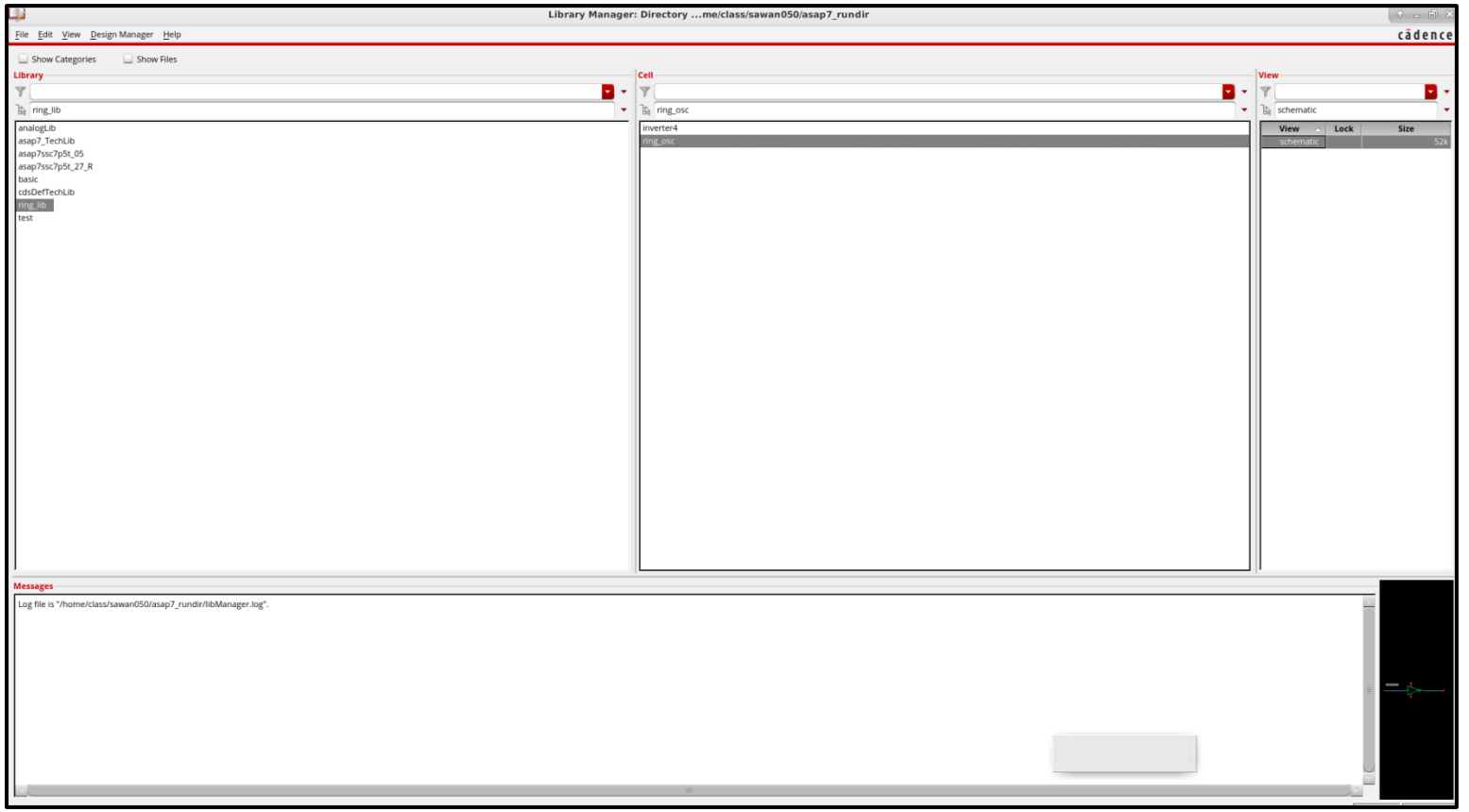


Fig 5: Creating in Library ring_lib , cell name as ring_osc

Using the inverter4 symbol created earlier in ring_lib to use in ring_osc schematic

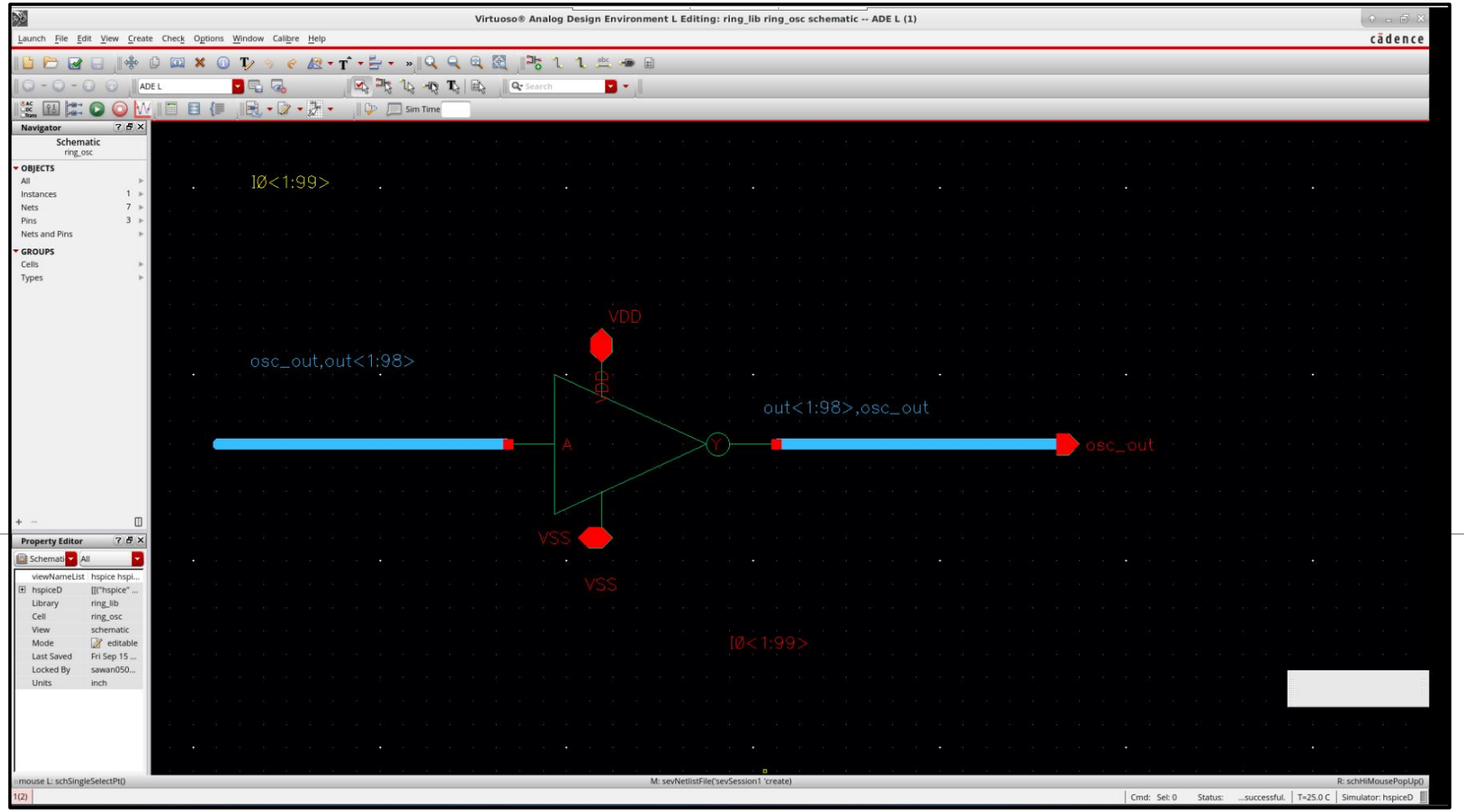


Fig 6: Creating in Library ring_lib schematic for 99 stage ring oscillator

Setting ADL for ring oscillator

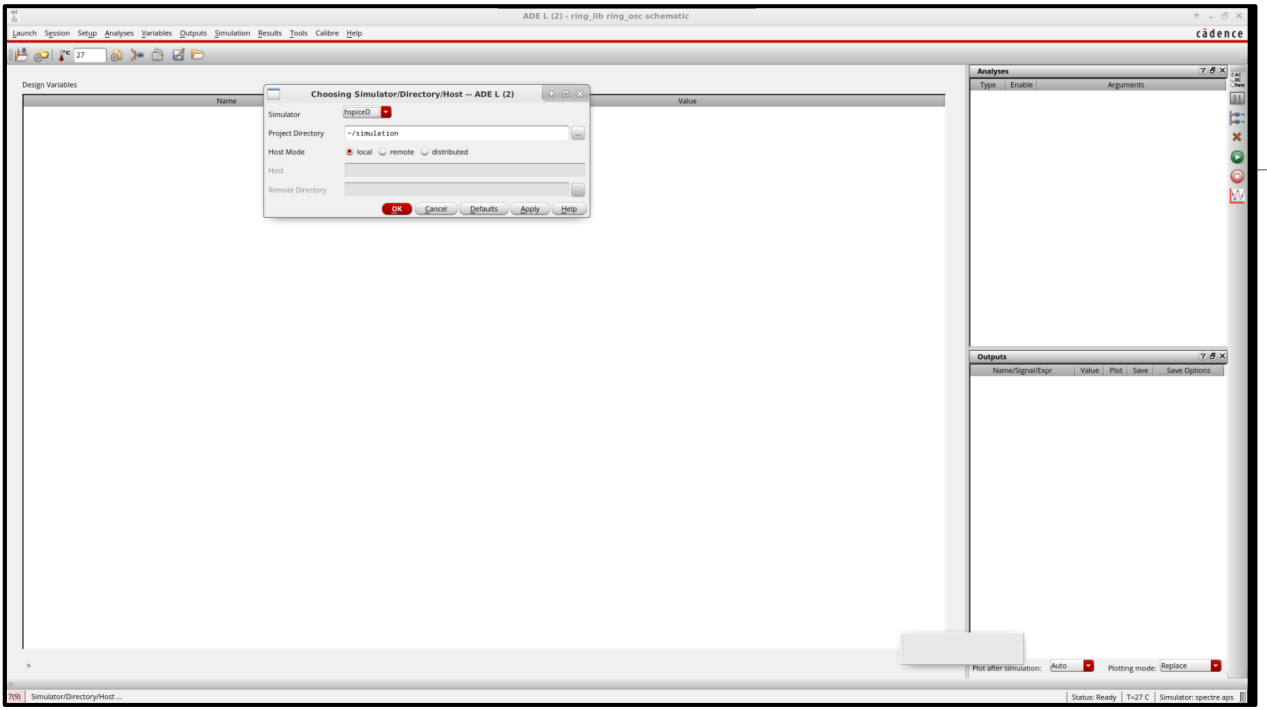


Fig 7: Setting up simulation folder in ADL

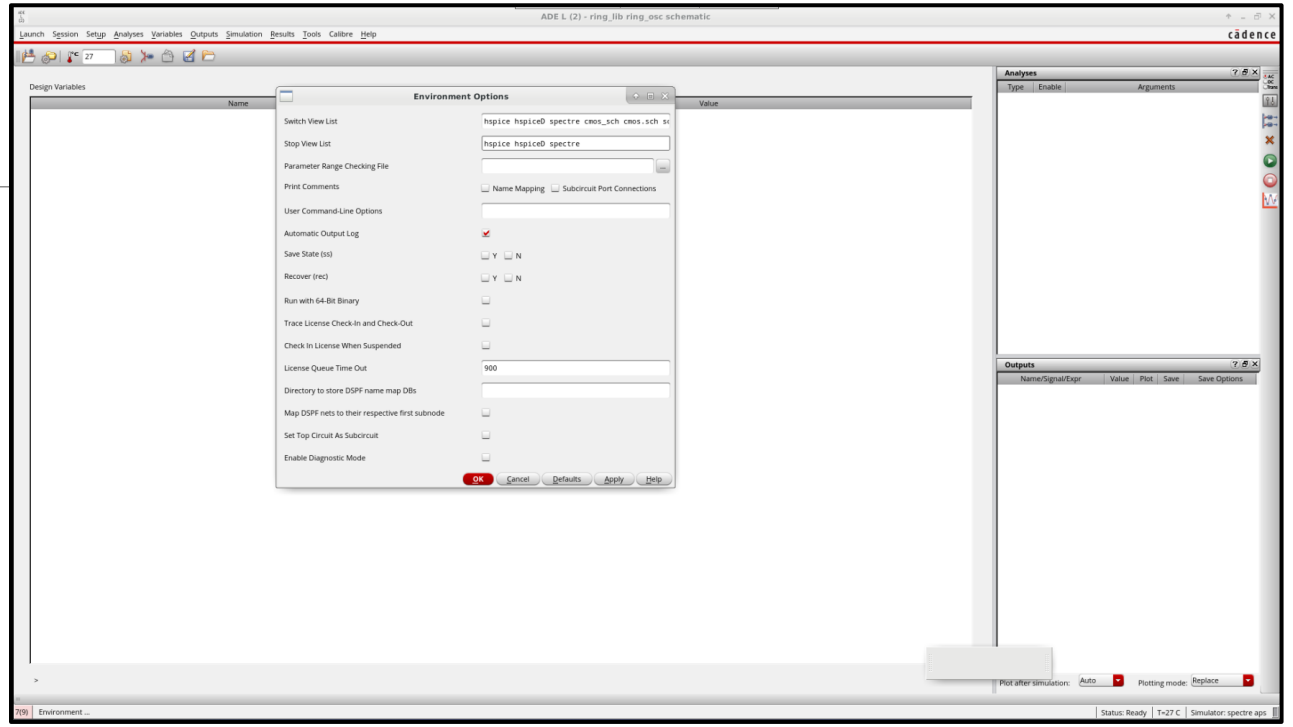


Fig 8: Setting up environment in ADL for simulation

Creating Netlist for Ring Oscillator

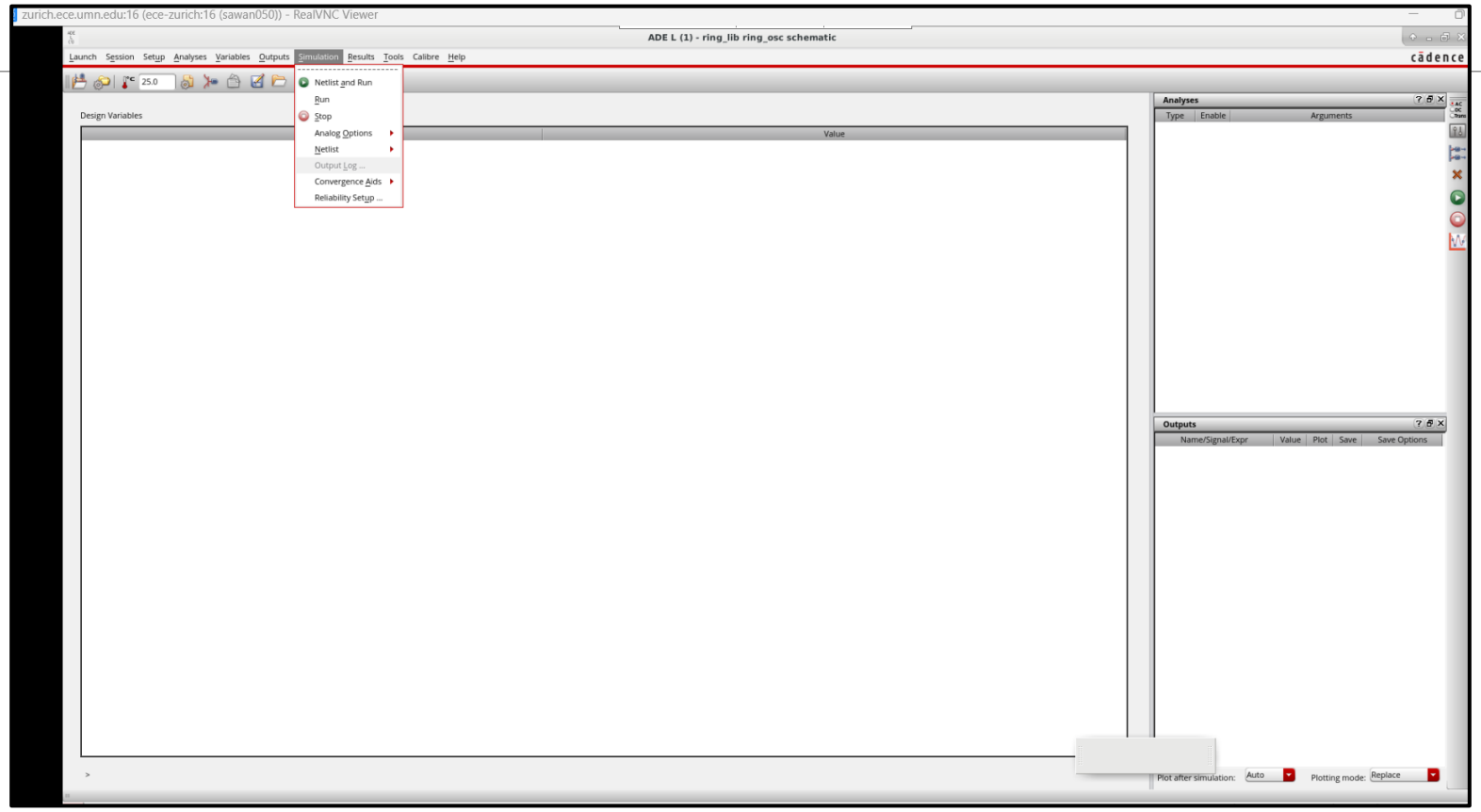


Fig 9: Creating netlist for 99-stage ring oscillator

Netlist generated for ring oscillator as input.ckt file in default simulation folder

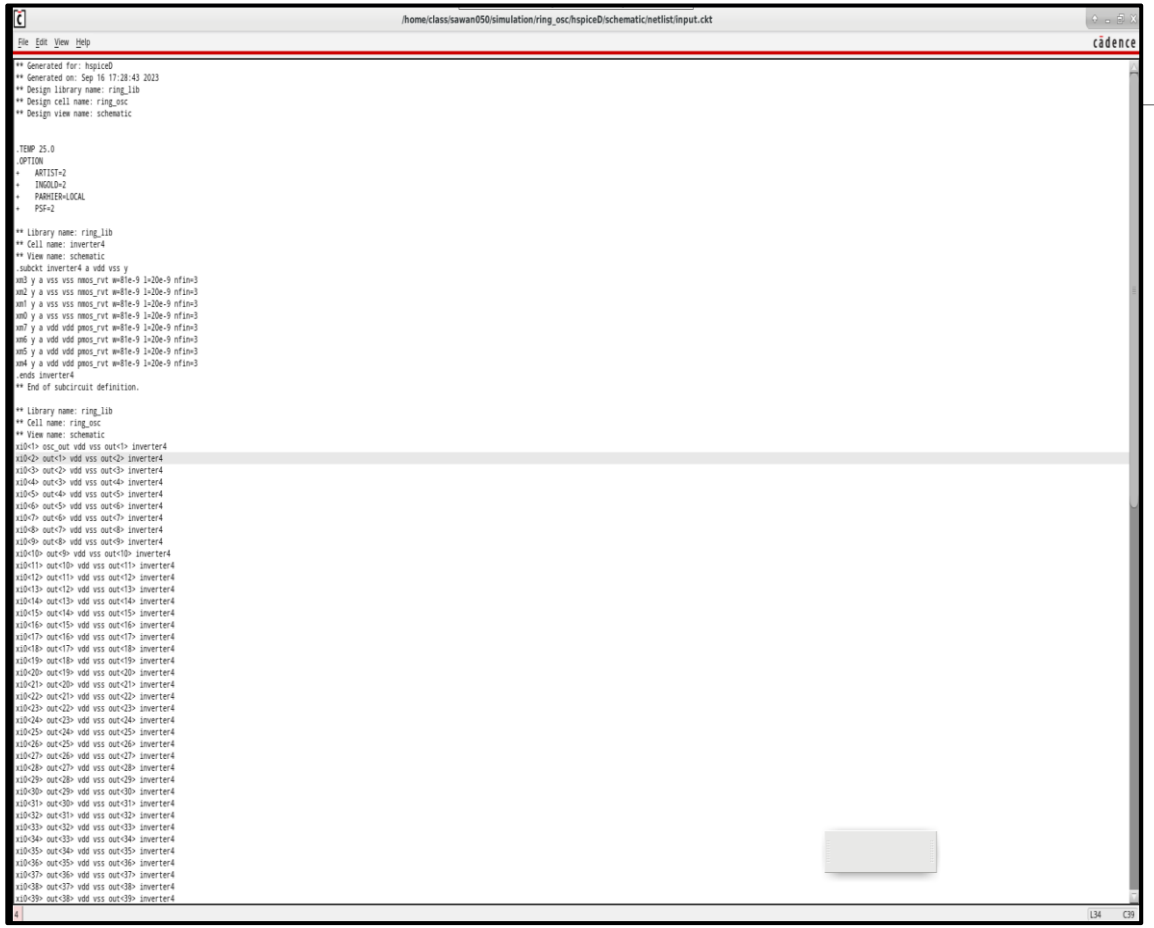


Fig 10: Netlist for ring oscillator before editing

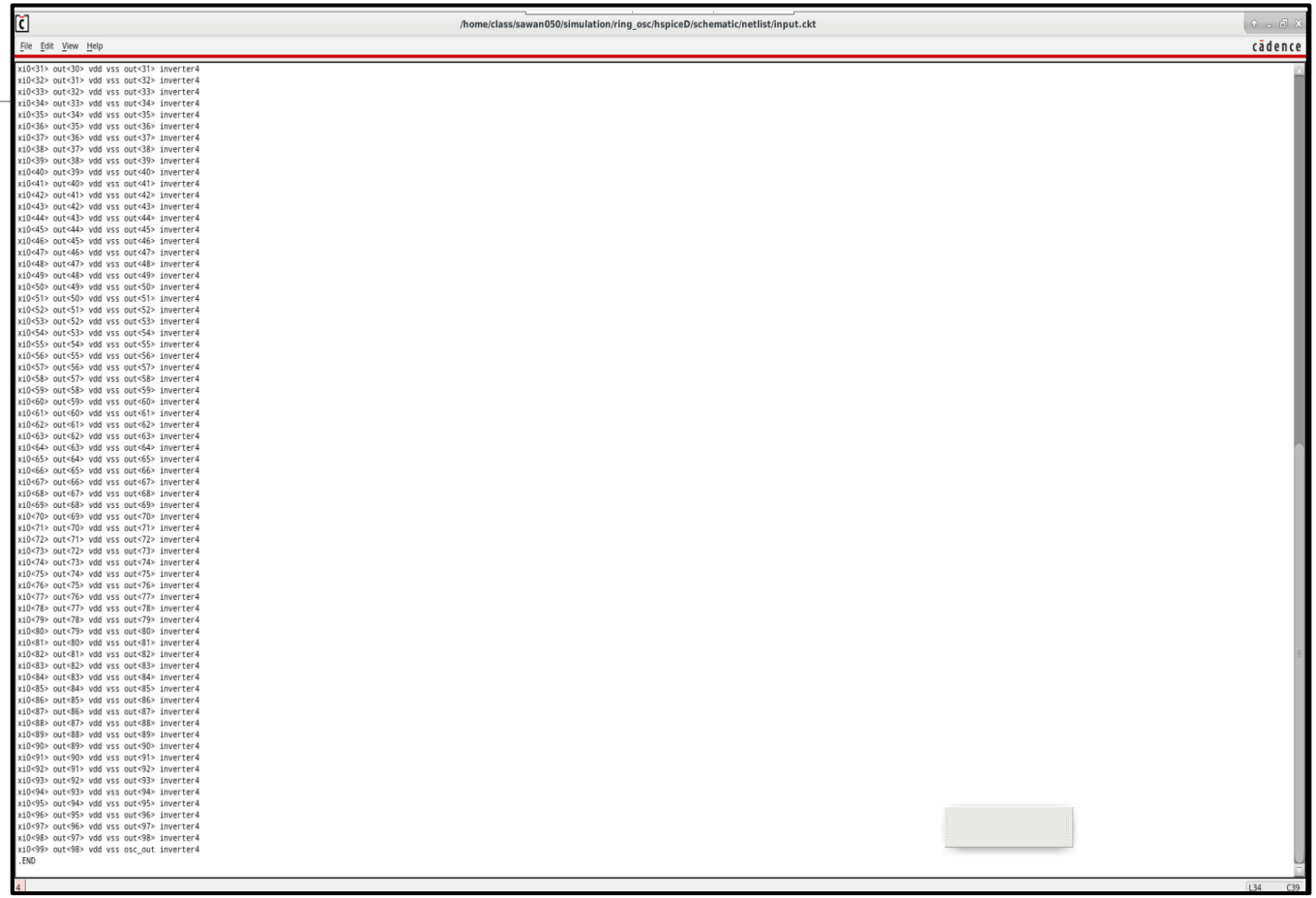


Fig 11: Netlist for ring oscillator before editing

Log File showcasing Netlist Created successfully

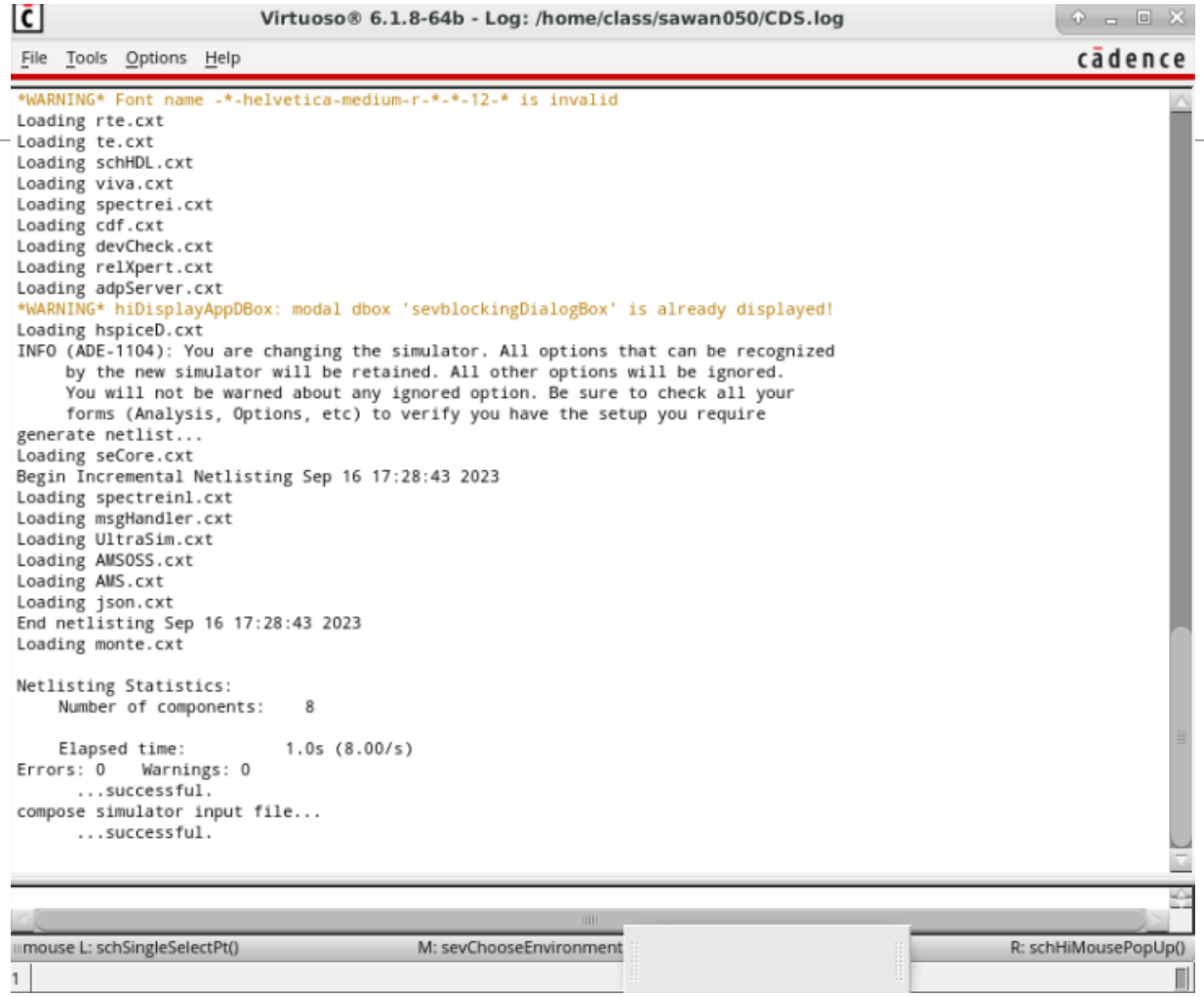


Fig 12: Cadence Log denoting Netlist for ring oscillator created successfully

Netlist generated for ring oscillator as input.ckt file in default simulation folder copying to project directory simulation folder and renaming it as ring_osc.sp

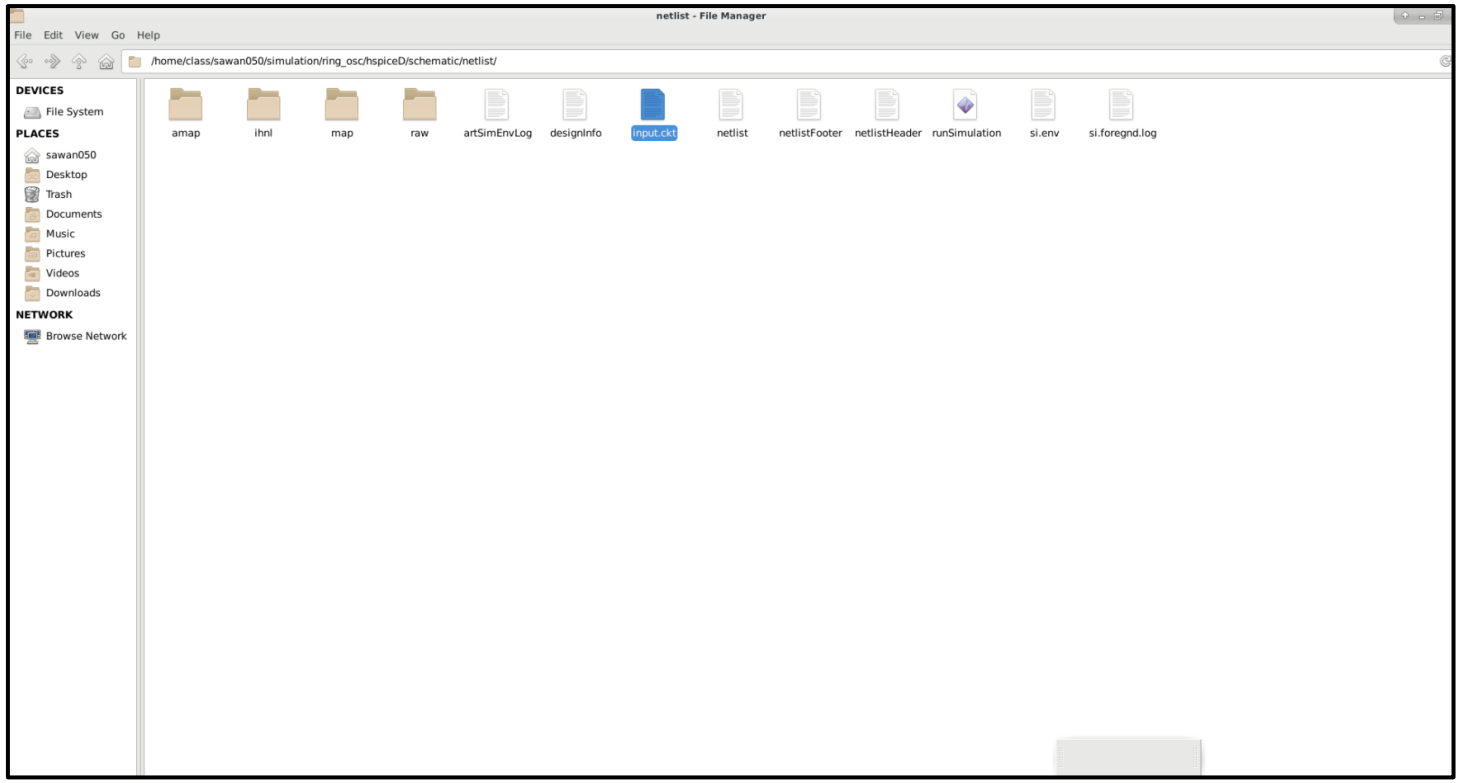


Fig 13: Netlist for ring oscillator and renaming it

Removing the temperature code and x from the gates from netlist file

```
** Generated for: hspiceD
** Generated on: Sep 16 17:28:43 2023
** Design library name: ring_lib
** Design cell name: ring_osc
** Design view name: schematic
.TEMP 25.0
.OPTION
+    ARTIST=2
+    INGOLD=2
+    PARHIER=LOCAL
+    PSF=2
** Library name: ring_lib
** Cell name: inverter4
** View name: schematic
.subckt inverter4 a vdd vss y
xm3 y a vss vss nmos_rvt w=81e-9 l=20e-9 nfin=3
xm2 y a vss vss nmos_rvt w=81e-9 l=20e-9 nfin=3
xm1 y a vss vss nmos_rvt w=81e-9 l=20e-9 nfin=3
xm0 y a vss vss nmos_rvt w=81e-9 l=20e-9 nfin=3
xm7 y a vdd vdd pmos_rvt w=81e-9 l=20e-9 nfin=3
xm6 y a vdd vdd pmos_rvt w=81e-9 l=20e-9 nfin=3
xm5 y a vdd vdd pmos_rvt w=81e-9 l=20e-9 nfin=3
xm4 y a vdd vdd pmos_rvt w=81e-9 l=20e-9 nfin=3
.ends inverter4
** End of subcircuit definition.
** Library name: ring_lib
** Cell name: ring_osc
** View name: schematic
xi0<1> osc_out vdd vss out<1> inverter4
xi0<2> out<1> vdd vss out<2> inverter4
xi0<3> out<2> vdd vss out<3> inverter4
xi0<4> out<3> vdd vss out<4> inverter4
xi0<5> out<86> inverter4
xi0<87> out<86> vdd vss out<87> inverter4
xi0<88> out<87> vdd vss out<88> inverter4
xi0<96> out<95> vdd vss out<96> inverter4
xi0<97> out<96> vdd vss out<97> inverter4
xi0<98> out<97> vdd vss out<98> inverter4
xi0<99> out<98> vdd vss osc_out inverter4
.END
```

Fig 14: Netlist for ring oscillator before editing

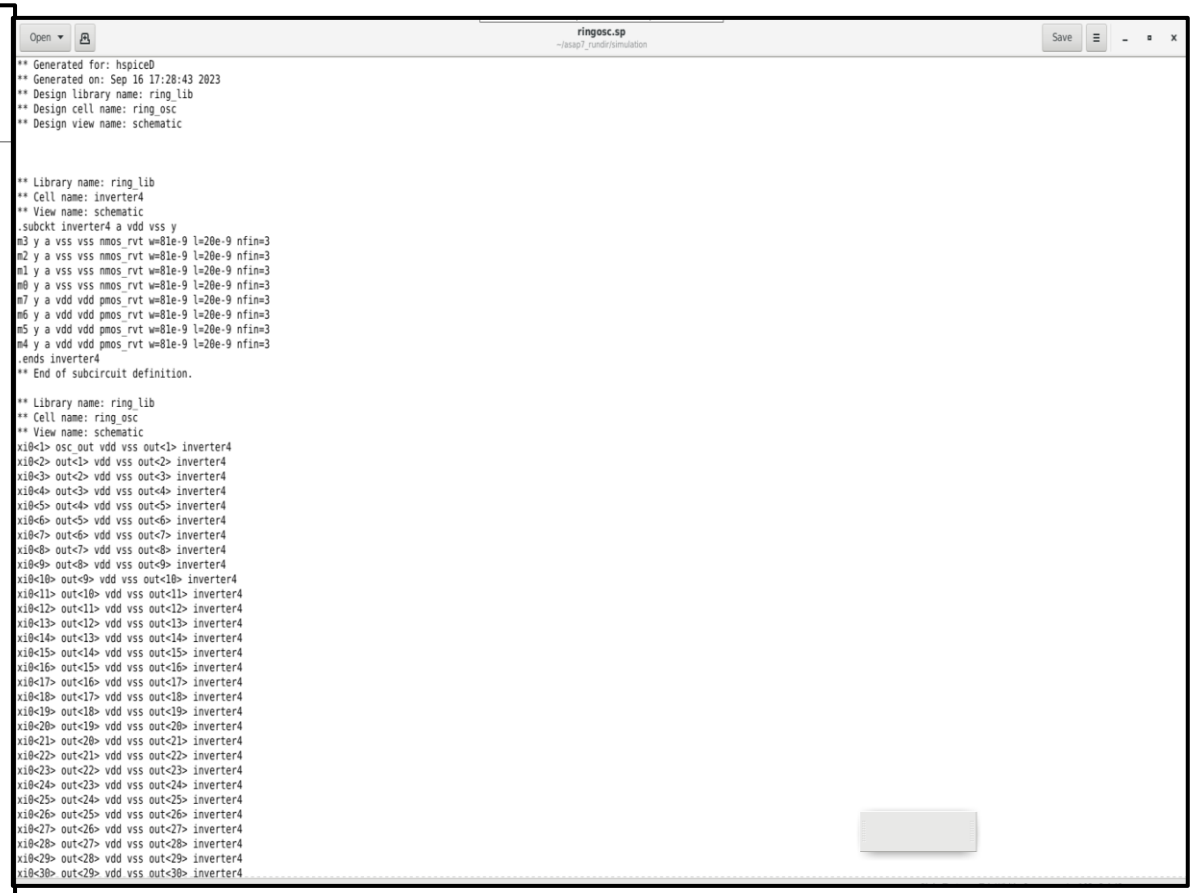


Fig 15: Netlist for ring oscillator after editing

Creating run_ringosc.sp file to run over hspice for analysis

Fig 16: Run simulation file for ring oscillator

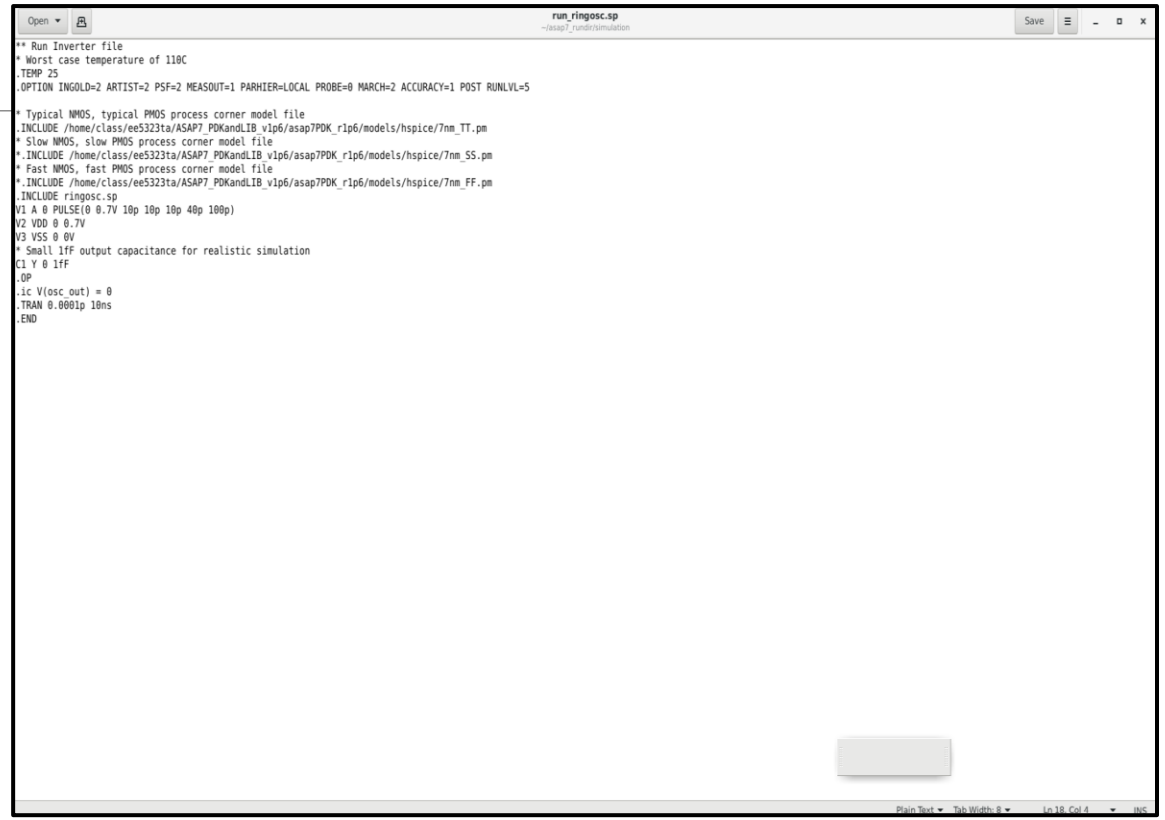


Fig 17: Run simulation file for ring oscillator manipulating it

Process corner = SS (slow), VDD = 0.63V (-10% VDD), Temperature = 110°C,

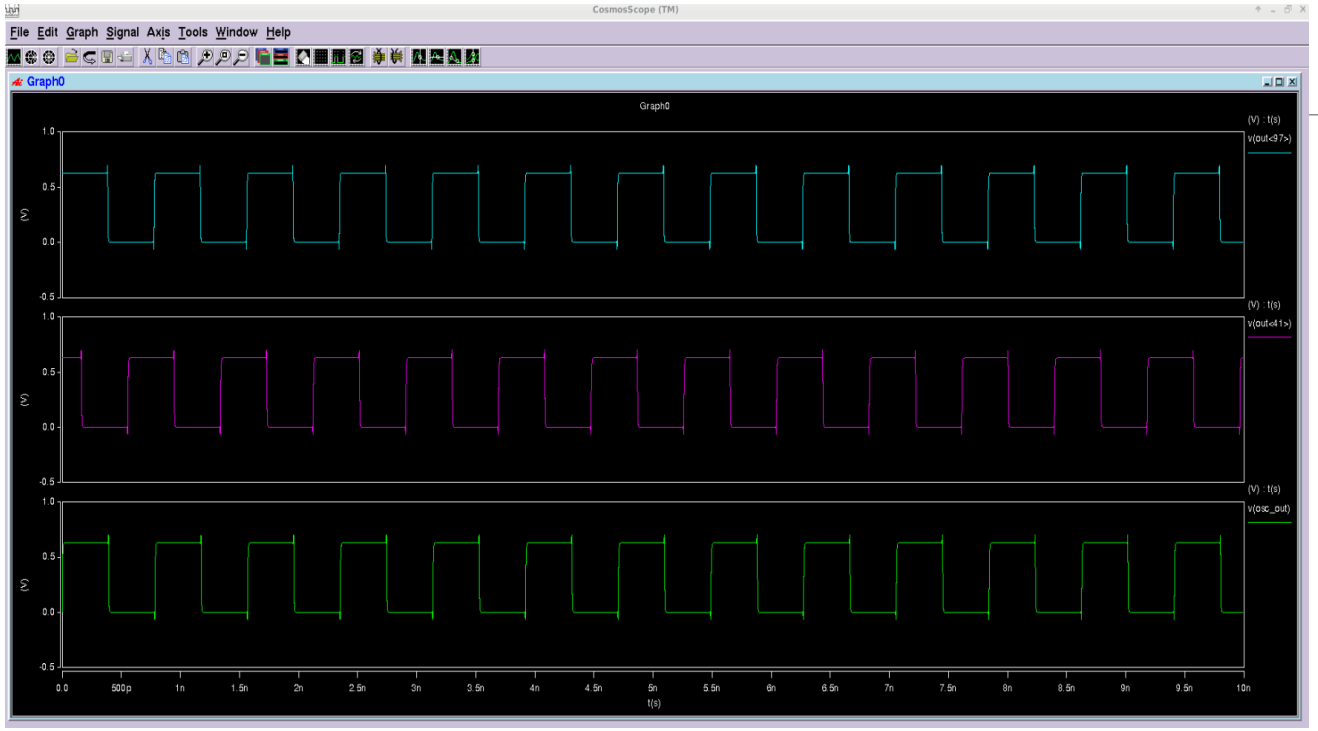


Fig 18: Process corner = SS (slow), VDD = 0.63V (-10% VDD), Temperature = 110°C

```
 cgd       3.191e-17   3.191e-17


******
** run inverter file

****** transient analysis tnom=  25.000 temp= 110.000 ******
period= 7.8931e-10  targ= 2.3616e-09   trig= 1.5723e-09
frequency= 1.2669e+09
iavg=-1.3250e-04  from= 0.0000e+00     to= 1.0000e-08
power=-8.3472e-05

        ***** job concluded
******
** run inverter file

****** job statistics summary tnom=  25.000 temp= 110.000 ******

******  Machine Information  ******
```

Fig 19: freq = 1.266 GHz , Power = -8.3472e-5 W

Process corner = FF (fast),VDD = 0.77V (+10% VDD),Temperature = -40°C

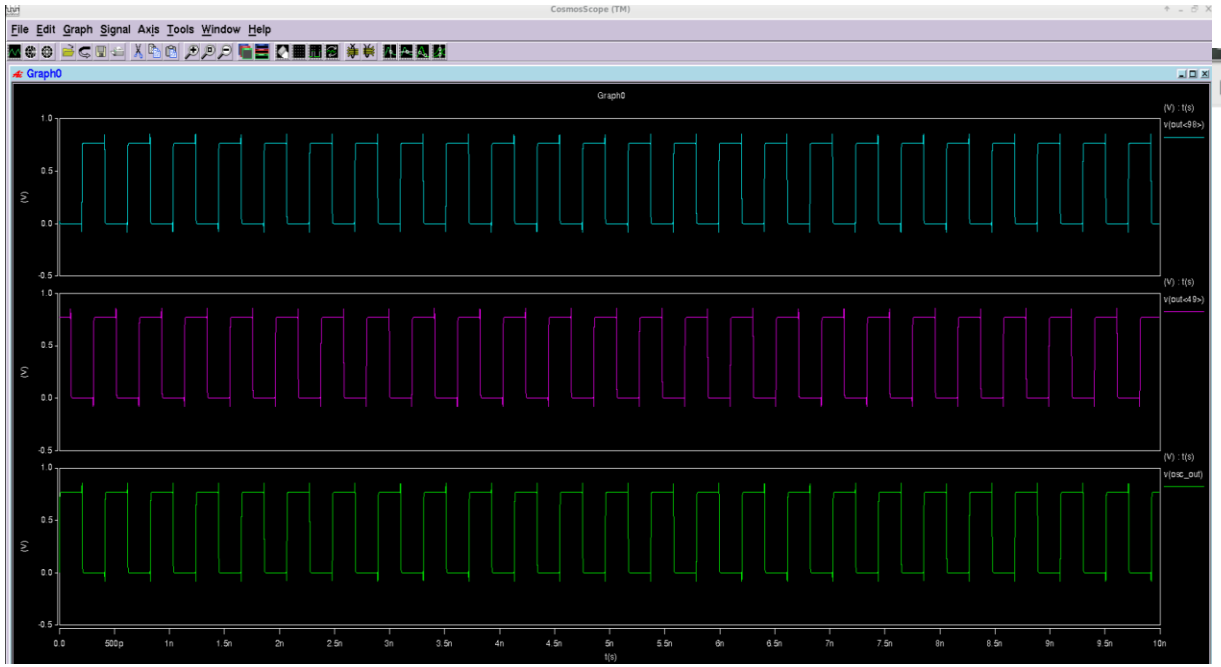


Fig 20: Process corner = FF (fast),VDD = 0.77V (+10% VDD), Temperature = -40°C

```
File  Edit  View  Search  Terminal  Help

****** transient analysis tnom=  25.000 temp= -40.000 ******
period= 4.1385e-10  targ= 1.2419e-09   trig= 8.2804e-10
frequency= 2.4164e+09
iavg=-4.0540e-04  from= 0.0000e+00     to= 1.0000e-08
power=-3.1216e-04

         ***** job concluded
******
** run inverter file

****** job statistics summary tnom=  25.000 temp= -40.000 ******

******  Machine Information  ******
CPU:
model name      : Intel(R) Xeon(R) Silver 4208 CPU @ 2.10GHz
cpu MHz         : 799.932
```

Fig 21: freq = 2.4164GHz , Power = -3.1216e-4 W

Process corner = TT (typical, i.e. nominal), VDD = 0.7V (-10% VDD), Temperature = 25°C (nominal),

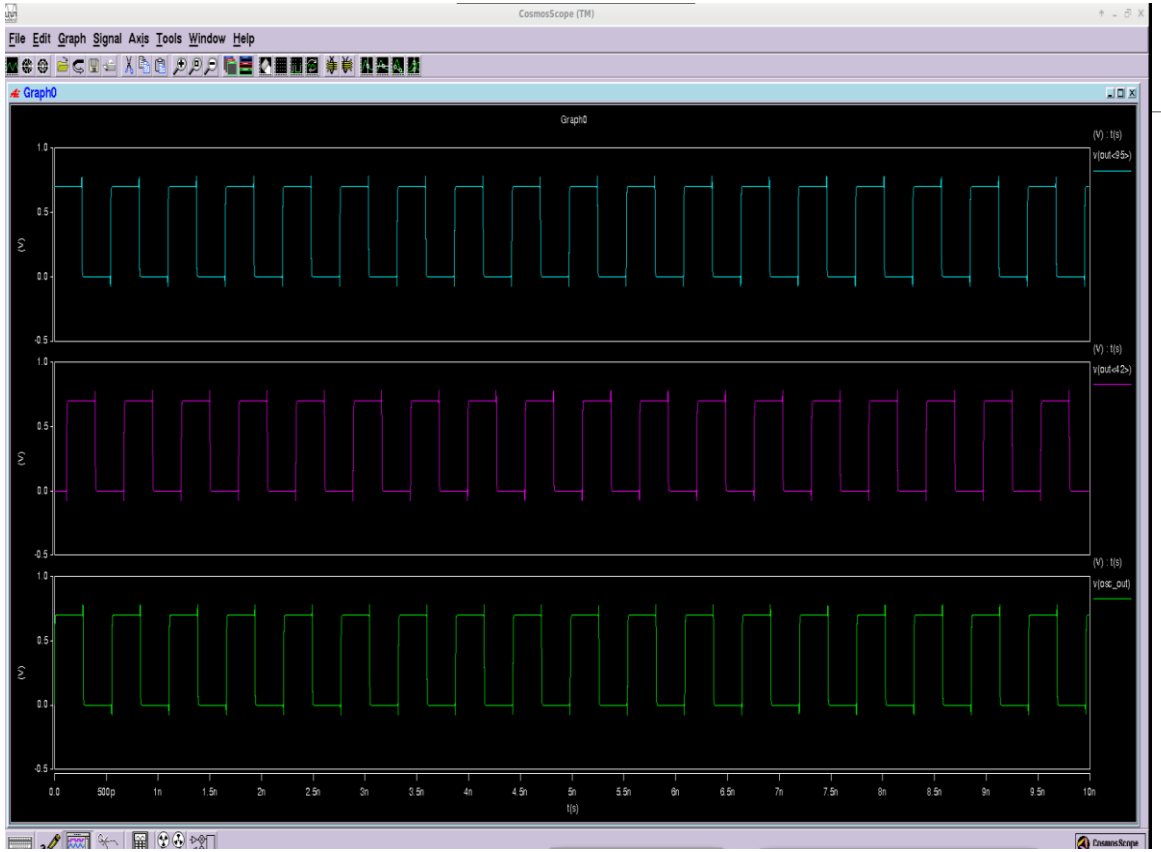


Fig 22: Process corner = TT (typical, i.e. nominal), VDD = 0.7V (-10% VDD), Temperature = 25°C (nominal),

```
File  Edit  View  Search  Terminal  Help
** run inverter file

****** transient analysis tnom=  25.000 temp=  25.000 ******
period= 5.5464e-10  targ= 1.6636e-09   trig= 1.1090e-09
frequency= 1.8030e+09
iavg=-2.3484e-04  from= 0.0000e+00     to= 1.0000e-08
power=-1.6439e-04

        ***** job concluded
******
** run inverter file

****** job statistics summary tnom=  25.000 temp=  25.000 ******
```

Fig 23: freq = 1.803 GHz , Power = -1.6439e-4 W

VDD= 0.7 , Process corner = tt, Temperature = 110

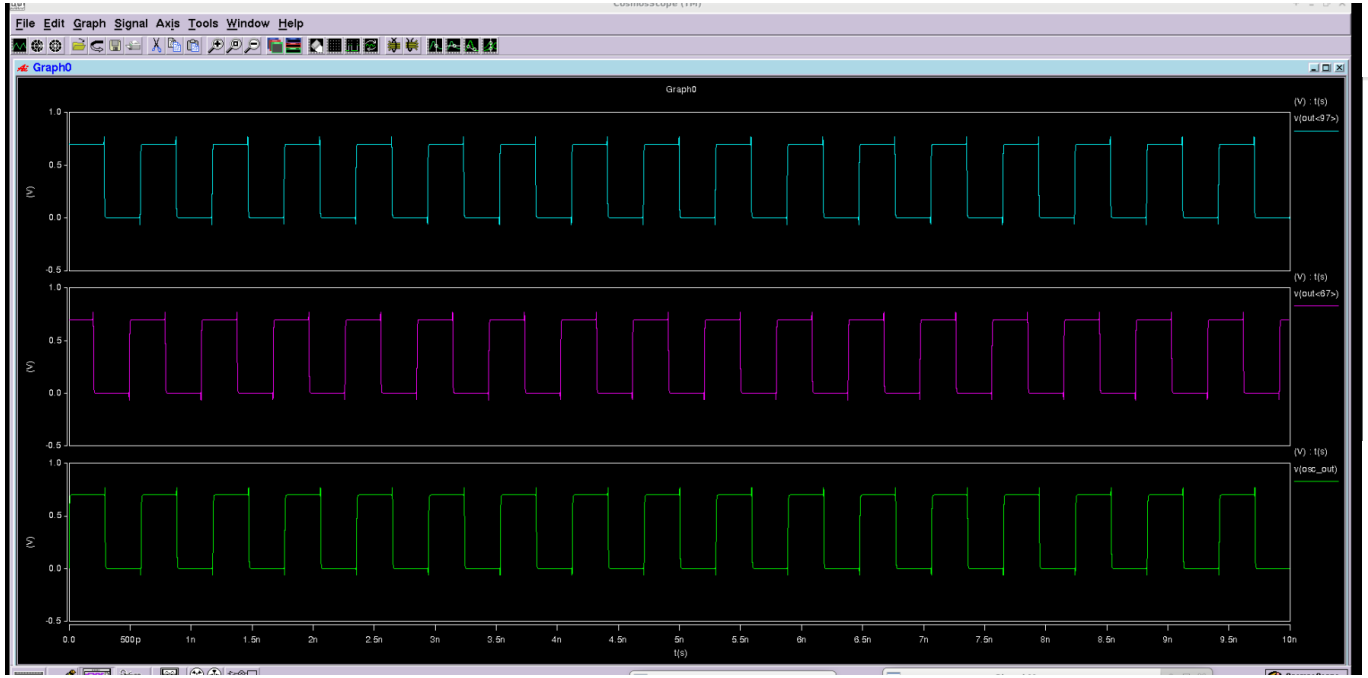


Fig 24: VDD= 0.7 , Process corner = tt, Temperature = 110

```
** run inverter file

****** transient analysis tnom=  25.000 temp= 110.000 ******
period= 5.9016e-10  targ= 1.7701e-09   trig= 1.1800e-09
frequency= 1.6945e+09
iavg=-2.2468e-04  from= 0.0000e+00     to= 1.0000e-08
power=-1.5728e-04

         ***** job concluded
******
** run inverter file

****** job statistics summary tnom=  25.000 temp= 110.000 ******
```

Fig 25: freq = 1.6945 GHz , Power = -1.57282e-4 W

Process corner = Tt , VDD = 0.7 , Temperature = -40

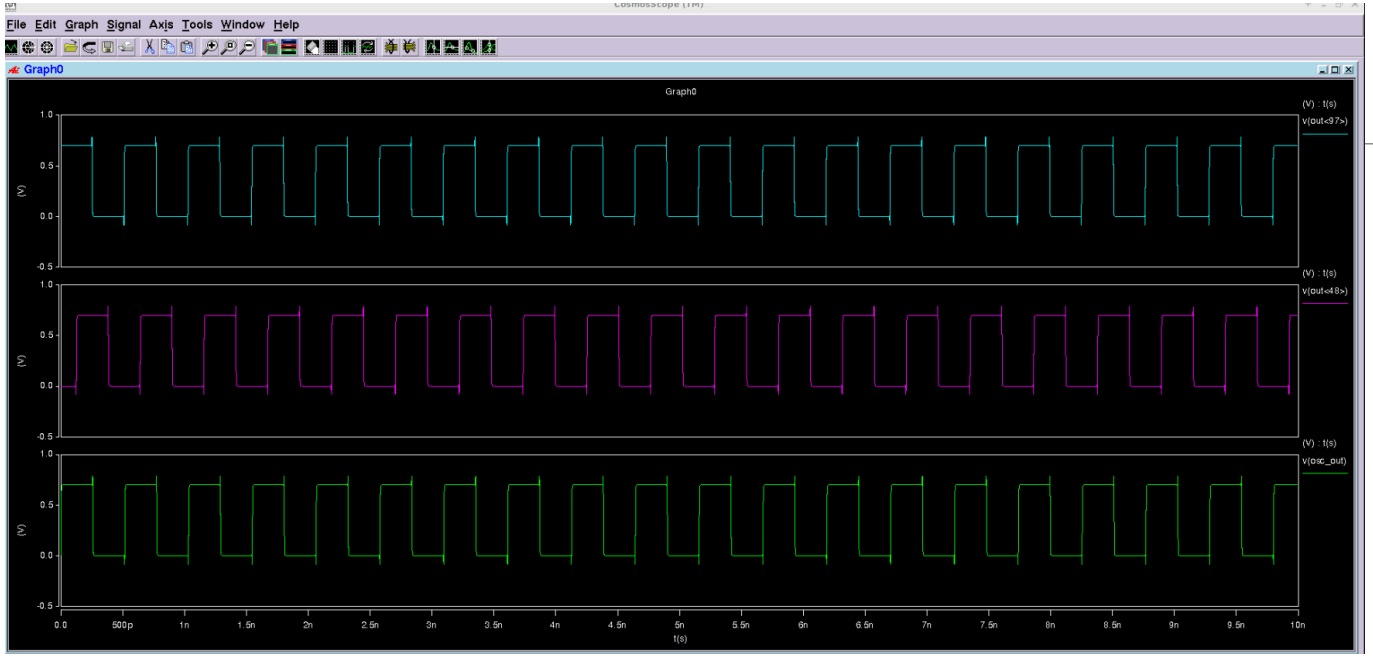


Fig 26: Process corner = Tt , VDD = 0.7 , Temperature = -40

```
File  Edit  View  Search  Terminal  Help
** run inverter file

****** transient analysis tnom=  25.000 temp= -40.000 ******
period= 5.1684e-10  targ= 1.5503e-09   trig= 1.0335e-09
frequency= 1.9348e+09
iavg=-2.5120e-04  from= 0.0000e+00     to= 1.0000e-08
power=-1.7584e-04

         ***** job concluded
******
** run inverter file

****** job statistics summary tnom=  25.000 temp= -40.000 ******

******  Machine Information  ******
CPU:
model name      : Intel(R) Xeon(R) Silver 4208 CPU @ 2.10GHz
```

Fig 27: freq =1.9348GHz , Power = -1.7584e-4 W

Process corner = Tt, VDD = 0.63, Temperature = 25

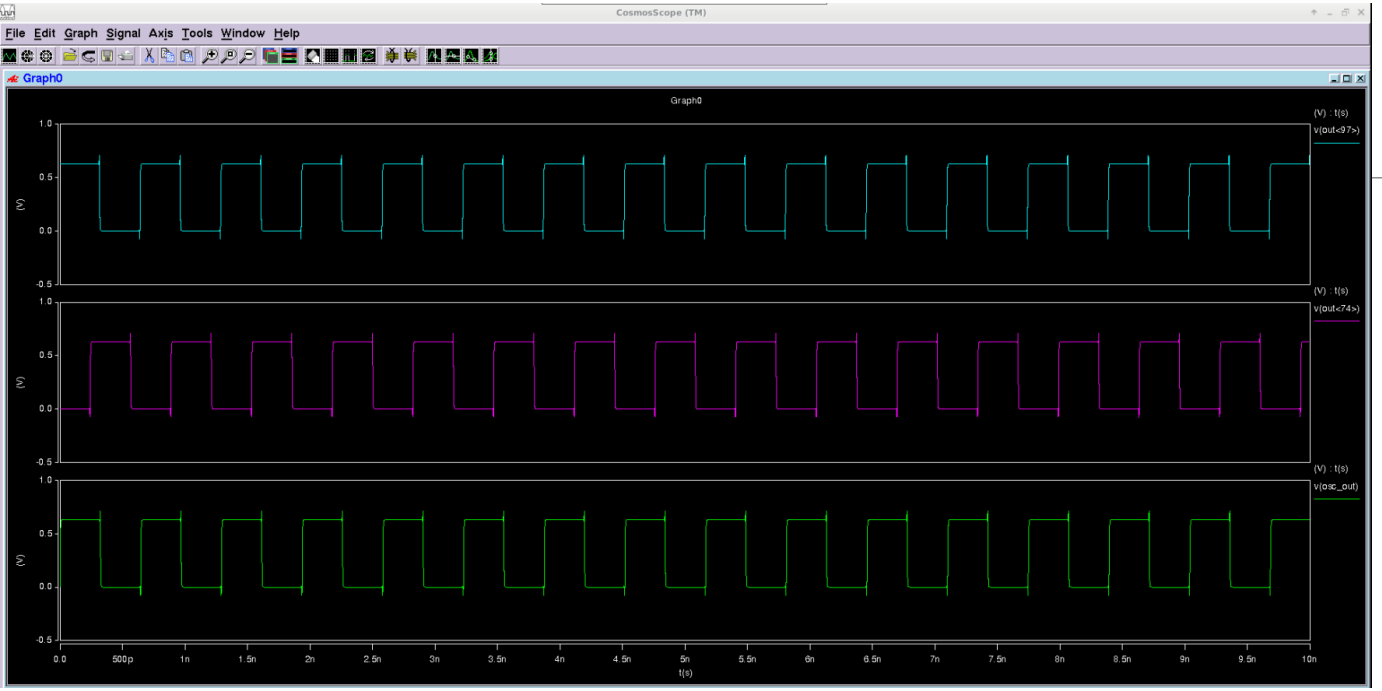
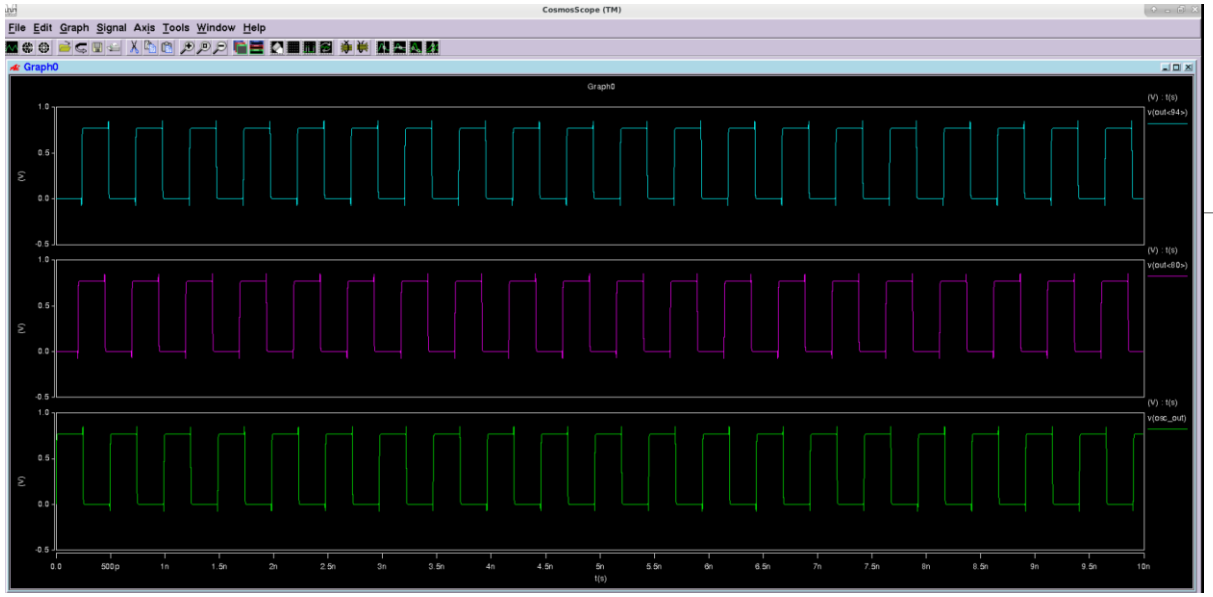


Fig 28: Process corner = Tt, VDD = 0.63, Temperature = 25

```
File  Edit  View  Search  Terminal  Help
** run inverter file

****** transient analysis tnom=  25.000 temp=  25.000 ******
period= 6.4978e-10  targ= 1.9439e-09   trig= 1.2941e-09
frequency= 1.5390e+09
iavg=-1.7589e-04  from= 0.0000e+00     to= 1.0000e-08
power=-1.1081e-04

         ***** job concluded
******
** run inverter file

****** job statistics summary tnom=  25.000 temp=  25.000 ******

******  Machine Information  ******
CPU:
model name      : Intel(R) Xeon(R) Silver 4208 CPU @ 2.10GHz
cpu MHz         : 2983.886
```

Fig 29: freq = 1.539 GHz , Power = -1.1081e-4 W

Process corner = Tt, VDD = 0.77, Temperature = 25




```
File  Edit  View  Search  Terminal  Help
** run inverter file

****** transient analysis tnom=  25.000 temp=  25.000 ******
period= 4.9578e-10  targ= 1.4877e-09   trig= 9.9193e-10
frequency= 2.0170e+09
iavg=-2.9609e-04  from= 0.0000e+00     to= 1.0000e-08
power=-2.2799e-04

         ***** job concluded
******
** run inverter file

****** job statistics summary tnom=  25.000 temp=  25.000 ******
```

Fig 30: Process corner = Tt, VDD = 0.77, Temperature = 25

Fig 31: freq = 2.017 GHz , Power = -2.2799e-4 W

Process corner = Ss, VDD = 0.7, Temperature = 25

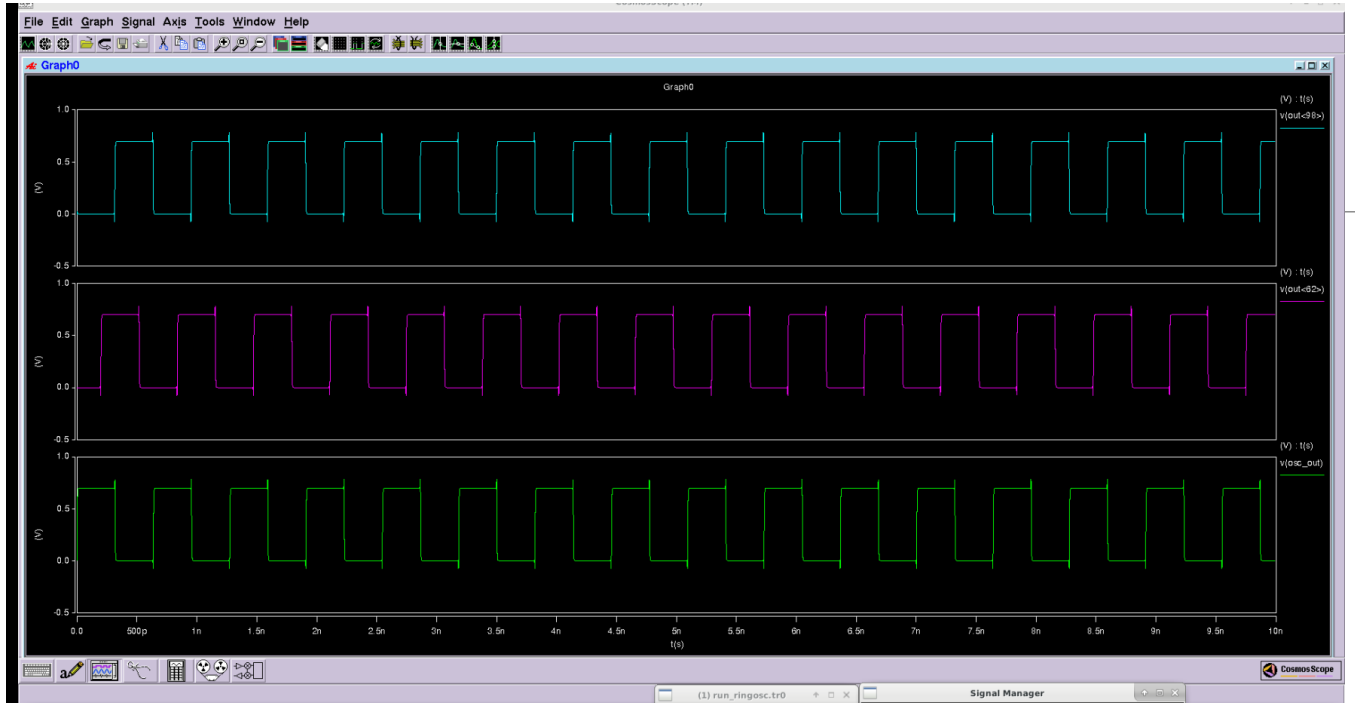


Fig 32 : Process corner = Ss, VDD = 0.7, Temperature = 25

```
File  Edit  View  Search  Terminal  Help
** run inverter file

****** transient analysis tnom=  25.000 temp=  25.000 ******
period= 6.3808e-10  targ= 1.9140e-09   trig= 1.2759e-09
frequency= 1.5672e+09
iavg=-1.8279e-04  from= 0.0000e+00     to= 1.0000e-08
power=-1.2795e-04

         ***** job concluded
******
** run inverter file

****** job statistics summary tnom=  25.000 temp=  25.000 ******
```

Fig 33 : freq = 1.5672 GHz , Power = -1.2795e-4 W

Process corner = Ff, VDD = 0.7, Temperature = 25

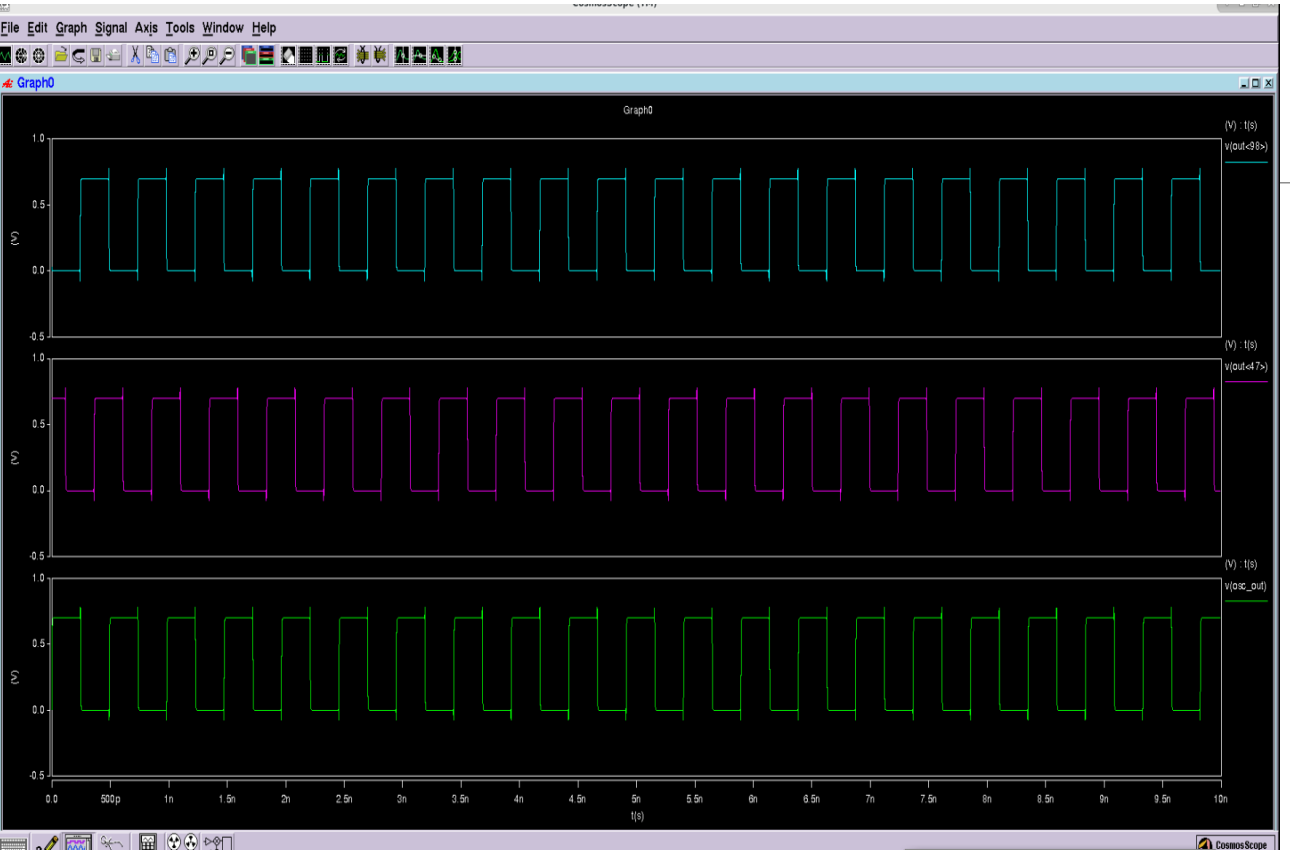


Fig 34: Process corner = Ff, VDD = 0.7, Temperature = 25

```
File  Edit  View  Search  Terminal  Help
** run inverter file

****** transient analysis tnom=  25.000 temp=  25.000 ******
period= 4.9215e-10  targ= 1.4762e-09   trig= 9.8402e-10
frequency= 2.0319e+09
iavg=-3.0136e-04  from= 0.0000e+00     to= 1.0000e-08
power=-2.1095e-04

         ***** job concluded
******
** run inverter file

****** job statistics summary tnom=  25.000 temp=  25.000 ******

******  Machine Information  ******
```

Fig 35: freq = 2.0319 GHz , Power = -2.1095e-5 W

Analysis

Process Corner	Voltage	Temperature	Frequency and Power
ff	.7	25	*freq = 2.0319 GHz , Power = -2.1095e-5 W*
ss	.7	25	*freq = 1.5672 GHz , Power = -1.2795e-4 W*
tt	.77	25	*freq = 2.017 GHz , Power = -2.2799e-4 W*
tt	.63	25	*freq = 1.539 GHz , Power = -1.1081e-4 W*
tt	.7	-40	*freq =1.9348GHz , Power = -1.7584e-4 W*
tt	.7	110	*freq = 1.6945 GHz , Power = -1.57282e-4 W*
tt.	.7	25	*freq = 1.803 GHz , Power = -1.6439e-4 W*
ff	.77	-40	*freq = 2.4164GHz , Power = -3.1216e-4 W*
ss	.63	110	*freq = 1.266 GHz , Power = -8.3472e-5 W*

Conclusion

The frequency and power characteristics of such an oscillator can vary at different process corners due to the following reasons:

1. **Supply Voltage Variation:** At different process corners, the supply voltage can vary. In the low voltage corner (LL), the supply voltage is lower, which can result in slower operation and lower power consumption. In the high voltage corner (HH), the supply voltage is higher, which can lead to faster operation and higher power consumption.
2. **Temperature Variation:** Process corners also consider variations in temperature. Higher temperatures can lead to increased resistance and slower transistor operation, affecting the frequency and power consumption of the oscillator.

- The schematic corresponding to the INVx4_ASAP7_75t_R layout was successfully drawn in Virtuoso. This layout was used as a fundamental building block for the subsequent ring oscillator design.
- Ring Oscillator Design: A 99-stage ring oscillator was designed in Virtuoso using the inverter symbol
- This assignment allowed for practical experience in designing and analyzing digital circuits, considering the impact of variations in process, voltage, and temperature on circuit performance.