Department of Electronics & Communication Engineering

(Faculty of Technology, Dharmsinh Desai University, Nadiad)

Academic Year: 2022 - 2023

TUTORIAL – 11

Subject : *PHYSICS (Module- 6)*
Class : *B. Tech. Sem.II (EC/IT)*

Q.1 Select the most appropriate option.

(1) An ordinary resistor is an example of _____
(I) a three-terminal device (II) an active load
(III) a passive load (IV) a switching device

(2) An E-MOSFET that operates at cutoff or in the ohmic region is an example of ____
(I) a three-terminal device (II) an active load
(III) a passive load (IV) a switching device

(3) CMOS stands for _____
(I) Common MOS (II) Active-load switching
(III) Complementary MOS (IV) none of the above

(4) The main advantage of CMOS is its _____
(I) switching capability (II) low-power consumption
(III) high-power rating (IV) small-signal operation

(5) When the gate-to-source voltage (V_{GS}) of a E-MOSFET with threshold voltage of 400 mV, working in saturation is 900 mV, the drain current is observed to be 1 mA. Assuming that the MOSFET is operating at saturation, the drain current for an applied V_{GS} of 1400 mV is _____
(I) 0.5 mA (II) 2 mA (III) 3.5 mA (IV) 4 mA

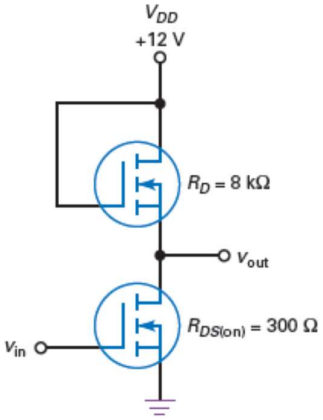
(6) Two n-channel E-MOSFETs, T1 and T2, are identical in all respects except that the width of T2 is double that of T1. Both the transistors are biased in the saturation region of operation, but the voltage (V_{GS}-V_{TH}) of T2 is double that of T1, where V_{GS} and V_{TH} are the gate – to – source voltage and threshold voltage of the transistors, respectively. If the drain current of T1 is I_{D1}, the corresponding value of this parameter for T2 is _____
(I) $2I_{D1}$ (II) $4I_{D1}$ (III) $8I_{D1}$ (IV) $32I_{D1}$

Q.2 Do as Directed (Descriptive Answers, Examples etc)

(1) An E-MOSFET has these values: $I_{D(active)}$ = 1 mA and $V_{DS(active)}$ = 10 V. What does its drain resistance equal in the active region? 10k

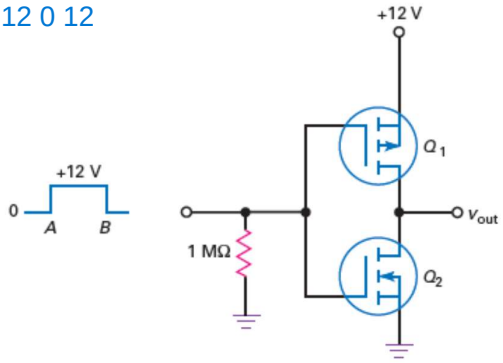
(2) What is the output voltage for the circuit shown in figure below, when the input is (a) low (b) high? A square wave drives the gate of circuit shown in figure below. If the square wave has a peak-to-peak value large enough to drive the lower MOSFET into the ohmic region, what is the output waveform?

12 & 0.4337



(3) The MOSFETs of figure below have $R_{DS(on)} = 250\ \Omega$ and $R_{DS(off)} = 5\ M\Omega$. What is the output waveform?

12 0 12



(4) An nFET with W = 10μm and L = 0.35 μm is built in a process where $k_n' = 110\ \mu A/V^2$ and $V_{Tn} = 0.7$ V.

(a) Find the drain current if the voltages are set to $V_{GSn} = 2$ V, $V_{DSn} = 1$ V. 2.5m

(b) Find the drain current if the voltages are set to $V_{GSn} = 2$ V, $V_{DSn} = 2$ V. 2.65m

(5) A CMOS inverter is built in a process where $k_n' = 100\ \mu A/V^2$, $k_p' = 42\ \mu A/V^2$, $V_{Tn} = +0.70$V and $V_{Tp} = -0.80$V and a power supply of 3.3 V is used . Find the midpoint voltage V_M if $(W/L)_n = 10$ and $(W/L)_p = 14$. 1.3665

(6) A DRAM cell has a storage capacitance of $C_S = 45$ fF. It is used in a system where $V_{DD} = 3.3$ V and $V_{Tn} = 0.55$ V. The bit line capacitance is $C_{bit} = 250$ fF.

(a) Find the maximum amount of charge that can be stored on C_S. 123.7f

(b) Suppose that the voltage on the capacitor is charged to a level of V_{max}. The word line controlling the access FET is dropped to a value WL = 0 at time t = 0. The leakage current is estimated to be 50 nA. To detect a logic 1 state, the voltage on the bit line must be at least 1.5 V. Find the hold time. 0.8u

(7) Consider a DRAM cell that has a storage capacitance of $C_S = 55$ fF. The power supply is $V_{DD} = 3$ V and the access FET has a threshold voltage of $V_{Tn} = 0.65$V. The leakage current from the storage capacitor is estimated to be 250 pA and the bit capacitance is $C_{bit} = 420$ fF. The capacitor has voltage V_{max} across it when the word line is brought low at time t = 0. A read operation is initiated at time t = 10 ms by elevating the word line up to a value of WL = 1. Find the voltage on a bit line. 0.2721