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Objective

To develop my career in semiconductor industry as an Analog Design Engineer.

Industry Exposure

Worked as an intern in GlobalFoundries, Bengaluru with OPC team, USTO org **[Feb'17- June'17]**

- **Project 1:** Optimization of xor script in terms of runtime and various functionality by applying a wrapper around dbdiff utility of calibre **Guided by**- Jeremy Ingle/Pardeep Kumar
- **Project 2:** Learn SVRF commands, ORC code & limits and try optimizations in ORC code and limits in order to improve the autopass percentage in various nodes **Guided by**- Priyanka Mantripragada

Working as a Regular Employee (Senior Engineer) in GlobalFoundries, Bengaluru with Mask data preparation (MDP) team. **[July'17- Present]**

- We send final data to Mask house for fabrication. Before sending data to mask house, we need to launch DSDP and ensure that DSDP is correctly validated with the given specification.

Education

Master of Technology (Microelectronics and VLSI)	IIT Gandhinagar	8/10	2015-2017
Bachelor of Engineering (Electronics and comm)	SSBT COET Jalgaon	8.04/10	2009-2013
HSC	TPS College Patna	69.44/100	2006-2008
SSC	High School Fatuha	72.13/100	2005-2006

2013-2015: I was working as an online tutor of chegg corporation for Mathematics and Basic Technical subjects related to electronics..

Publications

- Neha Kumari, J.Mekie "Upset Hardened Latch as Data Synchronizer" 2017 IEEE Electron Devices and Solid State Circuits (EDSSC'17), Taiwan. (Accepted) **[July'17]**
- J.Mekie, Neha kumari, Fathima sinin " Characterizing Metastability in different synchronizer ",23rd IEEE International Symposium on Asynchronous Circuits and System 2017, California (Under process)

Technical Skills

- **Tools-** Cadence virtuoso(IC 6.1.5) EDA tools, Synopsys EDA tools, Mentor-Graphics EDA tools, Xilinx ISE, Sentaurus TCAD, Hspice.
- **Programming Language-** Verilog, VHDL, Tcl, Perl, Shell Scripting, Mysql, C, C++, and MATLAB.

Relevant CourseWork

VLSI Design	CMOS analog IC Design	Physics Of Transistors
FinFET Design: Challenges and opportunity	Electronic Circuit Design	Electronic devices and circuits
Nanoscale devices	Microprocessor & µC	Digital circuits

Position Of Responsibility

- Teaching Assistant for Analog circuits Lab and "electrical and electronics lab" **[July'15- Feb'17]**
- Class Representative for M.Tech and Ph.D for Electrical Department **[July'15- Apr'16]**

Projects

- **Impact of Process variations and Technology scaling on synchronizer performance: M.Tech Thesis | guided by- Prof. Joycee Mekie [May'16- July'17]**
    - Impact of process variations on metastability resolution parameters of three different kinds of flip-flops; Standard DFF, a metastable hardened Pseudo-NMOS FF, a SEU-tolerant DICE FF has been observed in 180nm, 130nm, 90nm, 65nm, 40nm, 28nm technology node using cadence virtuoso and spectre simulator.
    - Impact of technology scaling on metastability resolution parameters of three different kinds of flip-flops; Standard DFF, a metastable hardened Pseudo-NMOS FF, a SEU-tolerant DICE FF has been observed in 180nm, 130nm, 90nm, 65nm, 40nm, 28nm MOSFET UMC process using cadence virtuoso and spectre simulator and 20nm, 16nm, 14nm, 10nm and 7nm FinFET PTM process using HSPICE simulator.
- **Design of Single Stage Fully Differential Telescopic OPAMP in cadence virtuoso [Apr'16]**
    - The schematic has been implemented in 180nm technology and managed the circuit to achieve the required specification- PD: 30 uW, GBW: 10 MHz, Gain > 3000 V/V, CMRR > 100dB, Out, Vdd:0.9V.
- **Design of cascode amplifier using PMOS current source load, PMOS current mirror load, PMOS wide swing current mirror load in cadence virtuoso [Mar'16]**
    - The schematic has been implemented in 180nm technology and managed the circuit to achieve the required specification- Gain= 5000(75dB), UGB= 60 MHz, PD= 0.3mW, Iref = 10uA, VDD = 1.8V

- **Design of 16 bit Zero Detector circuit in cadence virtuoso [Nov'15]**
    - Area, Power, Delay, PDP, EDP analysis using Static-CMOS (OR), Static-CMOS (AND) and Pseudo-NMOS in 65nm technology
- **Design of Low Power digital circuits using Asymmetric FinFET [Apr'16]**
    - Design and Analysis of inverter, NAND and NOR gates are being done in terms of power, delay and PDP for various asymmetric underlap and asymmetric gate oxide thickness of FinFET device
- **Characterization of FinFET with and without hydrodynamic model, 3D vs 2D Comparison and parametric analysis of 2D FinFET [Feb'16]**
    - Analysis of Ion, Ioff, SS, DIBL is done for both n-FinFET and p-FinFET
    - An accurate 2D model of FInFET device is made which can capture the 3D simulation accuracy
    - Analysis of Ion, Ioff, SS, DIBL has been done for n-FinFET and p-FinFET for different gate length, work-function, underlap length and Fin thickness
- **Design & Implementation of Random number generator and sequence detector on FPGA [May'16]**
    - 3-bit pseudo random number generator is being made and 1010 sequence is being detected on FPGA
- **Design and implementation of cordic algorithm on FPGA [Aug'15]**
    - Implemented sine and cosine function using look up table and standard approach.

Interests

- Games- Carrom, Badminton and Table Tennis
- Travelling, Cooking