Sequential Circuits

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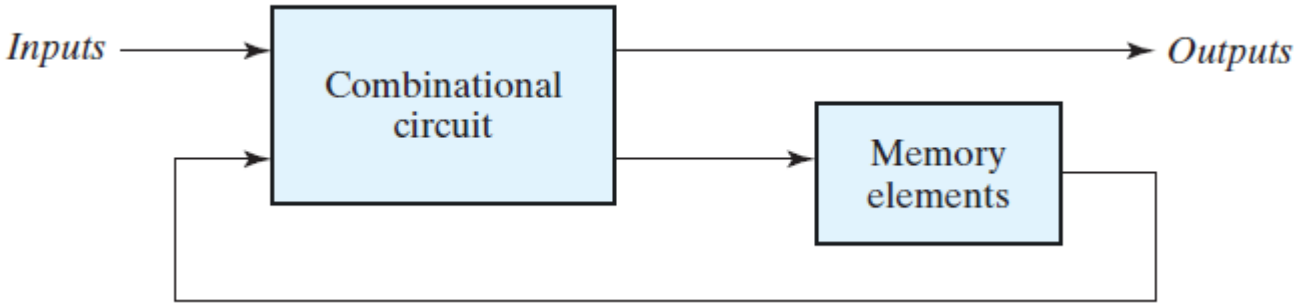
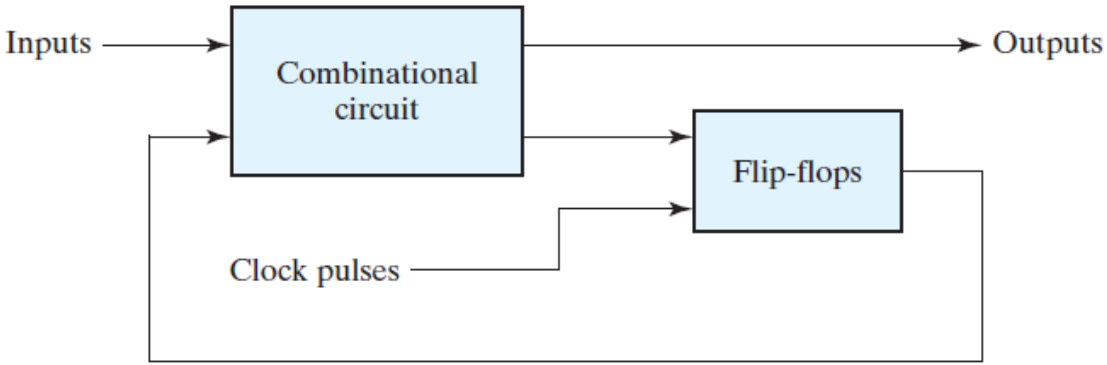


1. Synchronous Sequential Circuit
2. Asynchronous Sequential Circuit

Synchronous Clocked sequential Circuits



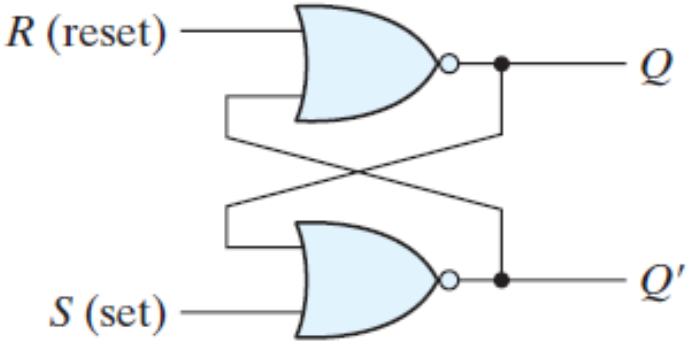
(a) Block diagram

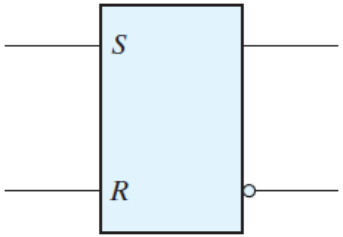
(b) Timing diagram of clock pulses

Storage Elements : Latches

S-R Latch

Logic Circuit

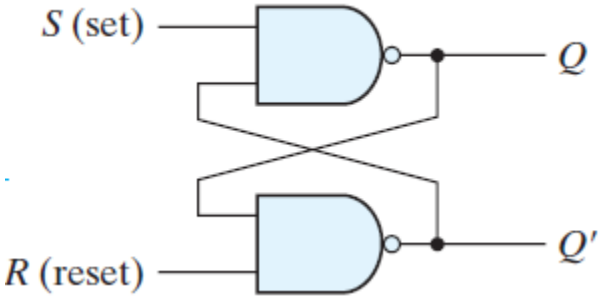




Function Table

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	(forbidden)

SR Latch (NAND Gate)

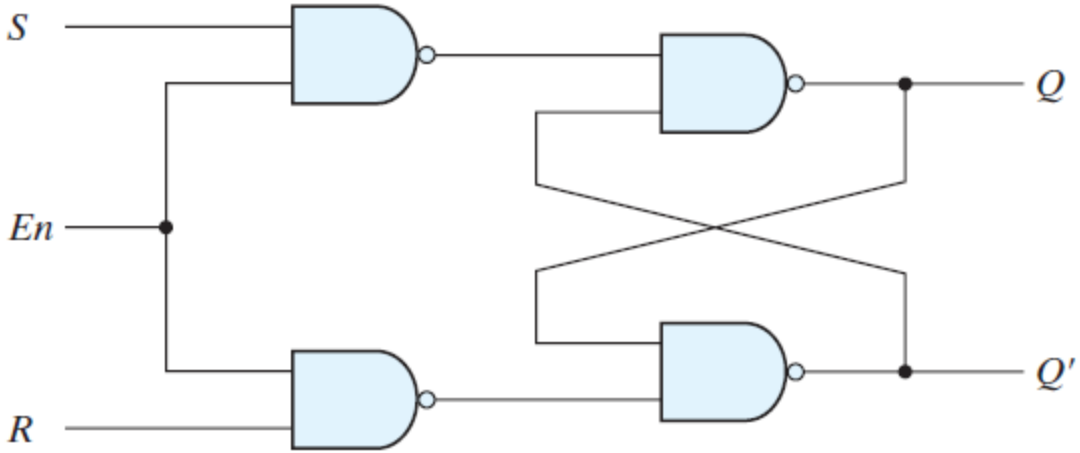


Logic Circuit

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	(forbidden)

Function Table

SR Latch with Control Input

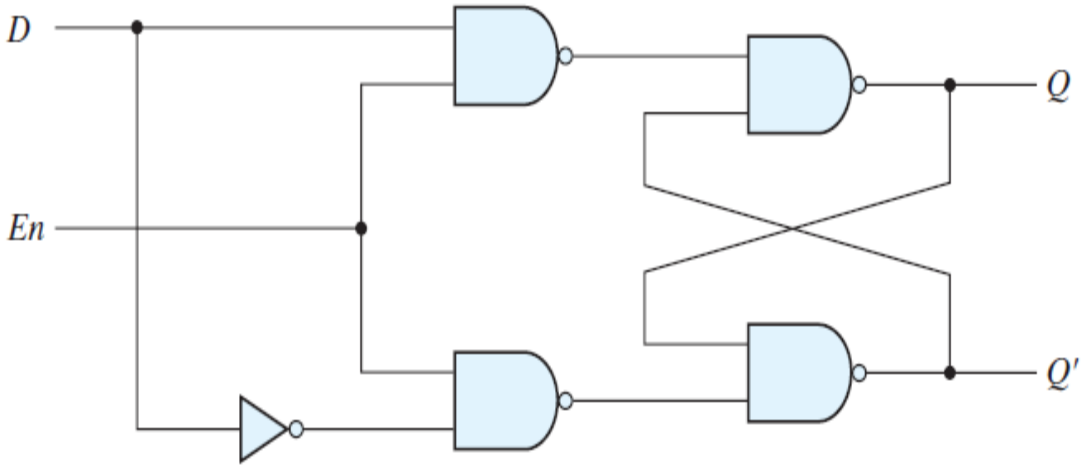


Logic Circuit

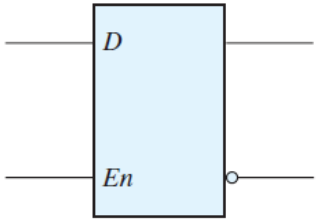
En	*S*	*R*	Next state of *Q*
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

Function Table

D Latch



Logic Circuit



En	*D*	Next state of *Q*
0	X	No change
1	0	$Q = 0$; reset state
1	1	$Q = 1$; set state

Function Table

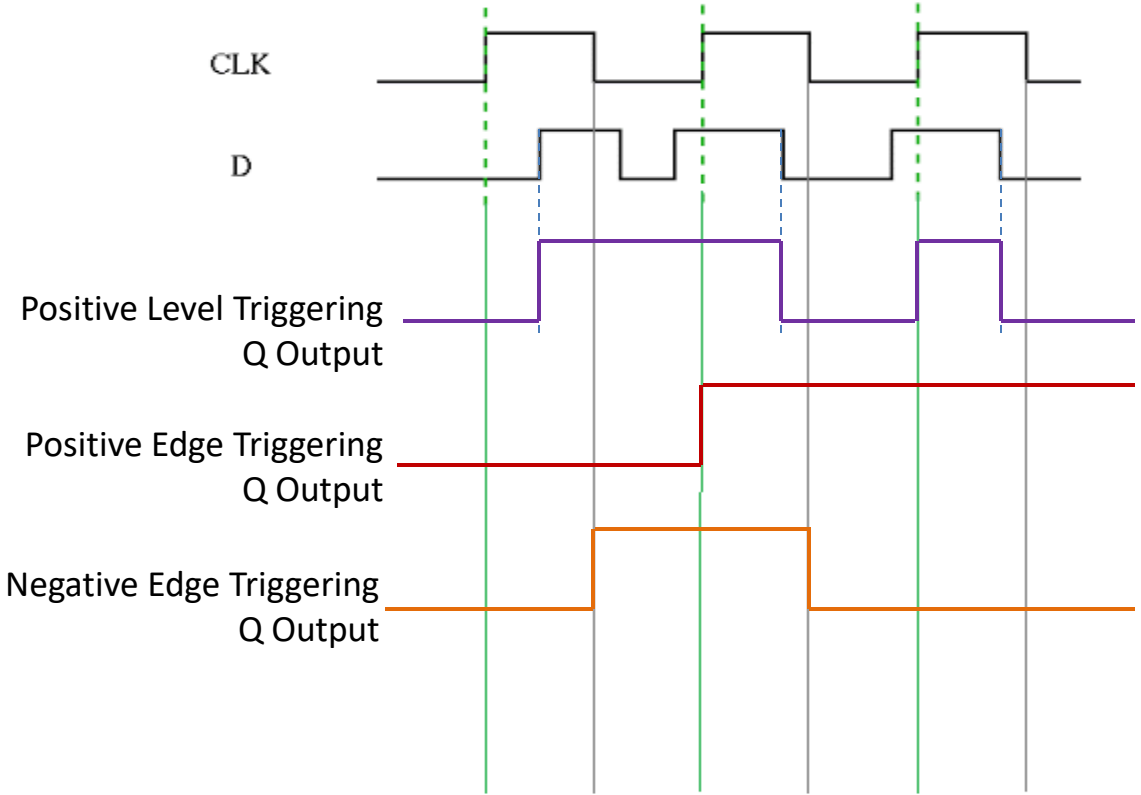
Clock Response

(a) Response to positive level

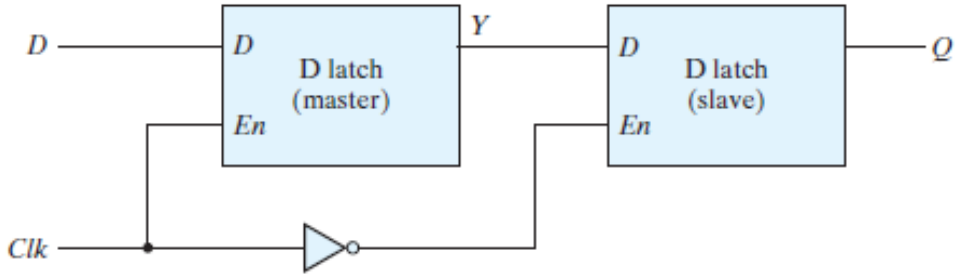
(b) Positive-edge response

(c) Negative-edge response

Triggering of Flip-flops

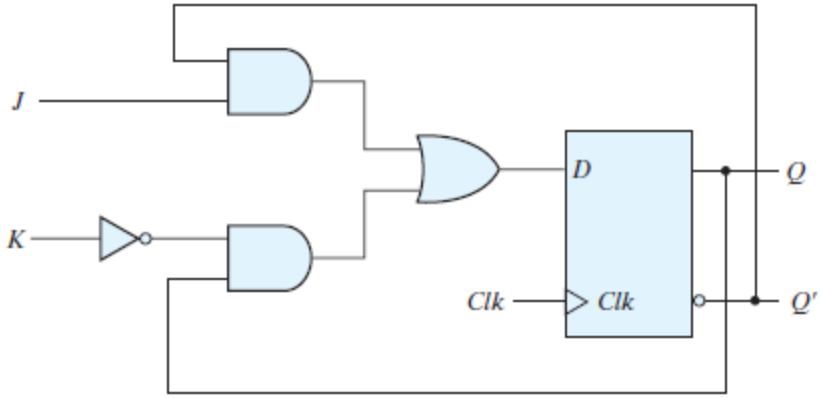


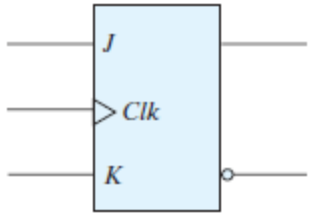
Edge Triggered D Flip-Flop

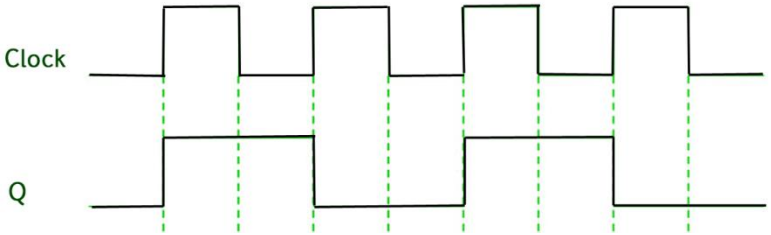


(a) Positive-edge (a) Negative-edge

J-K Flip flop





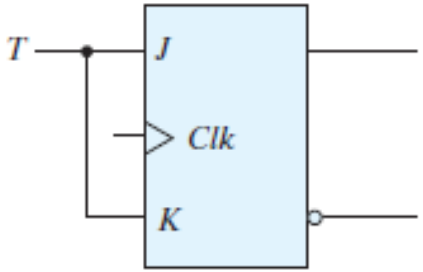


Flip-Flop Characteristic Tables

JK Flip-Flop

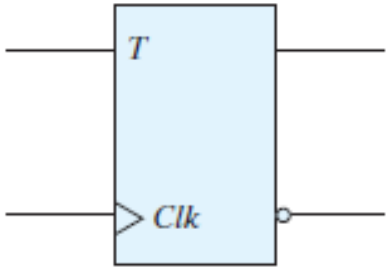
J	K	Q(t + 1)	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

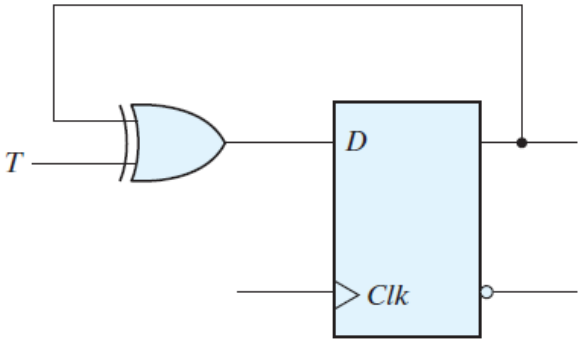
T Flip flop



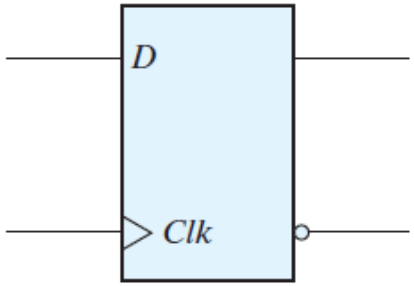
T Flip-Flop

T	Q(t + 1)	
0	$Q(t)$	No change
1	$Q'(t)$	Complement





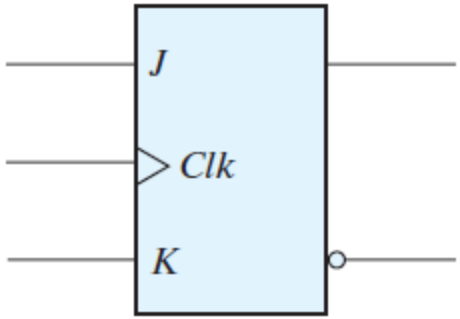
Flip-flops - Summary



D Flip-Flop

D	Q(t + 1)	
0	0	Reset
1	1	Set

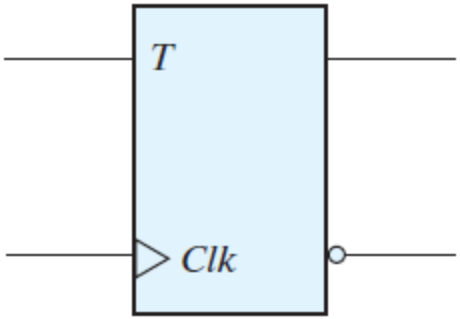
$$Q(t+1) = D$$



JK Flip-Flop

J	K	Q(t + 1)	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

$$Q(t+1) = JQ' + K'Q$$



T Flip-Flop

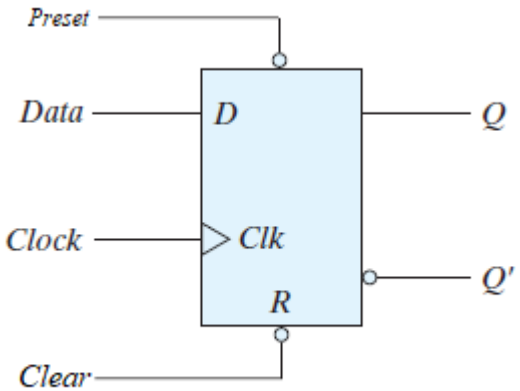
T	Q(t + 1)	
0	$Q(t)$	No change
1	$Q'(t)$	Complement

$$Q(t+1) = T \oplus Q$$

$$= TQ' + T'Q$$

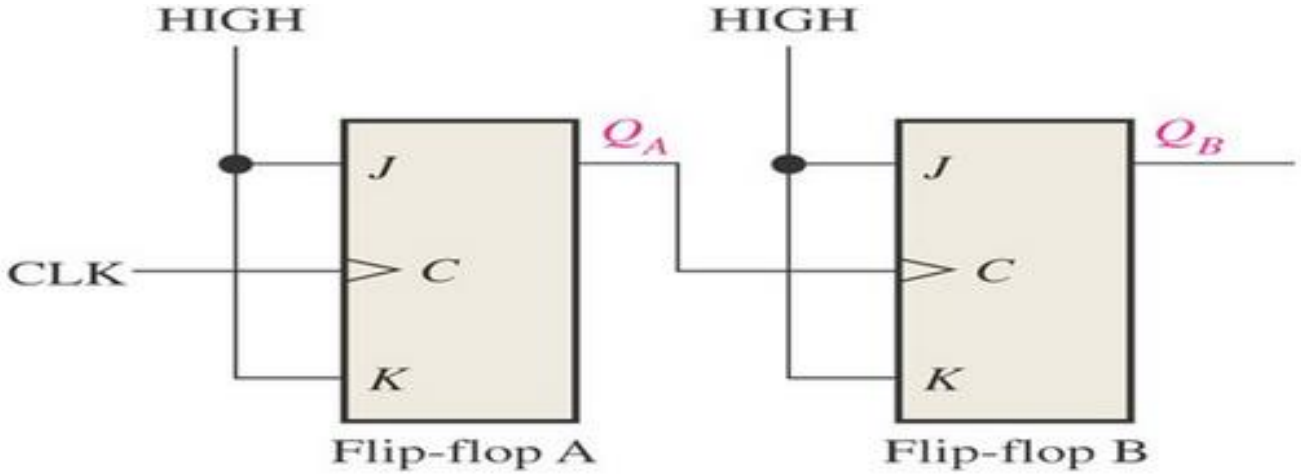
Counters

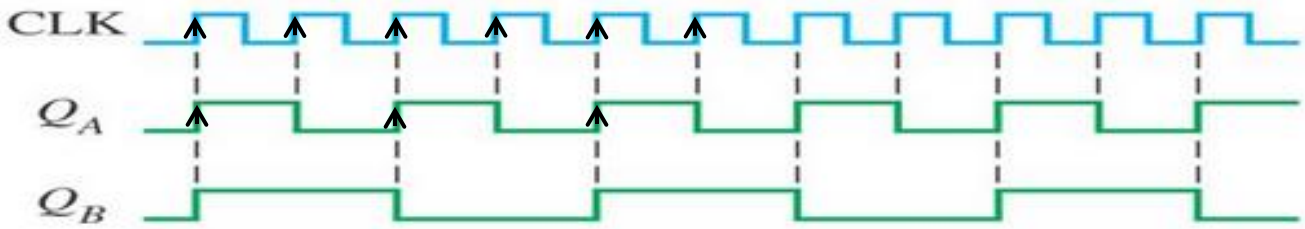
- Ripple Counter
- Synchronous Counter



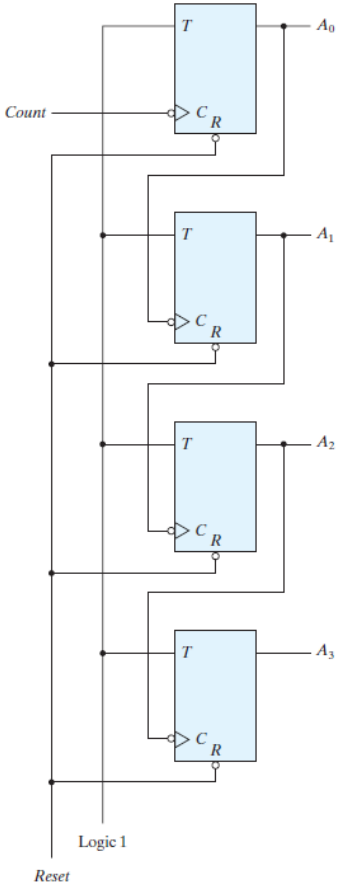
The input that sets the flip-flop to 1 is called ***preset*** or *direct set* .
The input that clears the flip-flop to 0 is called ***clear*** or *direct* ***reset*** .

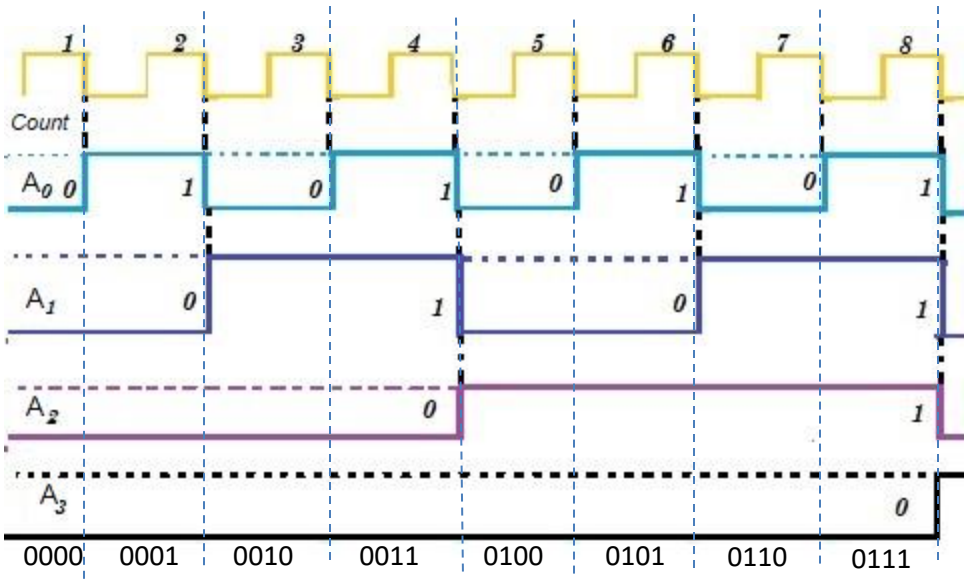
Frequency Divider





4 bit Binary Ripple Counter





CK	A_3	A_2	A_1	A_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

$\mathbf{0}$ *to* $(\mathbf{2^n - 1})$ *count using n flip flops* $-$ Q *output*

$(\mathbf{2^n - 1})$ *to* $\mathbf{0}$ *count using n flipflops* $-$ $\bar{Q}$ *output*