2/5/2021	Digital Logic And Design Digital Assignment -1	Name: Neha Ann Shygen Reg. No: 20BAI1230

1. Let F denote the pressure in fuel tank, O denote the pressure in Oxidizer tank and T denote the time.

F=1 ⇒ pressure in fuel tank is above the required minimum

O=1 ⇒ pressure in oxidizer tank is above the required minimum

T=1 ⇒ Time left for the satellite to lift off is more than 10 minutes

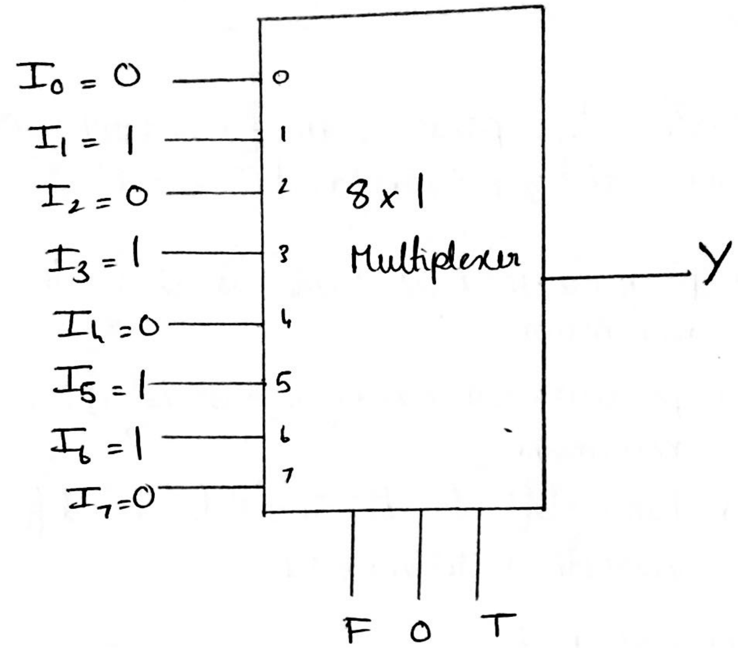
Conditions, Y=1 if:

1) F=1 and O=1 and T=0
2) F=0 and T=1
3) O=0 and T=1

Truth table:

F	O	T	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Therefore the 8×1 multiplexer is:



2. 8 x 3 priority encoder

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	x	y	z	V
0	0	0	0	0	0	0	0	X	X	X	0
1	0	0	0	0	0	0	0	0	0	0	1
X	1	0	0	0	0	0	0	0	0	1	1
X	X	1	0	0	0	0	0	0	1	0	1
X	X	X	1	0	0	0	0	0	1	1	1
X	X	X	X	1	0	0	0	1	0	0	1
X	X	X	X	X	1	0	0	1	0	1	1
X	X	X	X	X	X	1	0	1	1	0	1
X	X	X	X	X	X	X	1	1	1	1	1

From this truth table, the Boolean expression for the outputs x, y and z are:

$$z = \Sigma(1,3,5,7)$$
$$= \bar{D}_7\bar{D}_6\bar{D}_5\bar{D}_4\bar{D}_3\bar{D}_2D_1 + \bar{D}_7\bar{D}_6\bar{D}_5\bar{D}_4D_3 + \bar{D}_7\bar{D}_6D_5 + D_7$$

$$= D_7 + \bar{D}_6D_5 + \bar{D}_6\bar{D}_5\bar{D}_4D_3 + \bar{D}_6\bar{D}_5\bar{D}_4\bar{D}_3\bar{D}_2D_1$$
$$= D_7 + \bar{D}_6\left(D_5 + \bar{D}_5\bar{D}_4D_3 + \bar{D}_5\bar{D}_4\bar{D}_3\bar{D}_2D_1\right)$$
$$= D_7 + \bar{D}_6\left(D_5 + \bar{D}_4\left(D_3 + \bar{D}_2\bar{D}_3D_1\right)\right)$$
$$= D_7 + \bar{D}_6\left[D_5 + \bar{D}_4\left(D_3 + \bar{D}_2D_1\right)\right]$$

$$y = \Sigma(2,3,6,7)$$
$$= \bar{D}_7\bar{D}_6\bar{D}_5\bar{D}_4\bar{D}_3D_2 + \bar{D}_7\bar{D}_6\bar{D}_5\bar{D}_4D_3 + \bar{D}_7D_6 + D_7$$
$$= \bar{D}_5\bar{D}_4D_2 + \bar{D}_5\bar{D}_4D_3 + D_6 + D_7$$
$$= \bar{D}_5\bar{D}_4\left(D_2 + D_3\right) + D_6 + D_7$$

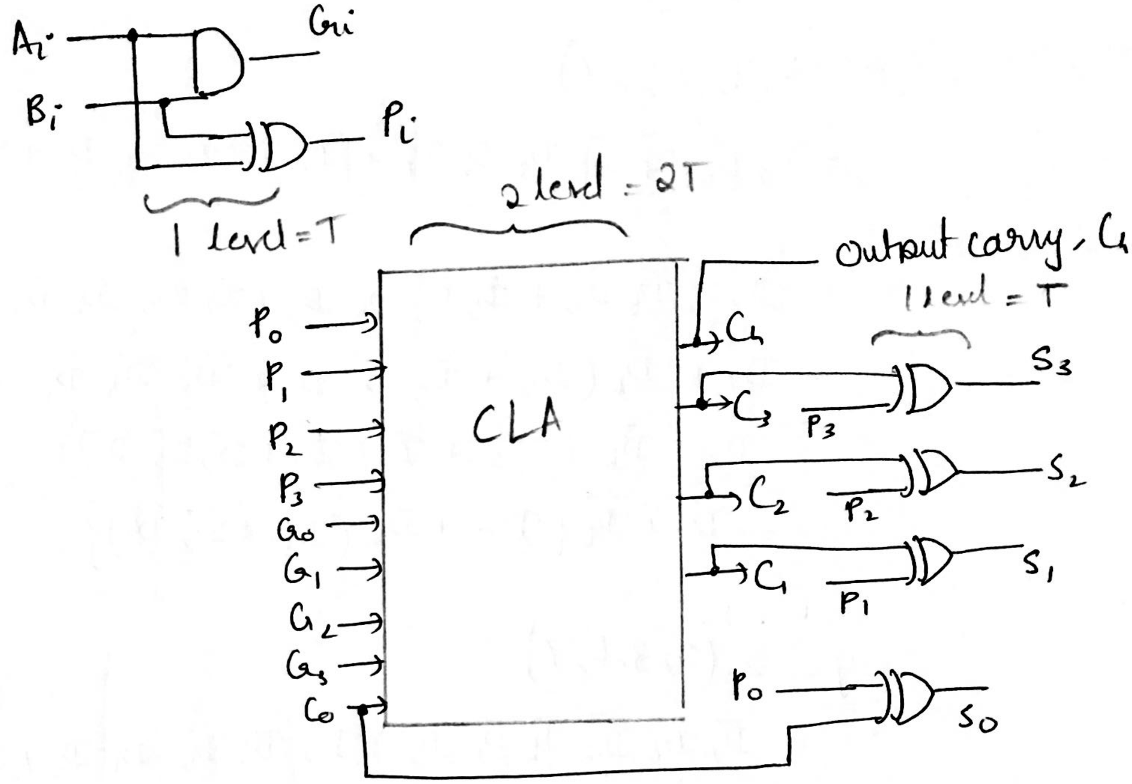
$$x = \Sigma(4,5,6,7)$$
$$= \bar{D}_7\bar{D}_6\bar{D}_5D_4 + \bar{D}_7\bar{D}_6D_5 + \bar{D}_7D_6 + D_7$$
$$= D_4 + D_5 + D_6 + D_7$$

3. For a single bit carry look ahead adder, the total propagation delay is given by 4T.

Here we are cascading 16, 4-bit carry look ahead module. Therefore the total propagation delay,

Total delay $= 16 \times 4T = 64T$

In a carry Look ahead adder, (4-bit)

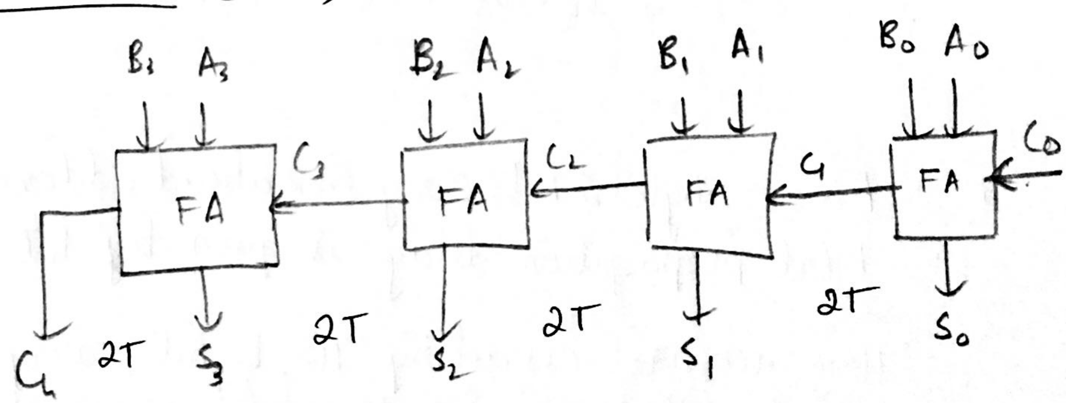


∴ Total delay = T + 2T + T = 4T for a 4-bit Carry Look Ahead Adder.

∴ Total delay of 64 bit adder = 64T

In case of a parallel adder,

Parallel adder (4-bit)



Here, total delay = 8T

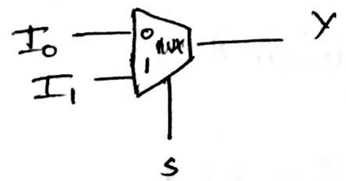
∴ For a 64-bit parallel adder,

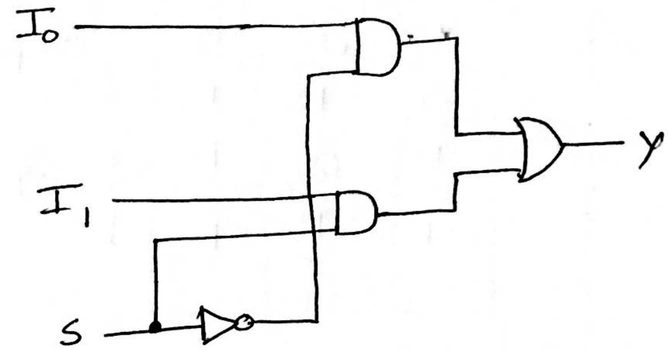
Total delay = 64 × 2T = 128T

The total delay for a 64 bit carry look ahead adder is 64T whereas that of a parallel adder is 128T which is twice of the initial. Therefore it is always better to go ahead with the carry look ahead adder as the total delay is low and thus we get the final output faster and accurately.

4.

2x1 Multiplexer





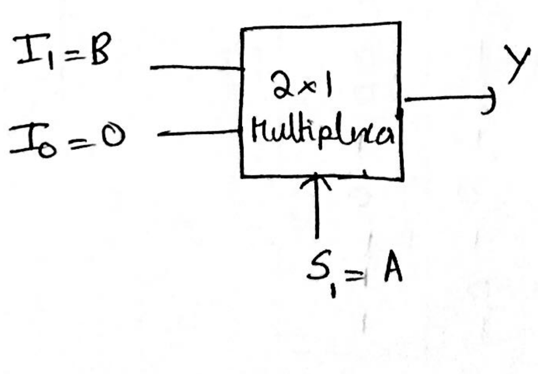
Truth table:

S	Y
0	I_0
1	I_1

a) Implementing an AND gate using a 2x1 multiplexer

Truth table:

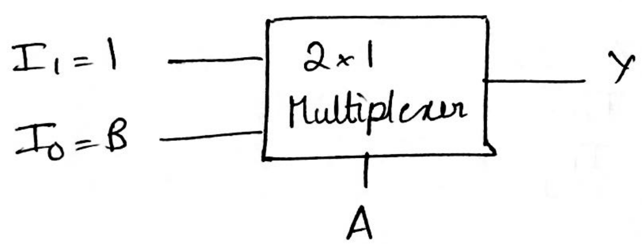
A	B	Y	
0	0	0	} Output = 0 when A = 0
0	1	0	
1	0	0	} Output = B when A = 1
1	1	1	



b) Implementing an OR gate using a 2×1 multiplexer.

Truth table:

A	B	Y	
0	0	0	} output = B when A = 0
0	1	1	
1	0	1	} output = 1 when A = 1
1	1	1	

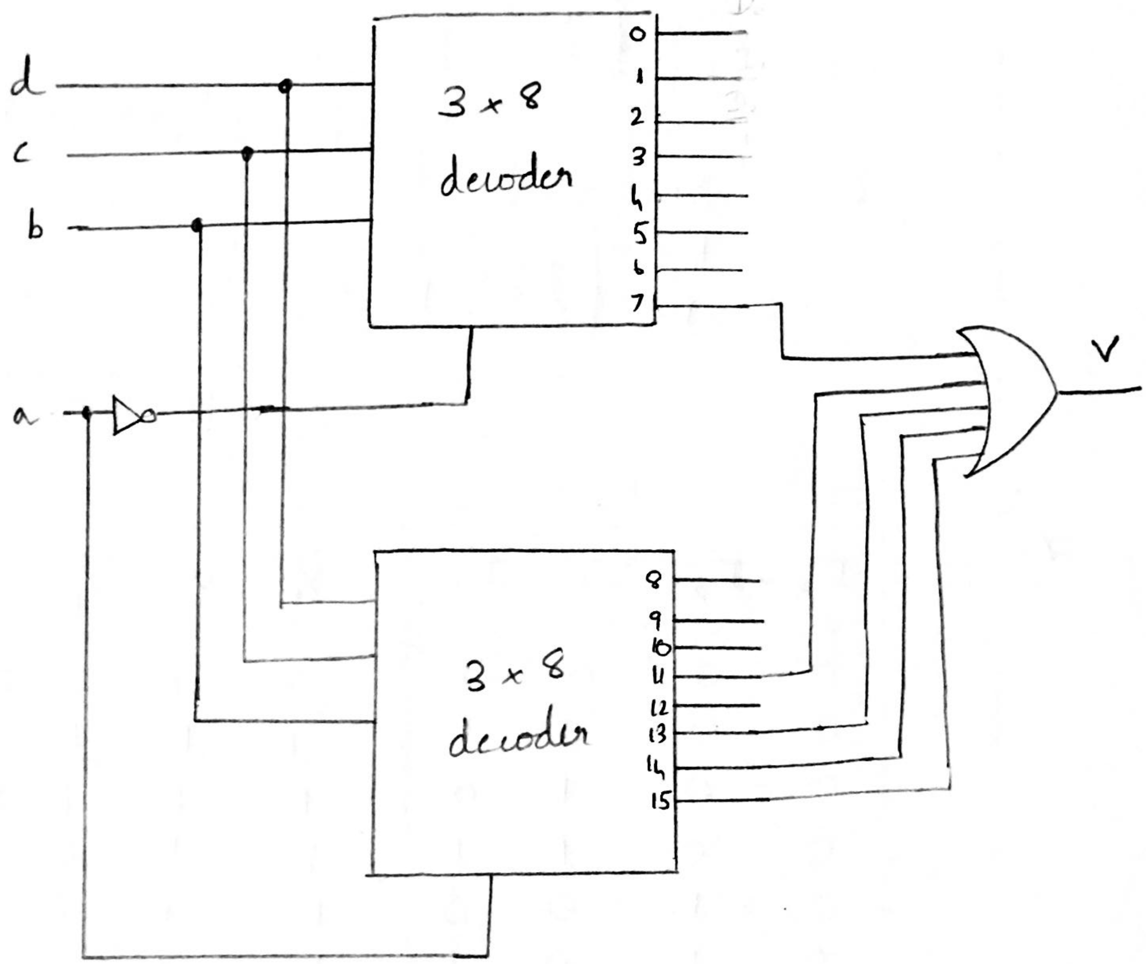


5. Inputs : a, b, c, d
Output : v

a	b	c	d	v
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

$v(a,b,c,d) = \Sigma(7, 11, 13, 14, 15)$

To implement v using a 3x8 Decoder:

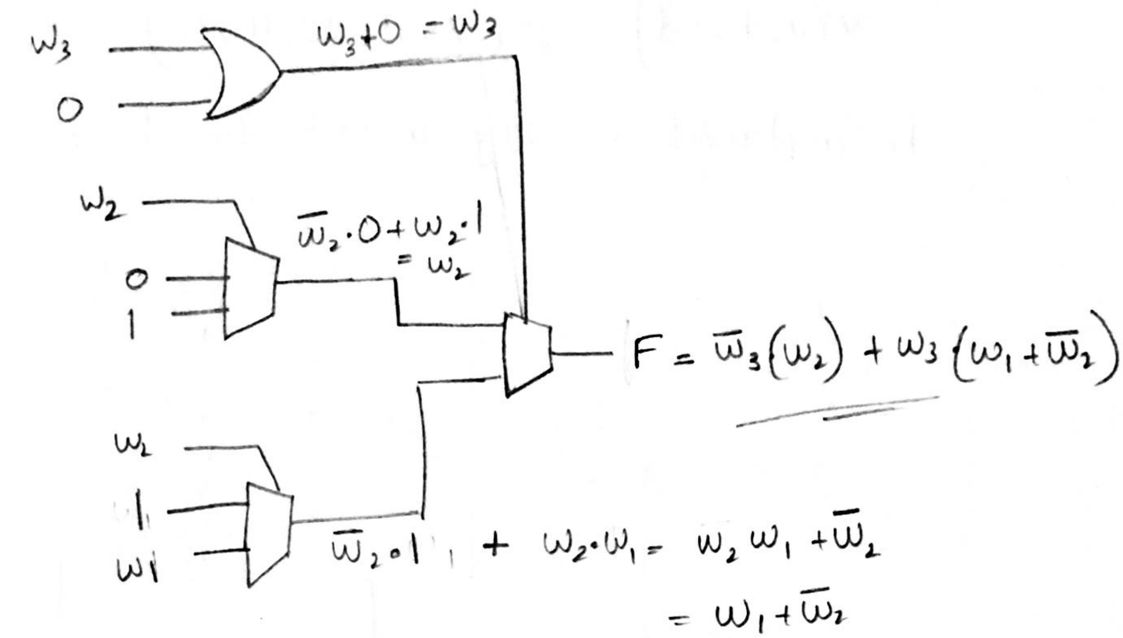


6. For a 2x1 multiplexer

The final expression $Y = \bar{S} I_0 + S I_1$

Here, $F = W_2 W_3' + W_1 W_3 + W_2' W_3$

$= W_3(W_1 + W_2') + W_2 W_3'$



7.

I_3	I_2	I_1	I_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	0
0	0	1	1	1	1	0	1
0	1	0	0	1	1	0	0
0	1	0	1	1	0	1	1
0	1	1	0	1	0	1	0
0	1	1	1	1	0	0	1
1	0	0	0	1	0	0	0
1	0	0	1	0	1	1	1
1	0	1	0	0	1	1	0
1	0	1	1	0	1	0	1
1	1	0	0	0	1	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	0	1	0
1	1	1	1	0	0	0	1

$I_3I_2 \backslash I_1I_0$	00	01	11	10
00		1	1	1
01	1	1	1	1
11				
10	1			

$$Y_3 = I_3'I_2 + I_3'I_0 + I_3'I_1 + I_3I_2'I_1'I_0'$$
$$= I_3'(I_2 + I_0 + I_1) + I_3I_2'I_1'I_0'$$
$$= \underline{I_3 \oplus (I_2 + I_1 + I_0)}$$

$I_3I_2 \backslash I_1I_0$	00	01	11	10
00		1	1	1
01	1			
11	1			
10		1	1	1

$$Y_2 = I_2'I_0 + I_2'I_1 + I_2I_1'I_0'$$
$$= I_2'(I_0 + I_1) + I_2I_1'I_0'$$
$$= \underline{I_2 \oplus (I_1 + I_0)}$$

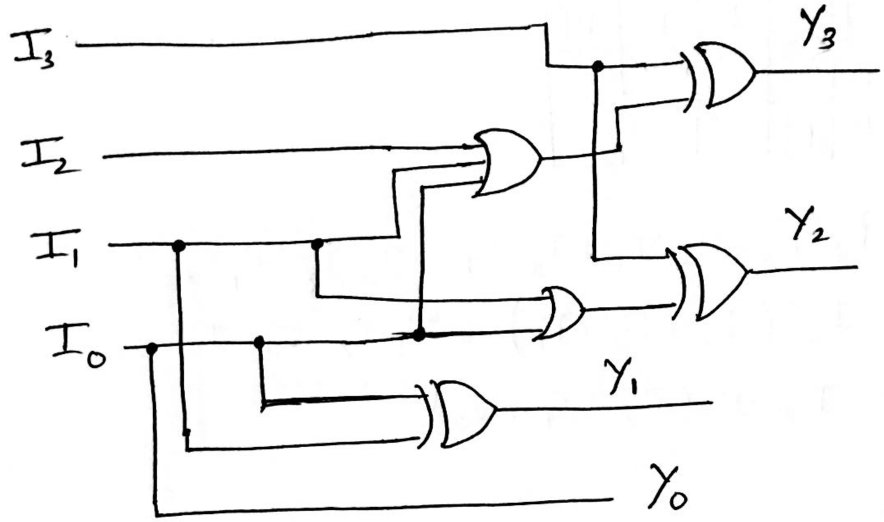
$I_3I_2 \backslash I_1I_0$	00	01	11	10
00		1		1
01		1		1
11		1		1
10		1		1

$$Y_1 = I_1'I_0 + I_1I_0'$$
$$= \underline{I_1 \oplus I_0}$$

$I_3I_2 \backslash I_1I_0$	00	01	11	10
00		1	1	
01		1	1	
11		1	1	
10		1	1	

$$\underline{Y_0 = I_0}$$

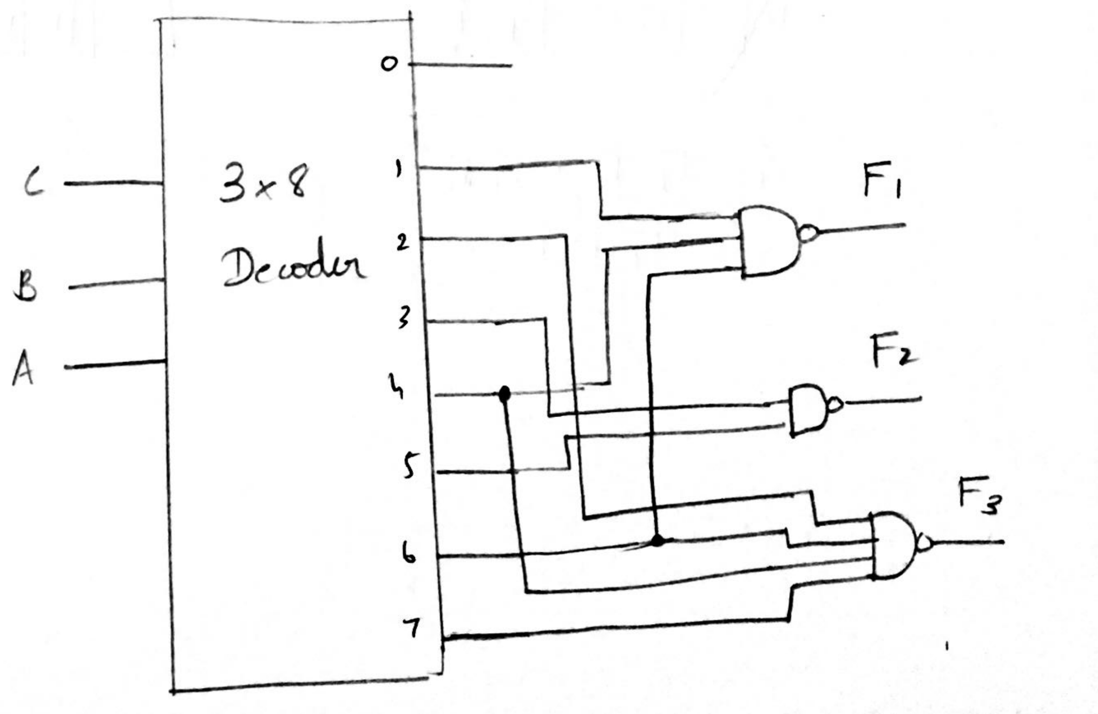
Circuit Diagram:



For a five bit 2's complement, the outputs are:

$$Y_4 = I_4 \oplus (I_3 + I_2 + I_1 + I_0)$$
$$Y_3 = I_3 \oplus (I_2 + I_1 + I_0)$$
$$Y_2 = I_2 \oplus (I_1 + I_0)$$
$$Y_1 = I_2 \oplus I_1$$
$$Y_0 = I_0$$

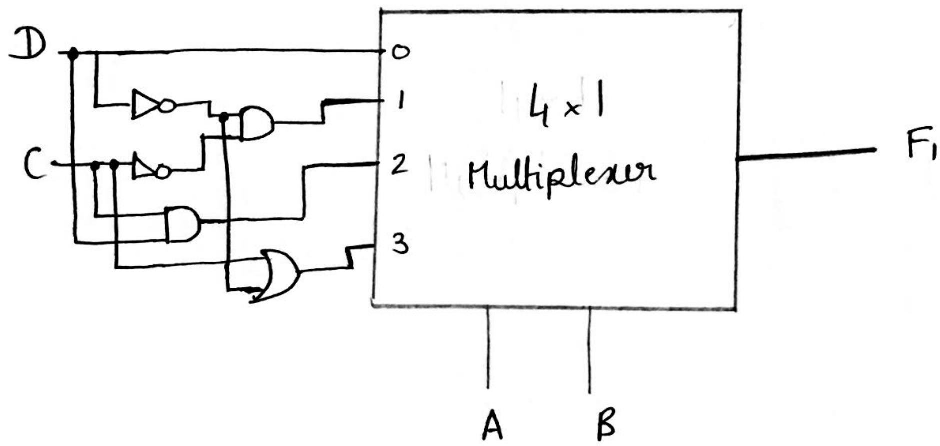
8.



9. $F_1(A, B, C, D) = \Sigma(1, 3, 4, 11, 12, 14, 15)$

AB \ CD	00	01	11	10
00		1	1	
01	1			
11	1		1	1
10			1	

A	B	
0	0	$I_0 = D$
0	1	$I_1 = \bar{C}\bar{D}$
1	0	$I_2 = CD$
1	1	$I_3 = C + \bar{D}$



10. 8x1 Multiplexer

$I_0 = D$

$I_1 = 0$

$I_2 = 0$

$I_3 = 1$

$I_4 = D$

$I_5 = 1$

$I_6 = D'$

$I_7 = 0$

A	B	C	D	F	
0	0	0	0	0	I_0
0	0	0	1	1	
0	0	1	0	0	I_1
0	0	1	1	0	
0	1	0	0	0	I_2
0	1	0	1	0	
0	1	1	0	1	I_3
0	1	1	1	1	
1	0	0	0	0	I_4
1	0	0	1	1	
1	0	1	0	1	I_5
1	0	1	1	1	
1	1	0	0	1	I_6
1	1	0	1	0	
1	1	1	0	0	I_7
1	1	1	1	0	

$\therefore F = \Sigma(1, 6, 7, 9, 10, 11, 12)$

AB \ CD	00	01	11	10
00	0	1	3	2
01	4	5	7: 1	6: 1
11	12: 1	13	15	14
10	8	9: 1	11: 1	10: 1

$\Rightarrow \quad F = \bar{A}BC + A\bar{B}C + \bar{B}\bar{C}D + AB\bar{C}\bar{D}$