Problem Statement

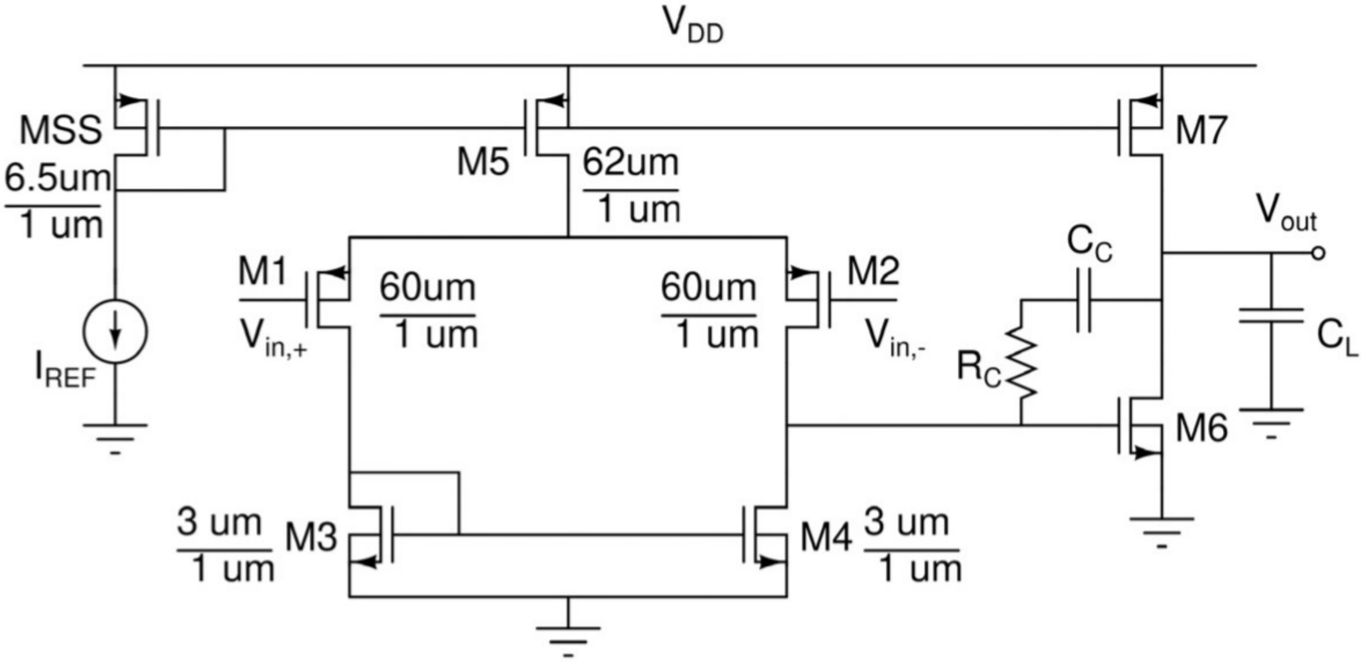


Figure 1:

In figure 1 a 2-stage Class A OTA is shown. Target specifications of the OTA is given in table 1.
Dimensions of transistors used in stage 1 is given in table 2.
Connect body of all PMOS transistors to their source terminals.
Connect the body of ALL NMOS transistors to GND.
Use PTM 130nm technology file

Table 1: Target Specifications

Slew Rate	>10 V/μs
Low frequency voltage gain, A_v	>75 dB
Unity Gain Frequency	>60 MHz
Phase Margin	>60 °
Power Dissipation	<750 μW

Design the 2^{nd} stage of the OTA to meet the target specifications (You can use your some other stage, Class B or Class AB, as well). Use PTM 130nm file. **Write the complete design procedure and report R_C, C_C and all transistor dimensions used in stage 2 (Driver Class A) of the OTA**.

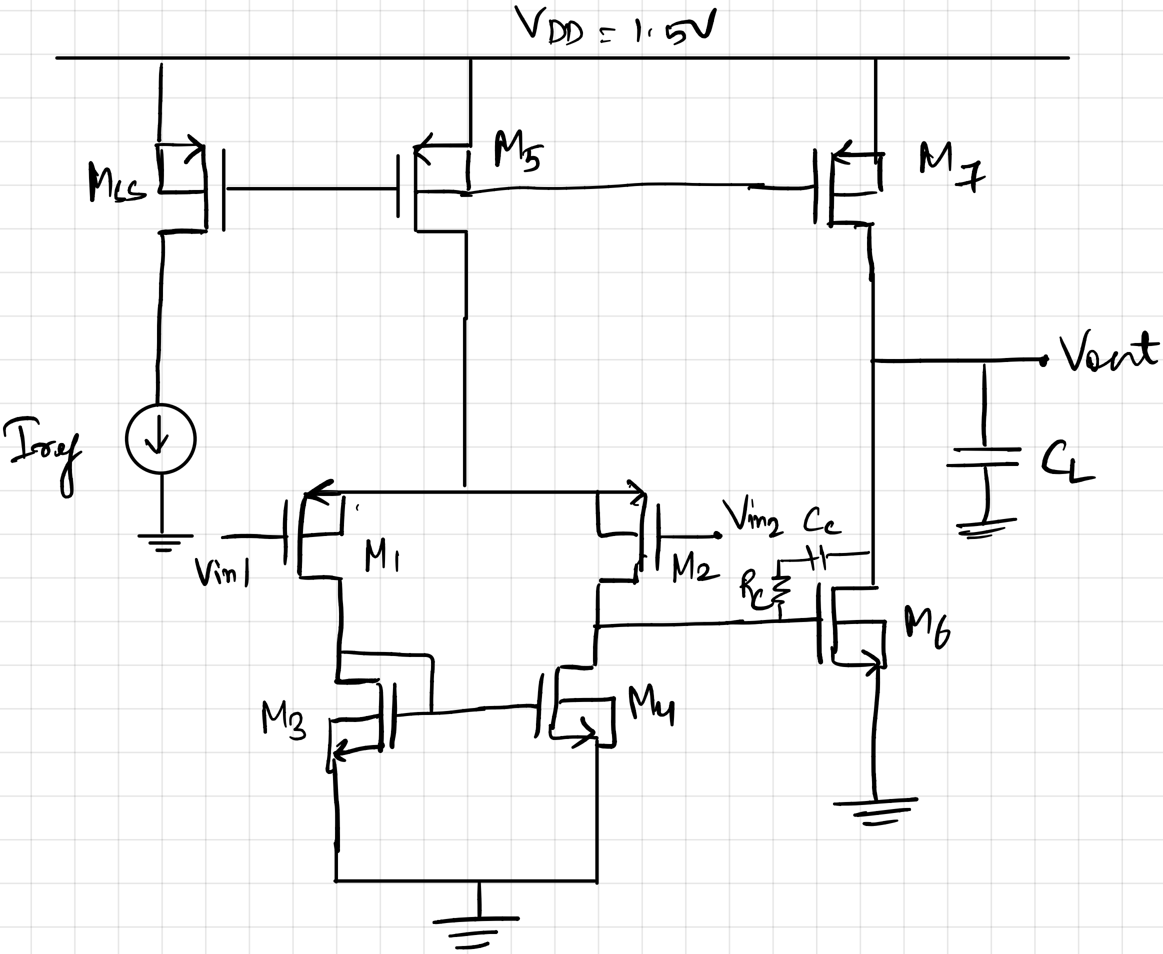
- Include X-circuit schematic and generate NGSPICE netlist.
- Perform the DC operating point analysis in NGSPICE for the $V_{IN,CM}$ and report I_{D6}, r_o and gm of all transistor dimensions used in stage 2 (Driver Class A) of the OTA.
- Plot (Bode) phase and magnitude with $V_{in}{}^{+} = V_{in,CM} + V_{AC}$, $V_{in}{}^{-} = V_{in,CM}$, $V_{AC} = 1$.

Table 2: Stage 1 Design Parameters

Parameter	Value
I_{REF}	10 μA
C_L	1 pF
V_{DD}	1.5 V
$V_{IN,CM}$	0.6 V
M1,M2	W/L = 60
M3,M4	W/L = 3
M5	W/L = 62
MSS	W/L = 6.5
L	1 um

Frequency Compensation

Given Circuit :



Design parameters :

$L = 1\mu m$, $I_{ref} = 10\mu A$, $C_L = 1pF$, $V_{DD} = 1.5V$,

$V_{incm} = 0.6V$

$M_1, M_2 : \frac{W}{L} = 60$

$M_3, M_4 : \frac{W}{L} = 3$

$M_5 : \frac{W}{L} = 62$

$M_{55} : \frac{W}{L} = 6.5$

Target Specifications:

1) Slew rate > 10 V/μs
2) $A_v > 75\,dB$
3) GBW > 60 MHz
4) PM > 60°
5) Power dissipation < 750 μW.

Since $I_{ref} = 10\mu A$

$$\therefore I_{D5} = I_{ref} \frac{(W/L)_5}{(W/L)_{ss}}$$

$$I_{D5} = 10 \times \frac{62}{6.5} = 95.38\mu A$$

$$I_{D5} \simeq 96\mu A$$

Also, $SR > 10V/\mu s$

Let Slew Rate = 20 V/μs.

$$\frac{I_{D5\,min}}{C_L} = 20V/\mu sec$$

$$I_{D5\,min} = 20\mu A.$$

$\because$ we have taken $I_{D5} = 96\mu A$ — satisfies this condition

$\Rightarrow$ Power dissipation $= I_{D1} \times V_{DD}$

$$I_D \times V_{DD} < 750\mu W$$

$$I_D = I_{D5} + I_{ref} + I_{D7}$$

$$\therefore (96 + 10 + I_{D7})\mu A \times 1.5 < 750\mu W$$

$$I_{D7} < 394\mu A$$

Let $I_{D7} = 300\,\mu A$

Now, $(300 + 10 + 96) \times 1.5\,V < 750\,\mu W$

$609\,\mu W < 750\,\mu W$.

$\therefore$ $I_{ref} = 10\,\mu A$, $I_{D5} = 96\,\mu A$, $I_{D7} = 300\,\mu A$

Let limiting gain frequency = 80 MHz

Now, we know $\dfrac{g_{m1}}{2\pi C_c} = 80\,MHz$

$$P_2 = \frac{g_{m6}}{2\pi C_L} \quad \& \quad Z = \frac{1}{\left(R_C - \frac{1}{g_{m6}}\right)\left(\frac{1}{g_{m6}}\right)}$$

Also DC gain $= \dfrac{g_{m1}\, g_{m6}}{g_B\, g_C}$

where $g_B = g_{ds2} + g_{ds4}$

and $g_C = g_{ds6} + g_{ds7}$

Now PM is given as

$$PM = 180^\circ + \left[-90^\circ - \tan^{-1}\left(\frac{UGBW}{P_2}\right)\right]$$

Let PM = 70°

$$70^\circ = 180^\circ - 90^\circ - \tan^{-1}\left[\frac{UGBW}{P_2}\right]$$

$$\frac{UGBW}{P_2} = \tan 20^\circ$$

$$P_2 = \frac{UGBW}{\tan 20^\circ}$$

$$P_2 = 219.84\,MHz$$

Now $$P_2 = \frac{g_{m6}}{2\pi C_L}$$

$$g_{m6} = 219.84 \times 10^6 \times 2\pi \times C_L$$

$$g_{m6} = 1.38\,mS$$

Now for $g_{m1} = \sqrt{2 I_{D1} \mu_p C_{ox} (W/L)}$,

$$g_{m1} = \sqrt{2 \times 48\mu \times 62.7\mu \times 60}$$

$$g_{m1} = 0.6\,mS$$

$\because$ we considered $UGBW = 80\,MHz$

$$\frac{g_{m1}}{2\pi C_c} = 80\,MHz$$

$$C_c = \frac{0.6 \times 10^{-3}}{2\pi \times 80 \times 10^6}$$

$$C_c = 1.19\,pF$$

Now $$R_c = \left(1 + \frac{1}{1.29}\right)(724.63)$$

$$R_c = 1333.5\,\Omega$$

Taking $\mu_n C_{ox} = 146.44\mu$.

$$g_{m6} = \sqrt{2 I_{D7} \mu_n C_{ox} (W/L)_6}$$

$$(W/L)_6 = \frac{g_{m6}^2}{2 I_{D7} \mu_n C_{ox}}$$

$$(W/L)_6 = \frac{(1.38)^2 \times 10^{-6}}{2 \times 300\mu \times 146.44\mu}$$

$$\left(W/L\right)_6 = 21.67.$$

For $(W/L)_7$, $\quad I_{D7} = \dfrac{I_{ref}\,(W/L)_7}{(W/L)_{M55}}$

$$\left(\frac{W}{L}\right)_7 = 195$$

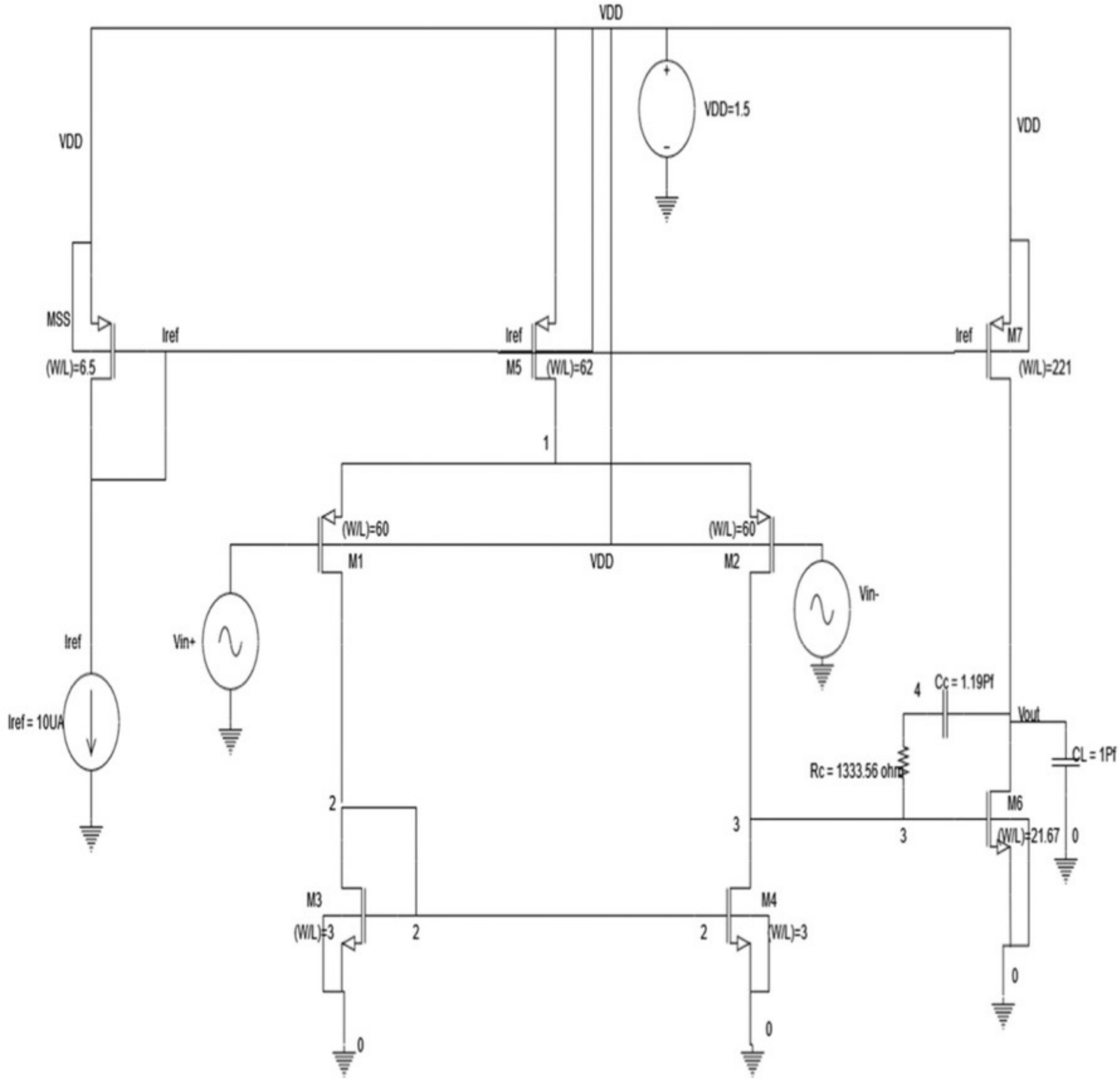
Now for 2nd iteration :

Let $I_{D7} = 340\mu A$

$$\therefore (W/L)_7 = 221$$

Include X-circuit schematic and generate NGSPICE netlist.

Below is the given schematic and netlisting to be used in order to obtain the output for the 2 stage OTA with the help of pmos and current mirror with reference current as 10 UA.



Here we are going to follow the terminology as MOS (DRAIN, GATE, SOURCE, BULK)

Where bulk must be connected to the ground in any case for the nmos and to the source for pmos.

M1 2 Vin1 1 1 PMOS

M2 3 Vin2 1 1 PMOS

M3 2 2 0 0 NMOS

M4 3 2 0 0 NMOS

M5 1 Iref vdd Vdd PMOS

M6 Vout 3 0 0 NMOS

M7 Vout Iref vdd Vdd PMOS

MSS Iref Iref vdd Vdd PMOS

Here, we can clearly see that Iref, Vout, Vdd, 1,2 ,3 ,4, 0 are the various nodes that are use as an intra connects between different mosfets, capacitor and resistor.

We can see the values of various mosfet's (W/L) are:

(W/L)1 = 60

(W/L)2 = 60

(W/L)3 = 3

(W/L)4 = 3

(W/L)5 = 62

(W/L)6 = 21.67

(W/L)7 = 221

(W/L) ss = 6.5

Perform the DC operating point analysis in NGSPICE for the VIN, CM and report ID6, ro and gm of all transistor dimensions used in stage 2 (Driver Class A) of the OTA.

For VinCM = 0.6 v

CODE SNIPPET:

```
2 stage OTA with current mirror dc parameters


*** netlisting can be given as
.include cmos_130nm.txt
M1 2 Vin1 1 1 PMOS          W= 60U L= 1U
M2 3 Vin2 1 1 PMOS          W= 60U L= 1U
M3 2 2 0 0 NMOS             W= 3U L= 1U
M4 3 2 0 0 NMOS             W= 3U L= 1U
M5 1 Iref vdd Vdd PMOS      W= 62U L= 1U
M6 Vout 3 0 0 NMOS          W= 21.67U L= 1U
M7 Vout Iref vdd Vdd PMOS   W= 221U L= 1U
MSS Iref Iref vdd Vdd PMOS  W= 6.5U L= 1U
*Capacitors
CL  Vout 0 1p
Cc  4  Vout   1.19p
*resistor
Rc  4 3 1333.56
*supply**
V1 vdd 0 1.5
* Iref required for constant current mirror*
I1 Iref  0 10U
** given value of Vcm to be used to calculate parameters**
VG1 Vin1 0 0.6
VG2 Vin2 0 0.6 |
.control
**** DC Operating Point******
op
print @M6[gm]
print @M7[gm]
print @M6[id]
print @M7[id]
print @M6[gds]
print @M7[gds]
print @M1[gm]
print @M2[gds]
print @M3[gm]
print @M4[gds]
print @M5[gm]
print @M2[gm]
let gd6 = @M6[gds]
let ro6 = '1/gd6'
print ro6
let gd7 = @M7[gds]
let r07 = '1/gd7'
print r07
let Av1 = @M1[gm]/(@M4[gds]+@M2[gds])
print Av1
let Av2 = @M6[gm]/(@M6[gds]+@M7[gds])
print Av2
.endc
.end
```

TERMINAL RESULTS:

ngspice 35

```
No. of Data Rows : 1
@m6[gm] = 1.533611e-03
@m7[gm] = 2.828515e-03
@m6[id] = 3.403974e-04
@m7[id] = 3.403974e-04
@m6[gds] = 9.079421e-06
@m7[gds] = 1.285854e-05
@m1[gm] = 5.149377e-04
@m2[gds] = 4.532084e-06
@m3[gm] = 2.120507e-04
@m4[gds] = 1.288382e-06
@m5[gm] = 7.786964e-04
@m2[gm] = 5.149377e-04
ro6 = 1.101392e+05
r07 = 7.776932e+04
av1 = 8.847019e+01
av2 = 6.990670e+01
ngspice 7 ->
```

twostage_ota_dc.cir -- ready -- Quit

Now, here we can observe that the values of various current Id, gm and gds required to calculate overall dc gain and the value of the resistances r0 are obtained are:

Id6= 3.403974e-04 Id7 = 3.403974e-04

gm6 = 1.533611e-03 gm1 = 5.149377e-04

gds6 = 9.079421e-06 gds7 = 1.285854e-05

gds2 = 4.532084e-06 gds4 = 1.288382e-06

since, ro = 1/gds therefore we get the values of

ro6 = 1.101392e+05 and

ro7 = 7.776932e+04

we got the value of gains of the two stages as Av1 = 8.847e+01 and Av2 = 6.990e+01

now the value of overall gain is Av = Av1*Av2 ➔ 88.47*70 ➔ 6192.9

which when converted into db we get Av (in db) = 20log (6192.9) ➔ 20*3.791 ➔ 75.837db

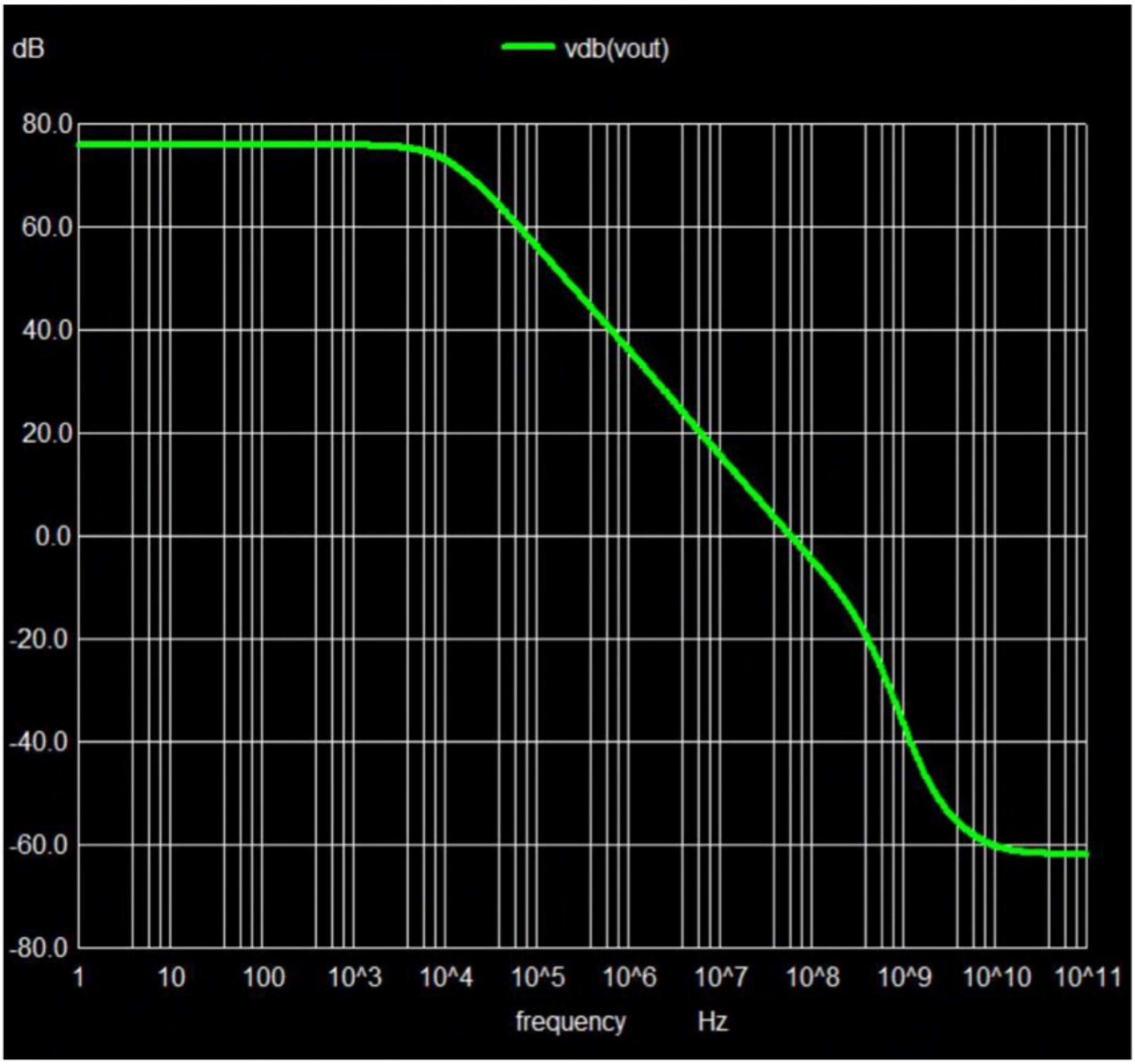
hence the requirement of dc gain to be 75db and above is attained while taking consideration of other parameters as well.

Plot (Bode) phase and magnitude with Vin + = VinCM + VAC, Vin − = VinCM, VAC = 1.

CODE SNIPPET:

```
2 stage OTA with current mirror ac parameters

*** netlisting can be given as

.include cmos_130nm.txt

M1 2 Vin1 1 1 PMOS          W= 60U L= 1U
M2 3 Vin2 1 1 PMOS          W= 60U L= 1U
M3 2 2 0 0 NMOS             W= 3U L= 1U
M4 3 2 0 0 NMOS             W= 3U L= 1U
M5 1 Iref vdd Vdd PMOS      W= 62U L= 1U
M6 Vout 3 0 0 NMOS          W= 21.67U L= 1U
M7 Vout Iref vdd Vdd PMOS   W= 221U L= 1U
MSS Iref Iref vdd Vdd PMOS W= 6.5U L= 1U

*Capacitors
CL  Vout 0 1p
Cc  4  Vout   1.19p

*resistor
Rc  4 3 1333.56

*supply**
V1 vdd 0 1.5

* Iref required for constant current mirror*
I1 Iref  0 10U

** given value of Vcm to be used to calculate parameters**
VG1 Vin1 0 0.6 ac 1
VG2 Vin2 0 0.6
.control
op
set xbrushwidth = 4
ac dec 100 1 100G
plot vdb(Vout)
plot 180/pi*phase(Vout)-180

.endc
.end
```

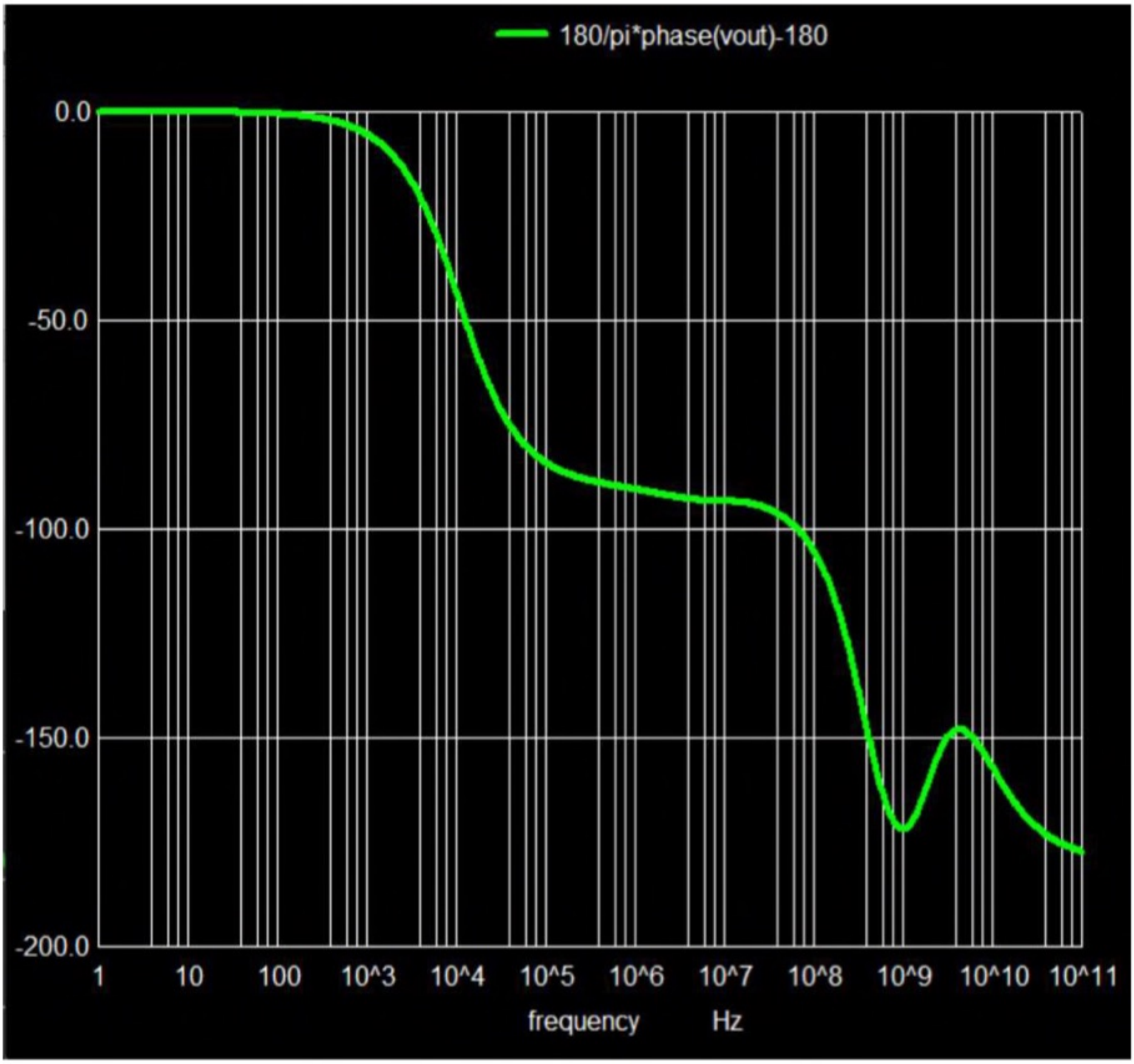
MAGNITUDE PLOT:



Here in this magnitude plot we can clearly see that at the lower frequency the overall gain in db is above 75db and further starts to decrease gradually as we keep on increasing the value of frequency which was expected.

We can also observe one particular thing that is that there a sort of peak at between 10^8 and 10^9 which actually shows that the zero is added there in order to compensate the effect of the pole2 but since the values of pole and zero's location cannot be matched perfectly, we are getting a peak first but gets compensated afterwards as the pole gets into the action and thus maintains a straight-line characteristic.

PHASE PLOT:



The same effect as seen in the magnitude plot can again be seen in the phase plot as well.