

# Project Report

## Design of OTA with class-B Slew-Rate Boosting for fast high-performance switched capacitor

By Neha Koundal (213070061)

### Target Specifications of the OTA:

Parameters	Specifications	
Static Power Consumption	Bias circuit + Pseudo class AB Amplifier	<4.5 mW
	Bias circuit + Pseudo class AB Amplifier with SR boosting	<5.25 mW
Input DC common mode voltage		0.75V
DC Voltage Gain		>70 dB
Small signal GBW, Gain Bandwidth Product, (UGF) of voltage gain		>1GHz
Open Loop Phase Margin		>60°
Load Capacitance		0.5pF
Slew Rate	Pseudo class AB Amplifier	>400 V/ $\mu$ S
	Pseudo class AB Amplifier with SR boosting	>900 V/ $\mu$ S
Input referred Noise ( $V_{in,n}$ (rms)) (1Hz to 250 MHz)		<200 nV <sub>rms</sub>
Maximum fully differential Output swing		±1.3V
1% settling time	Pseudo class AB Amplifier	<4ns
	Pseudo class AB Amplifier with SR boosting	<3ns
CMRR for input offset = 20mV		>100 dB

#### 1. Pseudo class AB design

- Report the design flow of the OTA in the form of step-by-step procedure. Design flow involves determining bias currents, voltages, and size of transistors to meet target specifications.
- The design procedure may not achieve the target specs in a single iteration. Hence, show successive iterations of design flow that finally achieve the target specs.
- Clearly show bias currents and voltages on the schematic.
- Write size of transistors in a table. (Keep names of transistors same as reference paper)

#### 2. Auxiliary circuit design (refer to the reference paper)

- Report the design flow of the auxiliary circuit in the form of step-by-step procedure.
- Show successive iterations, if any (as explained in 1.2 above).
- Clearly show bias currents and voltages on the schematic.
- Write size of transistors in a table. (Keep names of transistors same as reference paper)

### **3. Current Reference Generator Circuit Design**

In this section of the project, you will design a reference generator circuit of your choice. Reference generator circuits include reference current source ( $I_{ref}$ ) of your choice and current mirrors that use  $I_{ref}$  to generate bias voltages.

1. Draw the Reference current source for ( $I_{ref} = 50 \mu A$ ), and current mirrors that you use to generate bias voltages for main class AB amplifier as well as auxiliary circuit.
2. Report the step-by-step design procedure for reference generator circuits.
3. Tabulate the size of transistors used in the circuit.

### **4. DC Operating point simulations**

- Apply DC common mode voltage (VCM) to the input terminals of the OTA.
- Run DC simulations on the OTA and the Auxiliary circuit including reference generator and find DC operating points.
- DC operating points should clearly show all the node voltages and currents though each transistor.

### **5. AC simulations**

1. *For pseudo class AB amplifier:*
  - Plot the open loop fully differential voltage gain (in dB) and phase (in degrees) as a function of frequency (Bode plot). (Use common mode DC voltage: 0.75 V, AC signal for  $V_{in^+} = 1$  and  $V_{in^-} = 0$ ).
  - Highlight clearly GBW, Gain cross over frequency and phase cross over frequency.
  - Report Phase margin, small signal GBW and Open loop gain in dB.
2. *For pseudo class AB amplifier with auxiliary class B booster circuit:*
  - Plot the open loop fully differential voltage gain (in dB) and phase (in degrees) as a function of frequency (Bode plot). (Use common mode DC voltage: 0.75 V, AC signal for  $V_{in^+} = 1$  and  $V_{in^-} = 0$ )
  - Highlight clearly GBW, Gain cross over frequency and phase cross over frequency
  - Report Phase margin, small signal GBW and Open loop gain in dB.

## 6. Settling Time & Slew rate calculation

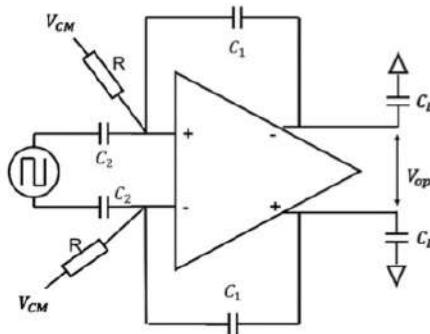


Figure 1: Settling Time setup

1. Connect the OTA as shown in fig. 1 with gain -1 and plot the fully differential output voltage. Choose appropriate value of  $C_1$  and  $C_2$  and  $R$ . consider  $V_{CM} = 0.75V$ . ( To avoid loading effect,  $C_1$  and  $C_2$  should be less than  $0.1 * C_L$ .)

- Square wave specification:
  - $T_{rise} = T_{fall} = 1 \text{ ps}$
  - $V_{pp} = 0.5V$
  - $T_{on} = 100 \text{ ns}$
  - $T_{period} = 200 \text{ ns}$

2. Plot  $V_{op}$  for

- Pseudo class AB amplifier only
- Pseudo class AB amplifier with auxiliary class B booster circuit

3. Calculate Slew rate by calculating time required for  $V_{out}$  to reach from 0V to 0.3V & 0.5V to 0.2V [4 Marks]

- $SR^+ = \frac{0.3V}{\text{time required for } V_{out} \text{ to reach from } 0V \text{ to } 0.3V}$
- $SR^- = \frac{0.3V}{\text{time required for } V_{out} \text{ to reach from } 0.5V \text{ to } 0.2V}$

4. Report average SR for

- Pseudo class AB amplifier only
- Pseudo class AB amplifier with auxiliary class B booster circuit
- $SR_{\text{average}} = \frac{SR^+ + SR^-}{2}$

5. Report 1% settling time for

- Pseudo class AB amplifier only
- Pseudo class AB amplifier with auxiliary class B booster circuit

## Pseudo class AB design

### Design Flow:

**Step 1 :** Given static power consumption:

Bias circuit + pseudo class AB  $< 4.5 \text{ mW}$

and static power  $\Rightarrow I_{\text{total}} \times V_{\text{dd}} < 4.5 \text{ mW}$

$$\therefore I_{\text{total}} \times 1.5 < 4.5 \text{ mW}$$

$$I_{\text{total}} < 3 \text{ mA}$$

Hence, total current consumed by pseudo AB circuit and bias circuit  $< 3 \text{ mA}$ .

**Step 2 :** As the current limit is defined, we will consider the currents mentioned in the paper.

i.e  $I_{B1} = 1.5 \text{ mA}$  : To main telescopic amplifier

$I_{B2} = 0.4 \text{ mA}$  : To second stage

$I_{B3} = 0.25 \text{ mA}$  : To CMFB

and remaining current will be for bias circuit.

Step 3: Given fully differential output swing =  $\pm 1.3V$

$$\therefore \text{differential o/p swing for single ended} = \frac{1.3}{2} = 0.65V$$

$$\therefore \text{o/p swing} = 0.65 \text{ volts}$$

Output swing for design of telescopic amplifier gets reduced to  $\frac{0.65}{10} = 0.065 \text{ volts}$

$\Rightarrow$  considering o/p swing for telescopic as  $0.1V$ . which means we have  $1400mV$  left with us to assign the  $V_{DSAT}$  for the MOSFETs that are being used in the telescopic amplifier.

$$V_{DSAT} \text{ Budget} = 1400mV$$

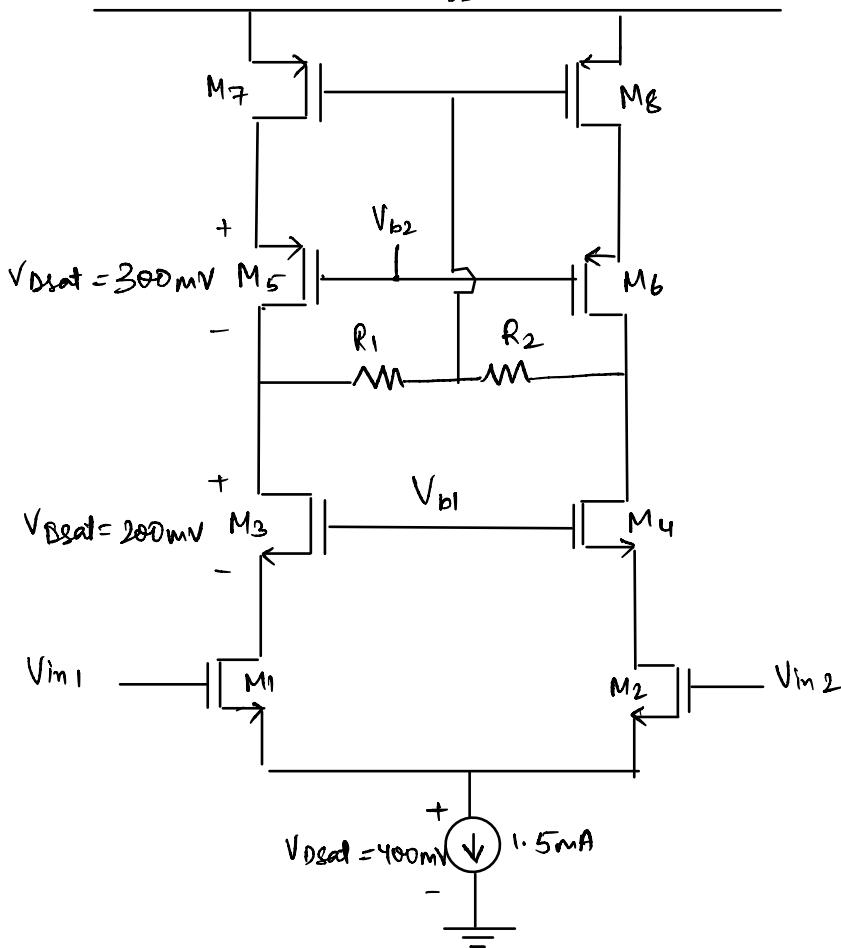
Step 4: Now for distributing the  $V_{DSAT}$  for the MOSFETs

$$M_1, M_3 = 200mV$$

$$M_5, M_7 = 300mV$$

$$I_{bias} = 400mV$$

$$V_{DD} = 1.5V$$



**Step 5 :-** After the distribution of  $V_{Dsat}$  we get  $g_m$  values for all transistors

$$g_{mx} = \frac{\partial I_{Dx}}{\partial V_{Dsatx}}$$

$$g_m \rightarrow g_{m3} = \frac{1.5mA}{200mV}$$

$$\left\{ \begin{array}{l} \therefore I_{D3} = 750\mu A \\ V_{Dsat23} = 200mV \end{array} \right\}$$

$$\therefore g_m + g_{m3} = 7.5mS$$

$$g_{m5}, g_{m7} = \frac{1.5 \text{ mA}}{300 \text{ mV}}$$

$$\left. \begin{array}{l} \therefore I_{D7,5} = 760 \text{ mA} \\ V_{Dsat7,5} = 300 \text{ mV} \end{array} \right\}$$

$$g_{m5}, g_{m7} = 5 \text{ mA}$$

$\Rightarrow$  For  $(\frac{W}{L})$  calculation,  $t_{ox}$ ,  $\mu_p, \mu_n$  are required.

Step 6: From 130 nm model file

$$\mu_p = 83.5, \mu_n = 592.8, t_{ox} = 2.25 \times 10^{-9}$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = 1.534 \times 10^{-6}$$

$$\mu_p C_{ox} = 128.08 \text{ } \mu\text{A/V}^2$$

$$\mu_n C_{ox} = 909.35 \text{ } \mu\text{A/V}^2$$

We know that

$$I_{Dx} = \frac{\mu_x C_{ox}}{2} \left( \frac{W}{L} \right)_x (V_{Dsat})_x^2 \quad \{ x: P \text{ or N mosfet} \}$$

$$g_{mx} = \sqrt{2 I_{Dx} \mu_x C_{ox} \left( \frac{W}{L} \right)_x}$$

$$\therefore \left( \frac{W}{L} \right)_x = \frac{g_{mx}^2}{2 I_{Dx} \mu_x C_{ox}}$$

$$\left( \frac{W}{L} \right)_{1-4} = \frac{(7.5)^2 \times 10^{-6}}{(1.5 \times 10^{-3} \times 909.35 \times 10^{-6})}$$

$$\left( \frac{W}{L} \right)_{1-4} = 41.23$$

$$\left(\frac{w}{l}\right)_{5-8} = \frac{5^2 \times 10^{-6}}{1.5 \times 10^{-3} \times 128.08 \times 10^{-6}}$$

$$(w/l)_p = 130.12$$

**Step 7:** Calculation of  $V_{b1}, V_{b2}$ :

$$V_{b1} = V_{Dsat_3} + V_{Dsat_5} + V_{Dsat_{2p}bias} + V_{Tn}$$

$$V_{Tn} = 0.3782 \text{ Volts} \quad \text{from PTM file}$$

$$\therefore V_{b1} = 0.2 + 0.2 + 0.4 + 0.3782$$

$$V_{b1} = 1.1782 \text{ Volts}$$

$$V_{b2} = 1.5 - V_{Dsat_7} - V_{Dsat_5} - (V_{tp}) \quad \text{where } V_{tp} = 0.321 \text{ Volts}$$

$$V_{b2} = 1.5 - 0.3 - 0.3 - 0.321$$

$$V_{b2} = 0.5479 \text{ Volts}$$

$\Rightarrow$  For gain of 55.53 dB, unity gain bandwidth 2.47 GHz the simulated values for telescopic slot are as follows:

$$V_{b1} = 1.065 \text{ Volts} \quad V_{b2} = 0.6547 \text{ Volts}$$

$\Rightarrow$  Keeping  $(w/l)$  same, change in length changes the width as well.

$$\therefore \left(\frac{w}{l}\right)_{1,2} = \frac{137.43}{0.3} \quad \leftarrow \text{new } (w/l) \text{ after changing } l \text{ to } 0.3 \mu\text{m}$$

$$\text{where } 41.23 \times 0.3 = 127.43 \mu\text{m}$$

$$\text{Similarly, } (w/L)_{3,4} = \frac{54.97}{0.75}, \quad (w/L)_{5,6} = \frac{130.12}{1\mu\text{m}}. \quad (\text{same as earlier})$$

$$(w/L)_{7,8} = \frac{162.65}{0.8} \quad \left\{ \text{from } \frac{130.12 \mu\text{m}}{1\mu\text{m}} \right\}$$

**Step 7:** For second stage

$$V_{CM} \text{ of 1st stage} = 0.725 \text{ volts} \quad \{\text{from simulation}\}$$

$$\therefore V_{S8,10} = 1.5 - 0.725 \Rightarrow 0.775 \text{ V}$$

$$V_{D8at,10} = 0.775 - 0.821 = 0.454 \text{ V}$$

$$\text{current in 2nd stage} = 400 \mu\text{A}$$

$$\therefore V_{D8at,10} = 0.454 \text{ volts}$$

$$\therefore g_{m10} = \frac{800 \mu\text{A}}{0.454} = \approx 1.76 \text{ mS}$$

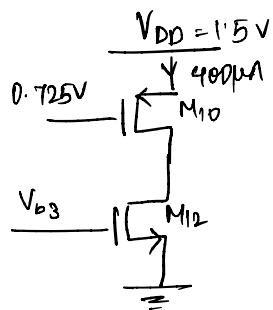
$$(w/L)_{10} = \frac{1.76^2 \times 10^{-6}}{800 \mu\text{A} \times 128.08 \times 10^{-6}}$$

$$(w/L)_{10,9} = 30.23$$

$$\text{let } g_{m10} = g_{m12} = 1.76 \text{ mS}$$

$$\therefore (w/L)_{12,11} = \frac{1.76^2 \times 10^{-6}}{800 \mu\text{A} \times 909.25 \times 10^{-6}}$$

$$(w/L)_{12,11} = 4.25$$

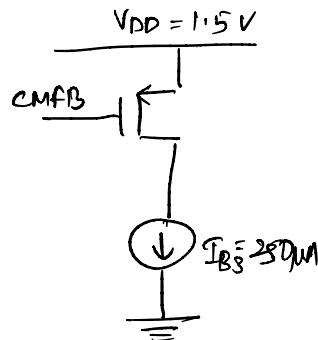


**Step 8 :** For CMFB :

$$V_{CM} = 0.725 \text{ Volts}$$

$$V_{Dsat}_{13,14} = 1.5 - 0.725 - 0.321$$

$$V_{Dsat}_{13,14} = 0.454 \text{ Volts}$$



$$\therefore g_m_{13,14} = \frac{500\mu}{0.454} = 1.101 \text{ mS}$$

$$(W/L)_{13,14} = \frac{(1.101)^2 \times 10^{-6}}{500\mu \times 128.08\mu}$$

$$(W/L)_{13,14} = 18.92$$

$\Rightarrow$  For gain of 82.222 dB, unity gain BW of 1.04 GHz & Phase margin of 117.43°.

$\Rightarrow$  The simulated values are given as:

$$(W/L)_{9,10} = \frac{51.76 \text{ nm}}{0.6 \mu\text{m}} \quad \text{from } \left( \frac{30.23}{1} \right)$$

$$\text{where } 30.23 \times 0.6 = 51.76$$

$$(W/L)_{12,11} \text{ is same as earlier} = \frac{4.25 \text{ nm}}{1 \mu\text{m}}$$

$$(W/L)_{13,14} = \frac{18.92}{1} \text{ to } \frac{23.64875 \mu\text{m}}{0.8 \mu\text{m}}$$

Currents in each stage has changed.

for  $I_{B1} = 1.5 \text{ mA}$  : same as earlier.

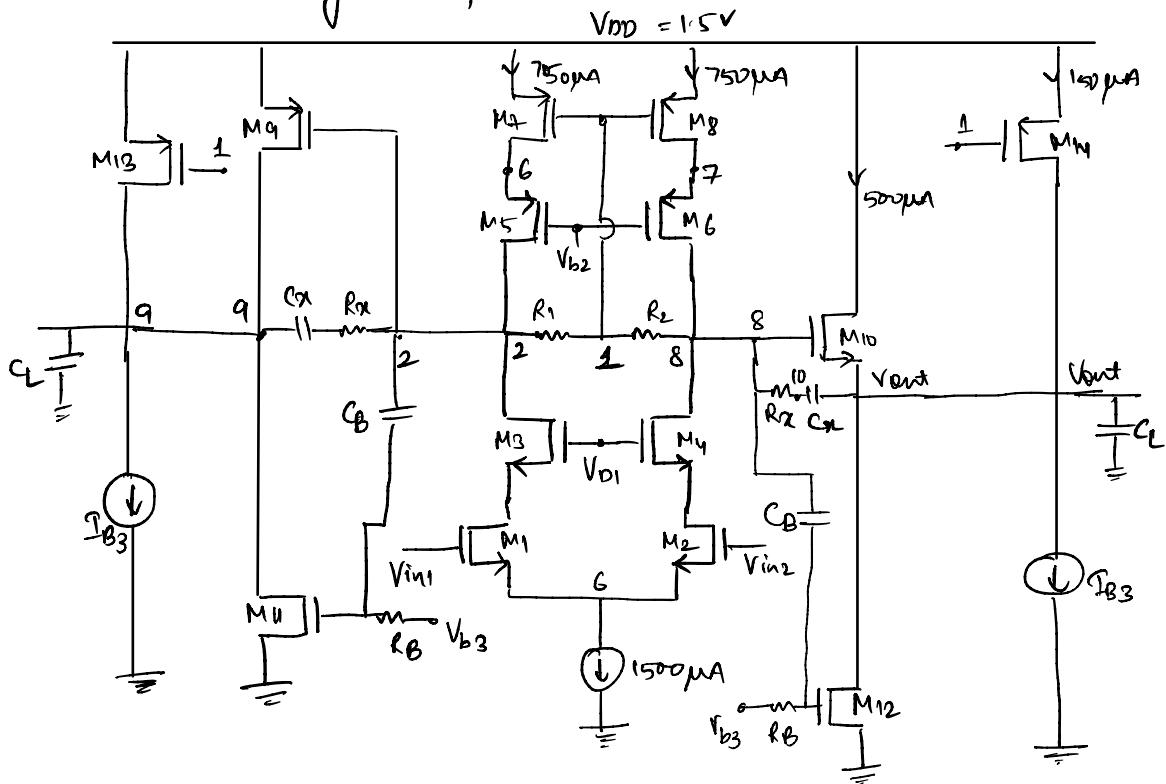
$I_{B2} \approx 500 \mu\text{A} \rightarrow$  from  $400 \mu\text{A}$

$I_{B3} \approx 150 \mu\text{A} \rightarrow$  from  $250 \mu\text{A}$

⇒ After simulation:

Also,  $R_Z = 30 \text{ k}\Omega$ ,  $C_Z = 0.8 \text{ pF}$ ,  $R_B = 20 \text{ k}\Omega$ ,  $R_1 = R_2 = 2 \text{ M}\Omega$ ,  
 $C_B = 200 \text{ fF}$

⇒ Circuit diagram for netlist:



## Iterations of the design flow:

1st Iteration: For calculated values of telepole ( $\omega/L$ ) for 1 $\mu m$  length, the gain was coming out to 30 dB with UGB = 70 MHz

2nd Iteration:  $(\omega/L)_{7,8} = \frac{136.49}{0.95}$        $(\omega/L)_{1,2} = \frac{54.97}{0.75}$

 $(\omega/L)_{3,4} = \frac{54.97}{0.75}$        $(\omega/L)_{5,6} = \frac{130.12}{1}$

Increasing  $(\omega/L)_{7,8}$  gives better UGB.

"  $(\omega/L)_{1,2} \Delta (\omega/L)_{3,4}$  gives better gain

→ obtained gain = 42 dB with UGB = 1.5 GHz

3rd Iteration:  $(\omega/L)_{7,8} = \frac{144.78}{0.9}$  ,  $(\omega/L)_{1,2} = \frac{82.46}{0.5}$

$$\left\{ \begin{array}{l} (\omega/L)_{3,4} = \frac{54.97}{0.75} \\ (\omega/L)_{5,6} = \frac{130.12}{1} \end{array} \right\} \Rightarrow \text{fixed.}$$

Obtained gain = 49 dB , UGB = 1.6 GHz

## 4th Iteration:

$(\omega/L)_{7,8} = \frac{162.65}{0.8}$  } fixed as further BW is not increasing  
nor will gain.

$(\omega/L)_{1,2} = \frac{108.075}{0.4}$

Obtained gain = 52dB , UGB = 2.77 GHz

5<sup>th</sup> Iteration :  $(w/L)_{11,12} = \frac{137.43}{0.3}$

obtained gain = 55.53 dB , UGB = 2.77 GHz

For 2nd stage : same pattern was followed.

After 4 such iterations,

$$(w/L)_{9,10} = \frac{51.76}{0.6} , (w/L)_{11,12} = \frac{4.25}{1} , (w/L)_{13,14} = \frac{23.643}{0.8}$$

### Amplifier device sizes.

Transistor	w/L ( $\mu\text{m}/\mu\text{m}$ )
M <sub>1</sub> - M <sub>2</sub>	137.43   0.3
M <sub>3</sub> - M <sub>4</sub>	54.97   0.75
M <sub>5</sub> - M <sub>6</sub>	180.12   1
M <sub>7</sub> - M <sub>8</sub>	162.65   0.8
M <sub>9</sub> - M <sub>10</sub>	51.76   0.6
M <sub>11</sub> - M <sub>12</sub>	4.25   1
M <sub>13</sub> - M <sub>14</sub>	23.64   0.8

## Auxiliary circuit Design.

Step 1: design of pre-amp.

Let pre-amp gain = 10

$$I_{bias} = 200\mu A, R_1 = 2.25 k\Omega$$

$$\text{gain} = g_{m1} (R_1 \parallel r_{o1})$$

$$\text{where } r_{o1} = \frac{1}{g_m I_{bias}} = \frac{1}{g_{ds1}}$$

By simulation:  $\lambda = 0.03235$

$$r_{o1} = \frac{1}{0.03235 \times 200\mu A} = 154.55 \text{ kHz}$$

$$g_{m1} (154.55 \parallel 2) = 10 \text{ mS}$$

$$g_{m1} = 5.064 \text{ mS.}$$

$$\text{Now } (\omega/L)_{1-2} = \frac{(25.65) \times 10^{-6}}{400\mu \times 909.35}$$

$$(\omega/L)_{1-2} = 70.52.$$

Step 2: for class-B

We know that, it works only to pump/sink current in one cycle where either PMOS or NMOS will be ON.

∴ They both should be in sub-threshold region.

for calculation of high slew rate we need spikes of current around 1.2 mA in +ve & -ve side

So, the value of  $(W/L)_{MP_1, MP_2} = 2.5 (W/L)_{ID}$

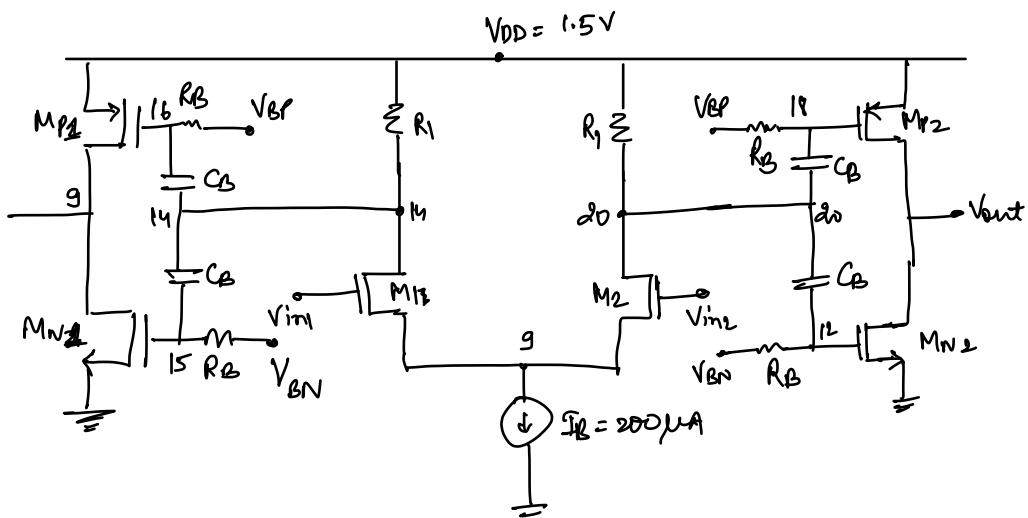
$$\therefore (W/L)_{MP_1, MP_2} = 2.5 \times 30.230 = \frac{75.575}{1 \mu\text{m}} \mu\text{m}$$

$\Rightarrow$  Mobility factor ( $\gamma$ ) from PTM file.

$$\gamma = \frac{134}{52} = 2.57$$

$$\text{and } (W/L)_{MN_1, MN_2} = \frac{75.575}{\gamma} = 29.4$$

$\Rightarrow$  For value of  $C_B$  and  $R_B$ , below setup is used to generate spike in off capacitor  $C_L = 0.5\text{pf}$  and got values as  $R_B = 25\text{k}\Omega$ ,  $C_B = 0.1\text{pf}$ ,  $R_1 = 7.75\text{k}\Omega$ .



$$V_{BP} = 1.2\text{V} \text{ and } V_{BN} = 0.3\text{V}$$

$\Rightarrow$  for iterations 8

used LT-Spice to get  $(W/L)$  for all transistors with input to

$$V_{BP} = 1.2V \quad \Delta \quad V_{BN} = 0.3V$$

In order to get high spikes of  $1.2mA$ . when either PMOS & NMOS gets into cutoff.

Keeping  $V_{BP}$  &  $V_{BN} = 0.3V$ .  $R_B = 25k\Omega$ ,  $C_B = 0.7pF$ .

1st Iteration:  $(W/L)_{MP_1, MP_2} = \frac{75 \cdot 575}{1}$

$$(W/L)_{MN_1, MN_2} = \frac{29 \cdot 4}{1}$$

We got spikes of around  $400 \mu A$ .

2nd iteration:  $(W/L)_{MP_1, MP_2} = \frac{180 \cdot 76}{0.75}, \quad (W/L)_{MN_1, MN_2} = \frac{39.2}{0.75}$

obtained spikes  $\approx 650 \mu A$ .

3rd iteration:

$$(W/L)_{MP_1, MP_2} = \frac{151 \cdot 15 \mu m}{0.5} \quad (W/L)_{MN_1, MN_2} = \frac{58.8}{0.5}$$

obtained spikes  $\approx 890 \mu A$ .

4th iteration:

$$(W/L)_{MP_1, MP_2} = \frac{302 \cdot 3}{0.25}, \quad (W/L)_{MN_1, MN_2} = \frac{117 \cdot 6}{0.25}$$

obtained spikes  $= 970 \mu A$ .

5th iteration:  $(\omega/L)_{MP1, MP2} = \frac{377 \cdot 875}{0.2}$ ,  $(\omega/L)_{MN1, MN2} = \frac{147}{0.2}$

obtained spikes  $\approx 1.05 \text{ mA}$ .

6th iteration:  $(\omega/L)_{MP1, MP2} = \frac{397 \cdot 73}{0.19}$ ,  $(\omega/L)_{MN1, MN2} = \frac{154 \cdot 73}{0.19}$

obtained spikes  $= 1.1 \text{ mA}$

7th iteration:

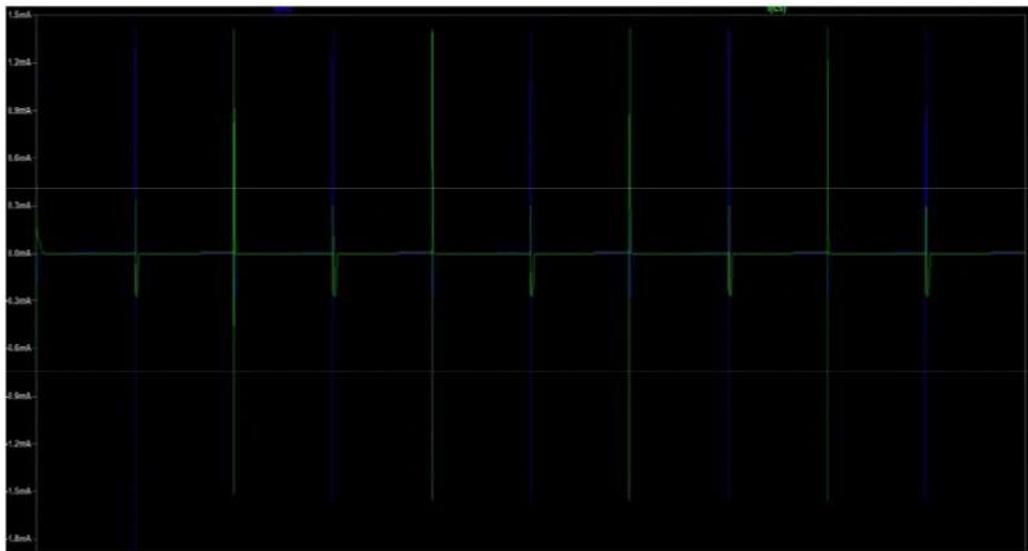
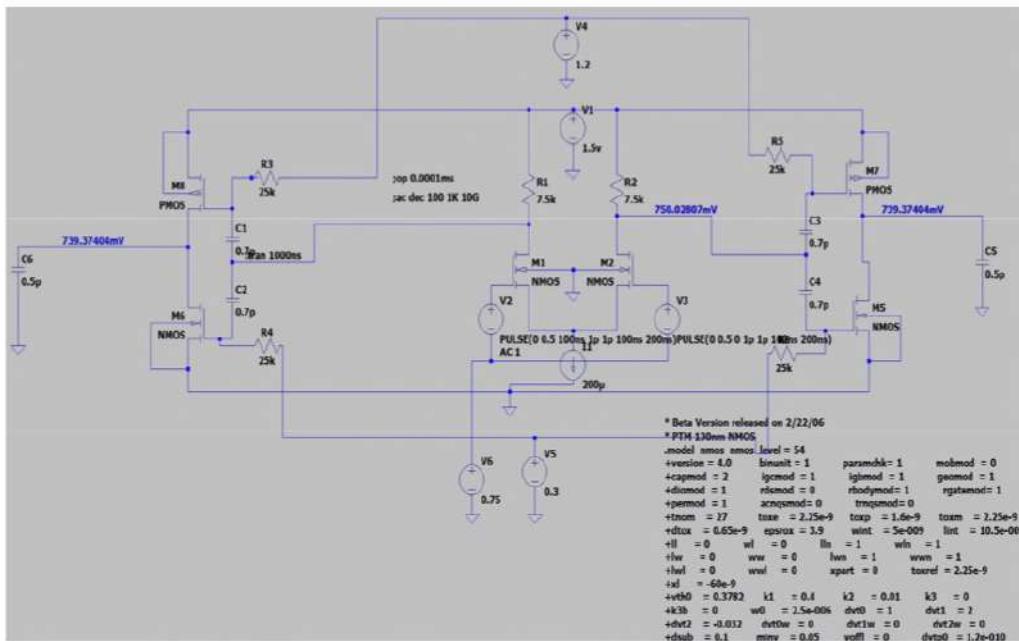
$$(\omega/L)_{MP1, MP2} = \frac{419 \cdot 86}{0.18}, (\omega/L)_{MN1, MN2} = \frac{163 \cdot 33}{0.18}$$

obtained spikes  $\approx 1.2 \text{ mA}$ .

$\Rightarrow$

Transistor	$(\omega/L) \text{ } \mu\text{m}/\mu\text{m}$
M <sub>1</sub> - M <sub>2</sub>	70.52 / 1
M <sub>N1</sub> - M <sub>N2</sub>	419.86 / 0.18
M <sub>P1</sub> - M <sub>P2</sub>	163.33 / 0.18

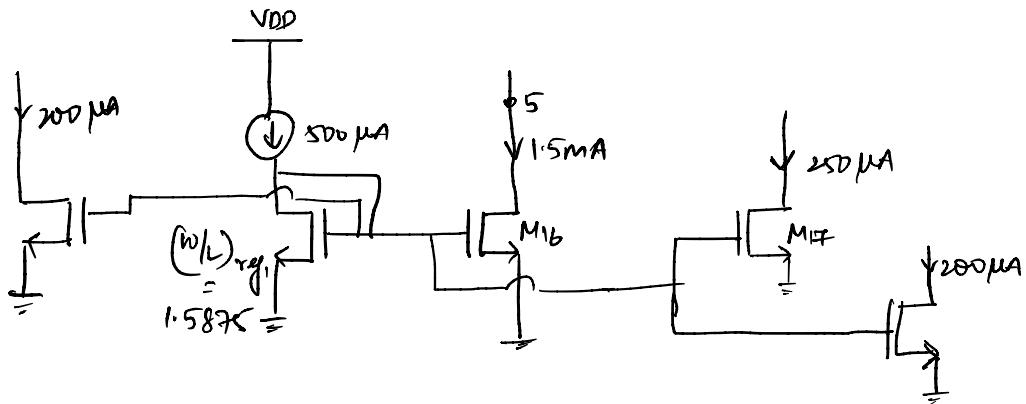
## LT SPICE SETUP AND REQUIRED CURRENT:



## Current Reference generator Circuit design:

Given:  $T_{ref} = 50 \mu A$ ,

For  $T_{B1}$ ,  $T_{B2}$ ,  $T_B$  and ( $T_B$  for auxiliary)



Now for 1.5mA from 50mA, we get  $V_{ocat16} = 450\text{mV}$  from budget

$$g_{\text{MIS}} = 10 \text{ mS}$$

$$\text{Now } \left(\frac{w}{l}\right)_{lb} = \frac{100 \times 10^{-6}}{3 \times 10^{-6} \times 909.85} = \frac{36.65 \mu\text{m}}{1 \mu\text{m}}$$

Now we know,

$$\left(\frac{\omega}{c}\right)_{\text{ref}} = \left(\frac{\omega}{c}\right)_{16} \times \frac{T_{\text{ref}}}{T_{\text{cont}}} = \frac{36.65 \times 50 \mu A}{1.5 \text{ mA}} = \left(\frac{1.5^3}{1}\right) \mu s$$

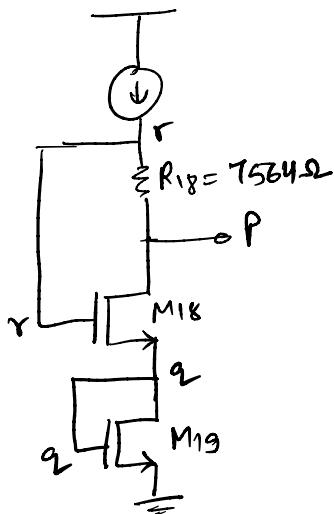
For  $\text{I}_{\text{Bim3}}$  :  $(w/L) = 5 \times 1.5825$

$$\omega/L = (7.91/1) \mu\text{m}$$

for *floras* of auxiliaries etc.

$$(w/L)_{\text{Aua}} = 4 \times 1.5825 = (6.331)$$

Now for  $V_{b1}, V_{b3} = 1.065V$



$$I_{ref} \times R_{18} \approx V_{t_{18}}$$

$$R_{18} = \frac{0.3782}{50\mu A}$$

$$R_{18} = 7.564\Omega$$

$$\text{Now } V_{G_{18}T_{18}} = 1 - 0.3782$$

$$V_{G_{18}T_{19}} = V_{D_{19}T_{19}} = 0.62V$$

$$V_P = V_{D_{sat18}} + V_{G_{18}T_{19}}$$

∴ We get

$$V_{D_{sat18}} = 0.6868 \text{ Volts}$$

Now  $g_{m18} = 0.45 \text{ mS}$ , we get

$$(w/l)_{18} = \frac{2.22 \text{ mV}}{1 \text{ \mu m}}$$

Similarly  $g_{m19} = 0.4 \text{ mS}$ , we get

$$(w/l)_{19} = \frac{1.75 \text{ mV}}{1 \text{ \mu m}}$$

⇒ For  $V_{b2} = 0.6547V$ .

$$I_{ref} \times R_{20} = 0.3782V$$

$$R_{20} = 7564\Omega$$

$$V_{D_{sat21}} = 0.6547 - 0.3782, V_{D_{sat21}} = 0.2765V$$

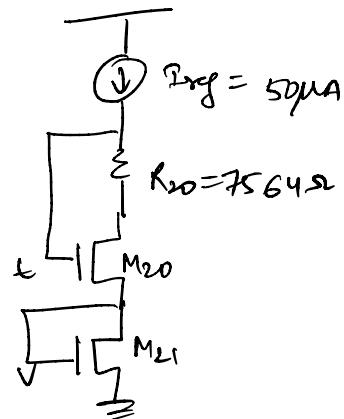
$$\sqrt{V_{Dsat20}} = 0.379 \text{ V}$$

$$g_m20 = 0.909 \text{ mS}$$

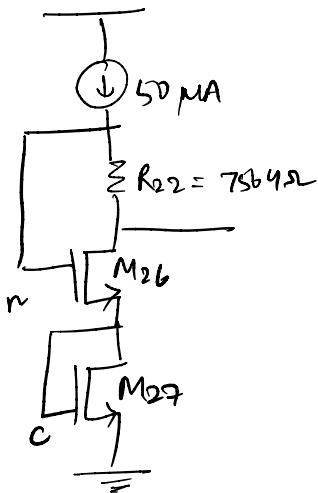
$$(w/l)_{20} = \frac{10 \mu\text{m}}{1 \mu\text{m}}$$

$$g_m21 = 1.02 \text{ mS}$$

$$(w/l)_{21} = \frac{12 \mu\text{m}}{1 \mu\text{m}}$$



$\Rightarrow$  For  $V_{BN} = 0.3 \text{ V}$ :



$$I_DQ \times R_{22} = 0.8782$$

$$R_{22} = 7564.52$$

$$V_{Dsat20} = 0.63 - 0.3782$$

$$V_{Dsat20} = -ve$$

$\therefore$  It was calculated through simulation.

$$(w/l)_{20} = \frac{120}{0.25} \quad , \quad (w/l)_{21} = \frac{45}{0.25}$$

## Current Reference Generator Device Sizes

Transistors	$(W/L)(\mu m/\mu m)$
M <sub>ref1</sub>	1.15825 / 1
M <sub>TB</sub>	2 / 1
M <sub>13</sub>	1.92918 / 1
M <sub>20</sub>	10 / 1
M <sub>21</sub>	11.08429 / 1
M <sub>22</sub>	5.762 / 1
M <sub>23</sub>	4.913 / 1
M <sub>24</sub>	2 / 1
M <sub>25</sub>	1.089 / 1
M <sub>26</sub>	+20   0.25
M <sub>27</sub>	4.913 / 1
M <sub>16</sub>	86.25 / 1
M <sub>17</sub>	5.762 / 1

To get the currents & voltages correct and 0V after the achieved values, the values of transistor widths have been tweaked from calculated values

## 4. DC operating point simulations.

### DC Operating point simulations:

#### For pseudo class AB:

```
No. of Data Rows : 1
v(vout) = 7.895558e-01
v(p) = 1.064016e+00
v(u) = 6.547001e-01
@m12[id] = 4.865931e-04
@m10[id] = 5.541172e-04
@m18[id] = 1.500631e-03
@m17[id] = 2.500005e-04
@m22[id] = 2.500005e-04
@m14[vds]-@m14[vgs]+@m14[vth] = 3.202046e-01
@m14[vgs]-@m14[vth] = 3.902396e-01
@m1[id] = 7.503035e-04
@m2[id] = 7.503035e-04
@m8[id] = 7.502852e-04
@m9[id] = 5.541172e-04
@m10[id] = 5.541172e-04
@m11[id] = 4.865931e-04
@m14[id] = 1.824507e-04
@m12[vds] = 7.895558e-01
@m14[id] = 1.824507e-04
@m13[id] = 1.824507e-04
@m2[gn] = 1.309345e-02
@m4[gn] = 7.178433e-03
@m6[gn] = 3.381701e-03
@m8[gn] = 2.100213e-03
@m12[vds] = 7.895558e-01
@m11[vds] = 7.895558e-01
1/@m2[gds] = 2.467059e+03
1/@m4[gds] = 1.845534e+04
1/@m6[gds] = 3.003806e+04
1/@m8[gds] = 2.535880e+02
@m6[gn]*((1/@m6[gds])*1/@m8[gds])) = 2.575940e+04
@m4[gn]*((1/@m4[gds])*1/@m2[gds])) = 3.268370e+05
@m10[gn] = 2.421754e-03
@m10[gn]*(1/(@m10[gds])*@m12[gds])) = 5.574336e+01
@m1[vgs]-@m1[vth] = 1.289964e-02
@m2[vgs]-@m2[vth] = 1.289964e-02
@m3[vgs]-@m3[vth] = 1.603621e-01
@m4[vgs]-@m4[vth] = 1.603621e-01
@m5[vgs]-@m5[vth] = 3.811007e-01
@m6[vgs]-@m6[vth] = 3.811007e-01
@m7[vgs]-@m7[vth] = 3.901960e-01
@m8[vgs]-@m8[vth] = 3.901960e-01
@m10[vgs]-@m10[vth] = 3.904378e-01
@m12[vgs]-@m12[vth] = 6.858157e-01
@m1[vds]-@m1[vgs]+@m1[vth] = 1.268635e-01
@m2[vds]-@m2[vgs]+@m2[vth] = 1.268635e-01
@m3[vds]-@m3[vgs]+@m3[vth] = 1.910505e-01
@m4[vds]-@m4[vgs]+@m4[vth] = 1.910505e-01
@m5[vds]-@m5[vgs]+@m5[vth] = 1.871191e-01
@m6[vds]-@m6[vgs]+@m6[vth] = 1.871191e-01
@m7[vds]-@m7[vgs]+@m7[vth] = -2.47060e-01
@m8[vds]-@m8[vgs]+@m8[vth] = -2.47060e-01
@m10[vds]-@m10[vgs]+@m10[vth] = 3.200064e-01
@m12[vds]-@m12[vgs]+@m12[vth] = 1.037401e-01
```

**For pseudo with auxiliary and reference generator:**

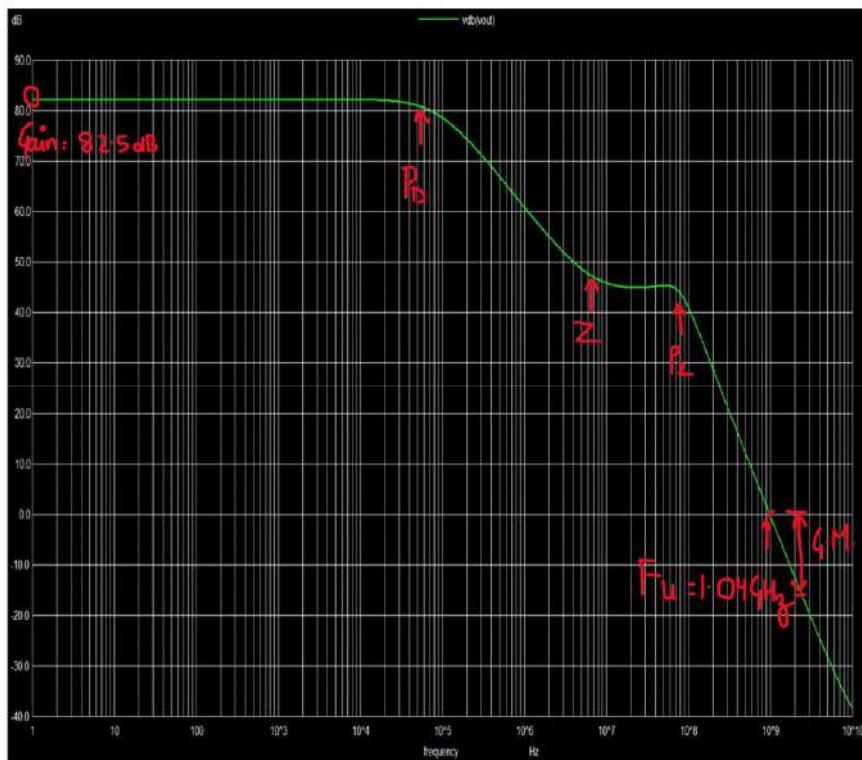
```
v(vout) = 7.358127e-01
v(p) = 1.064015e+00
v(u) = 6.547001e-01
v(f) = 1.200365e+00
v(m) = 3.000682e-01
@m16[id] = 1.500471e-03
@m22[id] = 2.499879e-04
@m23[id] = 2.000057e-04
@m12[id] = 4.853353e-04
@m10[id] = 5.550987e-04
@m16[id] = 1.500471e-03
@m17[id] = 2.499979e-04
@m22[id] = 2.499879e-04
@m14[vds]-@m14[vgs]+@m14[vth] = 3.740242e-01
@m14[vgs]-@m14[vth] = 3.901631e-01
@m1[id] = 7.502234e-04
@m2[id] = 7.502234e-04
@m8[id] = 7.502051e-04
@m9[id] = 5.550987e-04
@m10[id] = 5.550987e-04
@m11[id] = 4.853353e-04
@m14[id] = 1.827086e-04
@m11[id] = 9.999940e-05
@m12[id] = 9.999940e-05
@m1[id] = 4.692526e-04
@m11[id] = 4.717622e-04
@m12[id] = 4.692526e-04
@m13[id] = 4.717622e-04
@m11[vds] = 4.289893e-01
@m12[vds] = 4.289893e-01
@m1[vds] = 7.641873e-01
@m11[vds] = 7.358127e-01
@m12[vds] = 7.358127e-01
@m11[vds] = 7.358127e-01
@m12[vds] = 7.358127e-01
@m12[id] = 4.853353e-04
@m8[gm] = 1.309235e-02
@m4[gm] = 7.178065e-03
@m6[gm] = 3.381544e-03
@m8[gm] = 2.100677e-03
@m12[vds] = 7.358127e-01
@m11[vds] = 7.358127e-01
1/@m2[gds] = 2.457612e+03
1/@m4[gds] = 1.846681e+04
1/@m6[gds] = 3.002934e+04
1/@m8[gds] = 2.536904e+02
@m6[gm]*((1/@m6[gds])*(1/@m8[gds])) = 2.576113e+04
@m4[gm]*((1/@m4[gds])*(1/@m2[gds])) = 3.270966e+05
(1/(@m2[gds]+@m4[gds])) = 2.176746e+03
@m10[gm] = 2.427391e-03
@m10[gm]*(1/(@m10[gds]+@m12[gds])) = 5.082139e+01
@m1[vgs]-@m1[vth] = 1.289349e-02
@m2[vgs]-@m2[vth] = 1.289349e-02
@m3[vgs]-@m3[vth] = 1.603506e-01
@m4[vgs]-@m4[vth] = 1.603506e-01
@m5[vgs]-@m5[vth] = 3.810780e-01
@m6[vgs]-@m6[vth] = 3.810780e-01
@m7[vgs]-@m7[vth] = 3.901153e-01
@m8[vgs]-@m8[vth] = 3.901153e-01
@m10[vgs]-@m10[vth] = 3.903734e-01
@m12[vgs]-@m12[vth] = 6.858137e-01
@m1[vds]-@m1[vgs]+@m1[vth] = 1.268730e-01
@m2[vds]-@m2[vgs]+@m2[vth] = 1.268730e-01
@m3[vds]-@m3[vgs]+@m3[vth] = 1.911342e-01
@m4[vds]-@m4[vgs]+@m4[vth] = 1.911342e-01
@m5[vds]-@m5[vgs]+@m5[vth] = 1.870384e-01
@m6[vds]-@m6[vgs]+@m6[vth] = 1.870384e-01
@m7[vds]-@m7[vgs]+@m7[vth] = -2.46957e-01
@m8[vds]-@m8[vgs]+@m8[vth] = -2.46957e-01
@m10[vds]-@m10[vgs]+@m10[vth] = 3.738140e-01
@m12[vds]-@m12[vgs]+@m12[vth] = 4.999894e-02
```

## 5. AC Simulations.

### AC simulations:

For pseudo class AB:

Magnitude plot (in db):



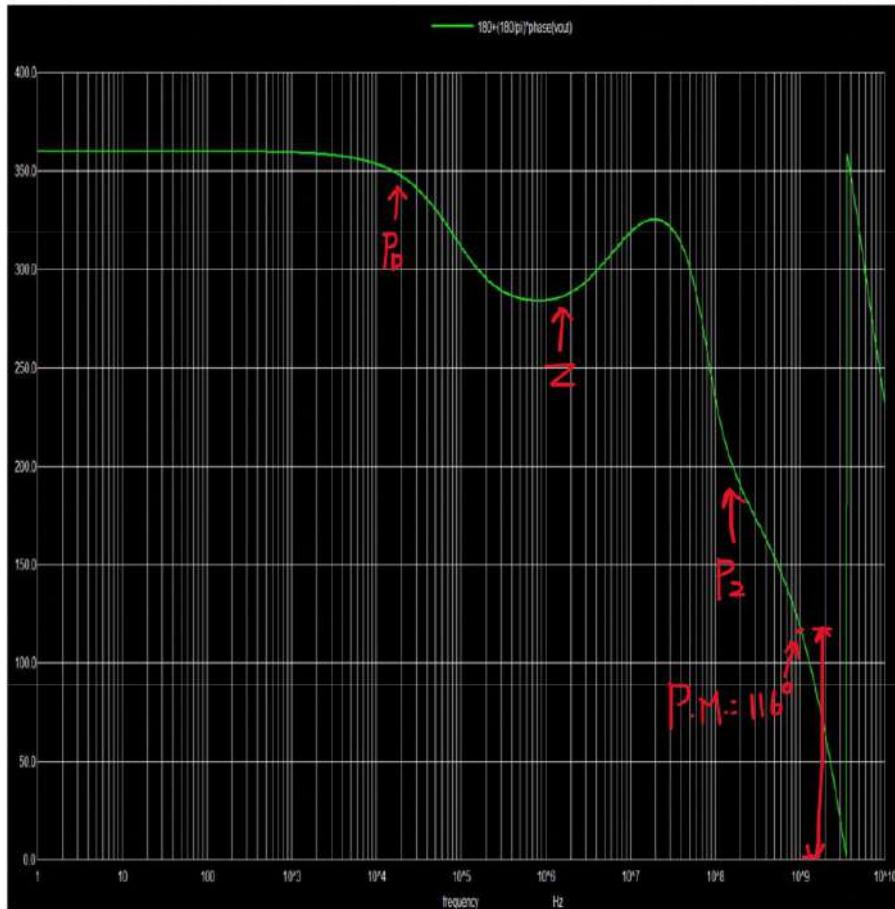
The above graph shows the value of gain achieved by the pseudo class AB amplifier with unity gain frequency ( $F_u$ )=1.04Ghz which is also the gain cross over frequency which will determine the value of phase and then phase margin. Gain in dB obtained is 82.5dB

We can observe that the dominant pole is  $7 \times 10^4$  hz and it decreases the gain by -40dB but this get compensate by the zero around  $9 \times 10^6$ hz.

But due to the pole P<sub>2</sub> the slope will again decrease with -40dB and will eventually meet 0dB line at 1.04Ghz.

And the phase cross over frequency is 3.184Ghz so the gain at this frequency is -23dB Therefore G.M. = 23dB.

### PHASE/PHASE MARGIN PLOT:



Since -180-degree line doesn't come in ngspice I have calculated for the Phase margin by adding 180 degrees to the phase and we get the phase margin of 116 degrees. With phase of -64 degrees.

We can clearly see the effects caused by the pole  $P_d$ ,  $P_2$  and  $Z$  around the same frequencies as mentioned earlier

**Simulator output:**

x-frequency

y-gain

 ngspice 35

- □ ×

```
Trying gmin = 4.5316E-05 Note: One successful gmin step
Trying gmin = 3.2781E-05 Note: One successful gmin step
Trying gmin = 2.0169E-05 Note: One successful gmin step
Trying gmin = 9.7338E-06 Note: One successful gmin step
Trying gmin = 3.2634E-06 Note: One successful gmin step
Trying gmin = 6.3352E-07 Note: One successful gmin step
Trying gmin = 6.3352E-08 Note: One successful gmin step
Trying gmin = 6.3352E-09 Note: One successful gmin step
Trying gmin = 6.3352E-10 Note: One successful gmin step
Trying gmin = 6.3352E-11 Note: One successful gmin step
Trying gmin = 6.3352E-12 Note: One successful gmin step
Trying gmin = 1.0000E-12 Note: One successful gmin step
Note: True gmin stepping completed

No. of Data Rows : 1001
ngspice 8 ->
x0 = 1.03847, y0 = 82.5

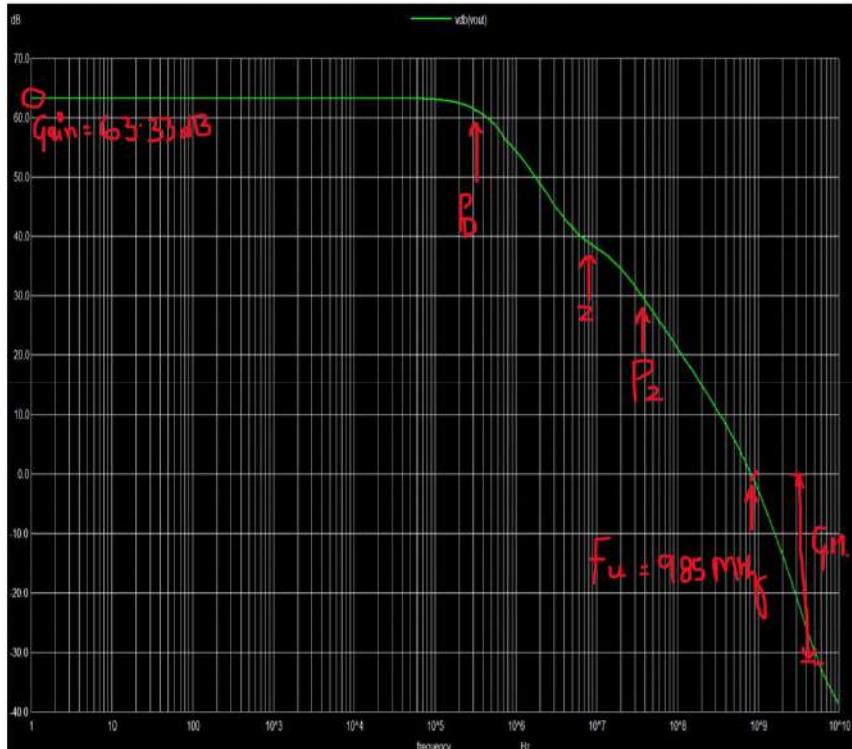
x0 = 1.04384e+09, y0 = 0

x0 = 1.09078e+09, y0 = 113.208
```

Simulator results prove that at low frequencies the gain is 82.5 constant but afterwards decreases and the phase margin at this can be seen is 116 degrees.

For Full circuit:

Magnitude plot (in db):



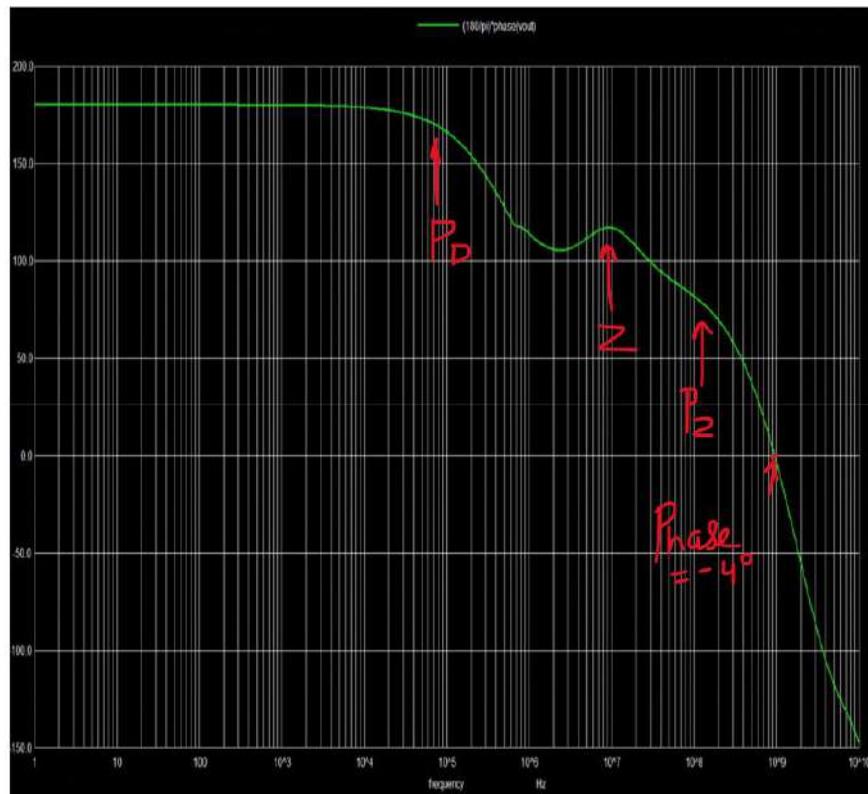
The above graph shows the value of gain achieved by the pseudo class AB amplifier with unity gain frequency ( $F_u$ )=985Mhz which is also the gain cross over frequency which will determine the value of phase and then phase margin. Gain in dB obtained is 63.33dB

We can observe that the dominant pole is  $4 \times 10^5$  hz and it decreases the gain by -40dB but this get compensate by the zero around  $9 \times 10^6$ hz.

But due to the pole P2 the slope will again decrease with -40dB and will eventually meet 0dB line at 985Mhz.

And the phase cross over frequency is 5Ghz so the gain at this frequency is -31dB Therefore G.M. = 31dB.

PHASE PLOT:



We get the phase margin of 176 degrees. With phase of -4 degrees.

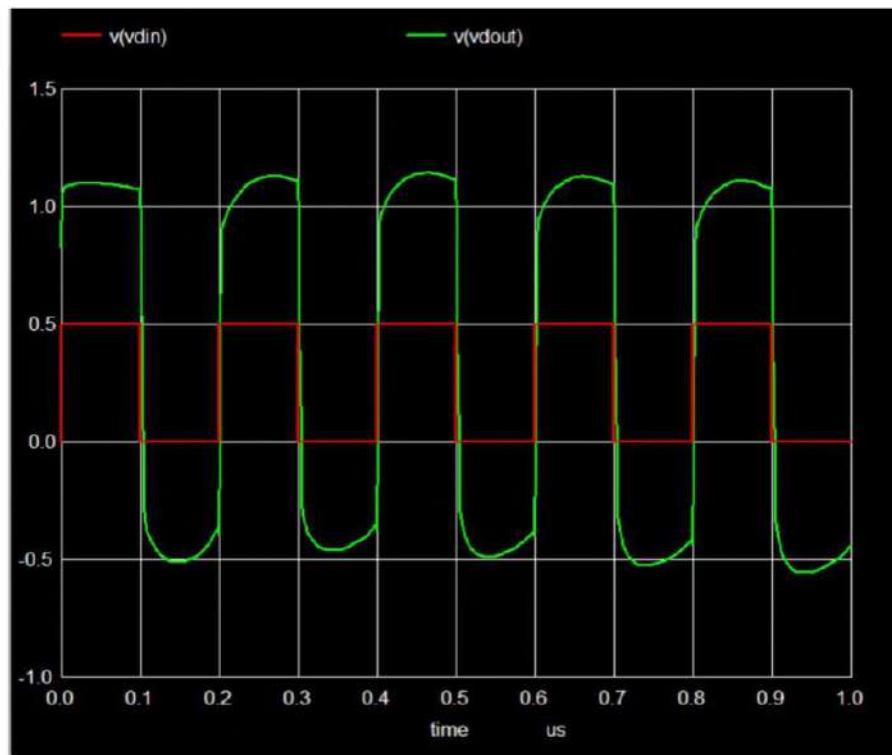
We can clearly see the effects caused by the pole  $P_d$ ,  $P_2$  and  $Z$  around the same frequencies as mentioned earlier.

After adding the auxiliary circuit, we get a rise in phase and loss in unity gain BW.

## 6. Settling Time & Slew rate calculation.

### Settling Time & Slew rate calculation:

For pseudo class AB:

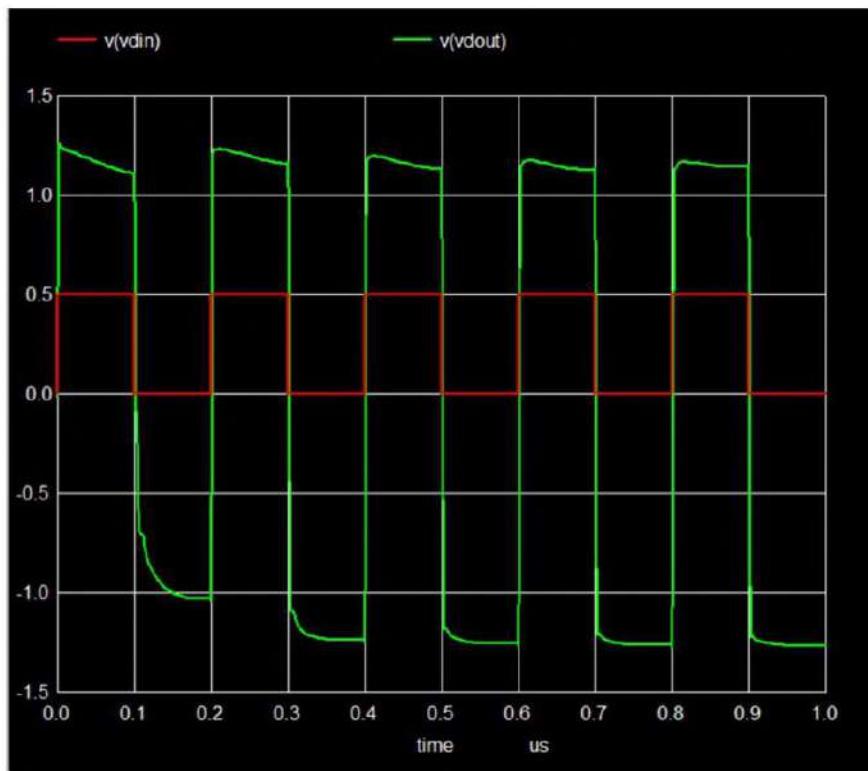


```
ngspice 35
n          0.678285
c          0.292496
10         0.931893
11         0.64324
12         0.6547
13         0.6547
vn1        0.75
vn2        0.75
vck2#branch 3.21168e-07
vck1#branch 3.21168e-07
v3#branch   -2.1305e-09
v2#branch   -2.15633e-09
vl#branch   -0.00364741

No. of Data Rows : 678
drise       = 5.326544e-10 targ= 4.015079e-07 trig= 4.009752e-07
dfall       = 8.149778e-10 targ= 3.026176e-07 trig= 3.018026e-07
ngspice 214 ->
```

Rise time seen by simulator is 0.532ns and fall time as 0.814ns.

For Full circuit:



```
ngspice 35
12          0.6547
13          0.6547
14          1.5
20          1.5
vm1         0.75
vm2         0.75
vin1        0
vin2        0
vck2#branch
vck1#branch
v3#branch   -2.13855e-09
v2#branch   -2.13955e-09
v1#branch   -0.00312187

No. of Data Rows : 522
drise       = 1.599271e-10 targ= 2.011622e-07 trig= 2.010022e-07
dfall       = 2.616452e-10 targ= 3.013846e-07 trig= 3.011230e-07
ngspice 238 ->
```

sl\_2.cir -- ready -- Quit

Rise time seen by simulator is 0.159ns and fall time as 0.261ns.

## Step Rate Calculation for Pseudo class AB amplifier

$$SR^+ = \frac{0.3}{\text{time reqd for } V_{out} \text{ to reach from } 0V \text{ to } 0.3V}$$

$$SR^- = \frac{0.2}{\text{time reqd for } V_{out} \text{ to reach from } 0.5V \text{ to } 0.2V}$$

So,

$$SR^+ = \frac{0.3}{5.3265 \times 10^{-10}} = 563.22 \text{ V/μsec}$$

$$SR^- = \frac{0.2}{8.14977 \times 10^{-10}} = 368.108 \text{ V/μsec.}$$

avg SR =  $465.654 \text{ V/μsec}$

Step rate calculation for pseudo class AB with auxiliary class B booster ckt.

$$SR^+ = \frac{0.3}{\text{time taken from } 0 \rightarrow 0.3}$$

$$SR^- = \frac{0.2}{\text{time taken from } 0.5 \text{ to } 0.2}$$

SR for pseudo class AB with auxiliary ckt

$$SR^+ = \frac{0.3}{1.599 \times 10^{-10}} = 1875.25 \text{ V/μsec.}$$

$$SR^- = \frac{0.2}{2.816 \times 10^{-10}} = 1146.57 \text{ V/μsec.}$$

To average slew rate with auxiliary circuit

$$= 1510.97 \text{ V/μsec.}$$

⇒ 1% settling time calculation

$$\frac{0.5 - 0.5}{100} \approx 0.5 \text{ volt}$$

For Pseudo AB,

$$\text{So time taken to settle down} = 8.7176 \times 10^{-10} \text{ sec.}$$

For Pseudo Class AB with auxiliary.

$$\text{Settling time} = 2.423 \times 10^{-10} \text{ sec.}$$

### Common Mode Analysis

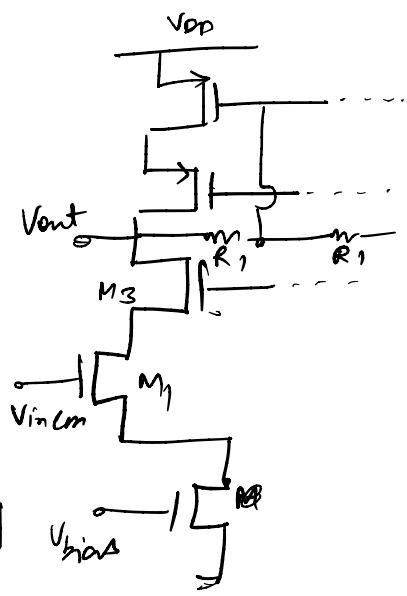
Common mode input range is

So the upper limit on  $V_{inCM}$  can be calculated from here.

$$V_{DD} - V_{GS1} - V_{GS2} > V_{inCM} - |V_{Th}|,$$

$$V_{inCM} < V_{DD} - V_{GS1} - V_{GS2} + V_{Th}$$

$$\begin{aligned} V_{inCM} &< V_{DD} - |V_{GS1}| - |V_{Th}| - |V_{GS2}| \\ &\quad + |V_{Th}| \end{aligned}$$



after putting the minimum value of  $(V_{GAT})_{\min} = 0$

$$V_{in,cm} < V_{DD} - |V_{TP}| + |V_{TN}| \quad \text{--- (1)}$$

Now the lower limit  $\rightarrow$

$$V_{in,cm} - V_{GSI} - |V_{GAT}|_{M_{2,3}} > 0$$

$$V_{in,cm} > |V_{GSI}| + |V_{GAT}|_{M_{2,3}}$$

now putting the minimum  $(V_{GAT})_{\min} = 0$

$$V_{in,cm} > V_{GSI} + 0$$

$$V_{in,cm} > \sqrt{\frac{d I_D}{k n C_o \left(\frac{W}{L}\right)}} + V_{th}$$

Range is given by

$$\sqrt{\frac{2 I_D}{k n C_o \left(\frac{W}{L}\right)}} + V_{th} < V_{in,cm} < V_{DD} - |V_{TP}| + |V_{TN}|$$

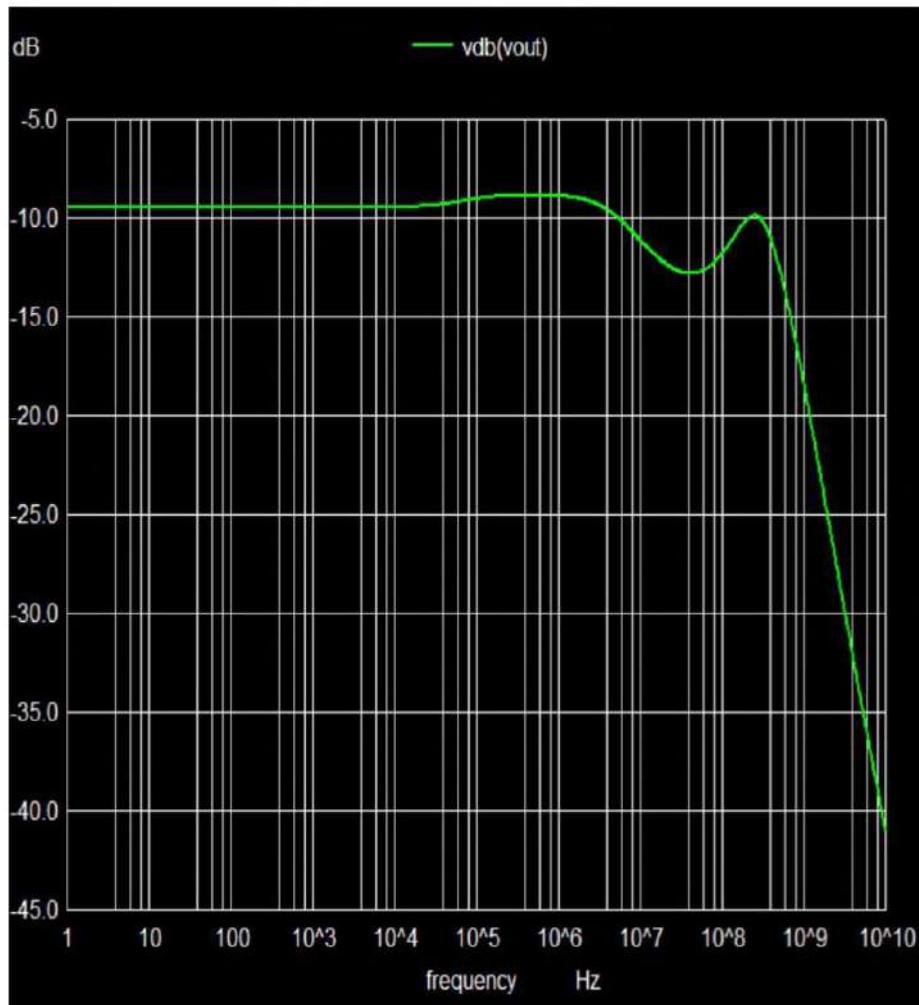
Range : 0.3782 V to 0.8008 V

$$CMRR = 20 \log \frac{A_{dm}}{A_{cm-dm}}$$

$$= 20 \log A_{dm} - 20 \log A_{cm-dm}$$
$$= 82.22 - (-9.56)$$

$$CMRR = 91.78 \text{ dB}$$

MAGNITUDE PLOT :



PHASE PLOT :

