Operational Transconductance Amplifier With Class-B Slew-Rate Boosting for Fast High-Performance Switched-Capacitor Circuits

Mohammad H. Naderi, *Student Member, IEEE*, Suraj Prakash, *Student Member, IEEE*, and Jose Silva-Martinez, *Fellow, IEEE*

***Abstract*— In this paper, a technique for slew-rate (SR) boosting suitable for switched-capacitor circuits is proposed. The proposed technique makes use of a class-B auxiliary amplifier that generates a compensating current only when high SR is demanded by large signals. The proposed architecture employs simple circuitry to detect the need for a large output current by employing a highly sensitive pre-amplifier followed by a class-B amplifier. The functionality of the class-B transconductance amplifier is dictated by a predefined hysteresis, and operates in parallel with the main amplifier. The proposed solution demands small static power (under 20% of main amplifier power) due to its class-B nature. The experimental results in a 40-nm CMOS technology show more than 45% reduction in slew time, and a 28% shorter slew time for 1% settling time when used in a typical 4.5 bit/stage block commonly used in pipelined analog-to-digital converters. Compared with the core amplifier, HD3 at 500 MHz reduces by more than 10 dB when the SR boosting circuit is activated.**

***Index Terms*— Slew rate boosting, switched-capacitor circuits, class B, linear settling, and high speed pipelined ADC.**

I. Introduction

MOST analog-to-digital converters (ADCs) like pipelined ADCs and discrete-time delta sigma modulators as well as high performance filters in the audio and video systems are based on switched-capacitor (SC) techniques [1]–[10]. For high-speed and large signal swing applications, the operational amplifier must settle into its final value within a time frame, which is a fraction of the main clock period, i.e., around 45% in the case of conventional two-phase SC circuits, which is usually in the range of nanoseconds for more than 100 MS/s (mega-samples per second) applications. For large signals, the settling process consists of two phases: slewing and linear settling. The slew phase does not require high precision, but a large amount of current is needed to more quickly move the output voltage from its initial condition closer to its final voltage value. Decreasing the slewing time allow us to allocate more time for the linear settling phase, which is dictated by loop bandwidth properties, e.g., gain-bandwidth products of the operational amplifier, loading conditions, feedback factor, and location of poles and zeros.

Usually, reducing the slewing time requires a large static current available at the amplifier's output to efficiently drive the feedback and load networks. The high current requirement at the output stage of a class-A amplifier must satisfy the high slew-rate needs, which drastically increases the amplifier's power consumption [11]–[15]. Current amplification has been used that is relying on increasing the tail-current efficiency by mirroring and amplifying the differential's input stage current [16]–[23]. In SC circuits, the differential current is produced by a differential voltage step at the beginning of the settling phase that turns one of the differential input transistors OFF and another input transistor ON [24]–[26]; this is especially noticeable in the presence of large input steps. The differential current, which is dictated by the input stage tail current, is mirrored and amplified and then delivered to the loading impedance. As a result, a high slew-rate is achieved at the expense of higher power consumption.

There are additional limitations in the case of low supply voltage deep sub-micron technologies. By reducing the full-scale voltage in pipeline ADCs, the voltage step across the differential input transistor is relatively small and may not exceed the input stage's overdrive voltage. This effect is often present when large number of bits per stage are used; the input voltage is reduced to be the ADC's full-scale value divided by 2^N; N being the number of bits resolved in that stage. Thus, only a small portion of the tail current used in the amplifier's input stage is processed, then resulting in slower settling time. Therefore, in order to maintain faster settling time, large amount of dc bias current is needed. Moreover, the extensive use of class-A circuits will limit solution's power efficiency.

The slew rate can be boosted by utilizing class-AB stages [27], [28]. In [28], a class-AB stage provides high dynamic current when demanded, but the bias current is relatively small. For switched-capacitor circuits, large current

Manuscript received April 3, 2018; revised June 4, 2018 and June 21, 2018; accepted June 25, 2018. Date of publication August 13, 2018; date of current version October 2, 2018. This work was supported by NSF under Contract 1509872. This paper was recommended by Associate Editor E. Bonizzoni. *(Corresponding author: Mohammad H. Naderi.)*

The authors are with the Department of Electrical and Computer Engineering, Texas A&M University, College Station, TX 77843 USA (e-mail: mh.naderi@tamu.edu; jose-silva-martinez@tamu.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSI.2018.2852273

TABLE I
ADVANTAGES AND DRAWBACKS OF AVAILABLE SLEW-RATE BOOSTING SOLUTIONS

Technique	Current Amplification [25]	Class-AB Stage [29]	This paper
SR correlated with Tail-Current	No	Yes	Yes
Functional for Low Supply Voltage	No	No	Yes
Fully functional for Multi-Bit (>3) Pipelined Stage	No	No	Yes
Required Optimization Between Different Building Blocks	No	Yes	No

values can be generated by utilizing a class-AB stage; however, the quiescent current has to be maintained at level such that the required linear settling requirements are satisfied. Settling errors are dictated by small signal parameters such as overall transconductance gain, bandwidth and low-frequency loop gain. Enhancing the slew rate utilizing a hybrid dynamic amplifier was proposed in [24]. However, the hybrid amplifier requires optimization of its different building blocks for slew rate, phase margin, stability, and accuracy. Also, since the initial step voltage in the pipelined stages decreases when increasing the number of bits per stage, the class-AB alone amplifier in [29] might not be able to perform well for the case of higher number of bits per stage. Therefore, only 2.5-bit pipelined stages are utilized which is not the most power efficient solution due to the required transconductance for the different pipelined ADC architectures [30]. Table I summarizes the properties of available architectures as well as the proposed slew-rate boosting technique.

In this work, we propose a slew-rate boosting technique based on the generation of high dynamic current when fast response is demanded. The proposed concept relies on monitoring the amplifier's input stage, employing a low-power single-stage ultra-fast preamplifier to detect the need for a higher current to boost the amplifier's slew-rate. Preamplifier output is used to drive a class-B amplifier with controlled hysteresis that can generate up to three times the current delivered by the main amplifier. Static power overhead is no more than 20%, and the noise level increases by 1dB; effects on input capacitance are negligible. The auxiliary circuit extends the frequency range of a 4.5 bit/stage residue amplifier from 400 MHz (core bandwidth) up to 780 MHz while maintaining the third harmonic distortion around −48 dB.

The paper is organized as follows. Section II discusses the slewing phase in operational transconductance amplifiers (OTA) when implementing switched capacitor circuits commonly employed in pipelined ADC stages. Section III discusses the proposed slew-rate boosting circuitry which uses a high-speed pre-amp followed by an auxiliary class-B amplifier. Section IV shows the simulation and measurement results and

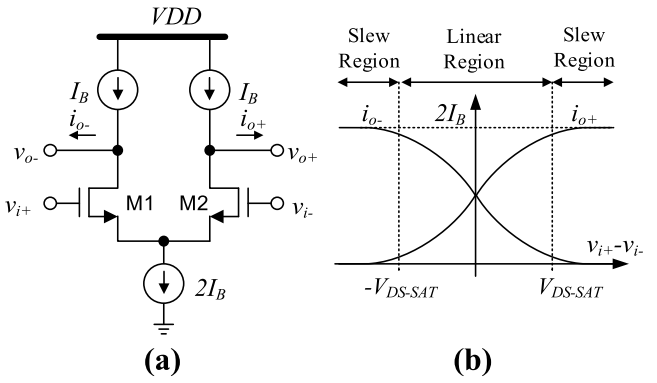


Fig. 1. (a) Differential pair and (b) output current versus the voltage across the input transistors in a simple OTA.

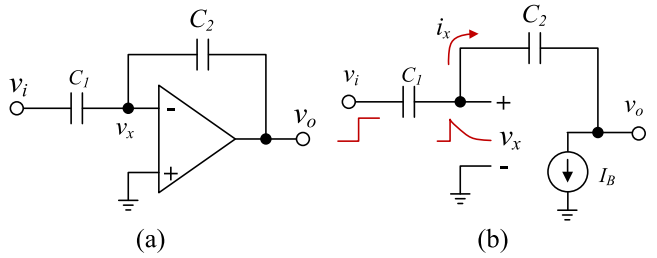


Fig. 2. Operation of the OTA when slewing in the switched capacitor gain stage without loading at the output stage.

discusses different operating conditions found in 4.5 bit/stage pipeline ADC applications. Finally, Section V presents the conclusions reached in this paper.

II. SLEW-RATE FUNCTION OF AN OTA BASED SC CIRCUIT

The output current versus the voltage across the gate of the input transistors in the simplest OTA is depicted in Fig. 1. The OTA's output current shows two different regions, the linear region and the slewing (saturation) region. When the input voltage across the differential pair is less than the overdrive voltage $V_{ds,sat}$, the transistors operate in their saturation regime, and in a first approximation the current is proportional to the differential input voltage. For input voltages larger than $V_{ds,sat}$, the current at differential pair ouputs remain constant; either one zero or $2I_B$.

A. Unloaded Switched-Capacitor Circuit

Let us consider the step response of a capacitive amplifier, commonly found in switched-capacitor circuits. Assuming zero initial conditions in the capacitors, when a large input step voltage is applied to the unloaded switched capacitor gain stage, the OTA acts as a constant DC-current source, as shown in Fig. 2. Right after the input step is applied, the voltage at the inverting terminal is identical to the input signal, which leads to

$$V_x = V_i = V_o \text{ at } t = t_{0+}. \tag{1}$$

If V_x is close or exceeds the overdrive voltage $V_{DS,sat}$, the OTA operates in the slew regime. The OTA generates the

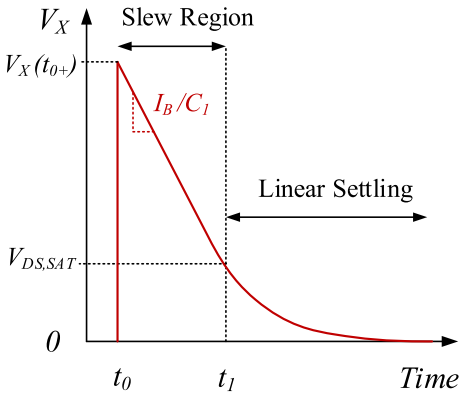


Fig. 3. Operational transconductance amplifier (OTA) waveform input voltage when slewing in the switched capacitor gain stage without loading at the output stage.

maximum possible current at its output and returns V_x towards ground as shown in the Fig. 3; V_x and the output voltage is estimated as follows.

$$V_x = V_i - \frac{I_B}{C_1}.(t - t_0) \tag{2}$$

$$V_o(t) = V_i - I_B.\left(\frac{1}{C_1} + \frac{1}{C_2}\right).(t - t_0)\,. \tag{3}$$

The output slew rate is a function of the I_B/C ratio and its boosting requires larger amount of current and/or use of smaller capacitors. Unfortunately, the capacitors cannot be reduced since the thermal kT/C noise level must be maintained at a low level; hence, a large amount of power is needed for highly demanding systems that requires fast response and high resolution.

In most practical cases, the capacitors are pre-charged from a previous phase. In the worst case, the voltage variation at the amplifier's input would be even larger than expected. Right after the circuit is reconfigured as shown in Fig. 2 based on the capacitor's initial conditions, the amplifier's input voltage is estimated after the capacitors are rearranged. This process can be shown through the following equation and is obtained using charge recombination techniques.

$$V_x(t_{0+}) = \frac{C_1\left(V_i(t_{0+}) - V_{c1}\left(t_0\right)\right) - C_2 V_{c2}\left(t_0\right)}{C_1 + C_2}. \tag{4}$$

$V_{c1}\left(t_0\right)$ and $V_{c2}\left(t_0\right)$ in (4) correspond to the initial conditions in C_1 and C_2, respectively. Equation (4) shows that the initial voltage variation at the inverting terminal of the amplifier, $V_x\left(t_{0+}\right)$, occurs after the connection of the capacitors. According to this equation, large excursions at the amplifier's input will occur when $V_{c1,2}\left(t_0\right)$ and the input voltage $V_i(t_{0+})$ have opposite polarity; this is the worst case for a slew-rate and slew may occur even if $V_i(t_{0+})$ does not exceed $V_{ds,sat}$.

The initial amplifier's input voltage $V_x(t_{0+})$ after the input pulse is applied is returned to its steady state value according to the slope of I_B/C_1 over time, as illustrated in Fig. 3. This constant current condition is maintained until the voltage across the input differential pair reaches the overdrive voltage; then, the amplifier's input stage will operate in a linear regime.

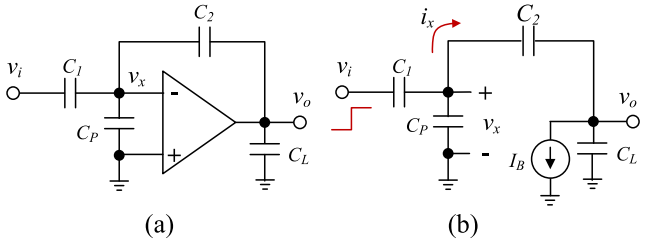


Fig. 4. OTA operation o when slewing in the switched capacitor gain stage by considering the load capacitor.

B. Loaded Switched-Capacitor Circuit

Fig. 4 shows the operation of the amplifier slewing when loaded by C_L; the parasitic capacitor C_P present at amplifier input is also included. The output capacitor C_L is usually pre-charged to a voltage before the charge recombination phase; this charge is a function of the operation of the following stage during the previous clock phase. The initial charge stored in all capacitors determines the instantaneous voltage at the amplifier's input after the capacitors are reconnected; V_x is then computed as

$$V_x\left(t_{0+}\right) = \frac{C_1\left(V_i\left(t_{0+}\right) - V_{c1}\left(t_0\right)\right) - C_P V_{CP}\left(t_0\right)}{C_1 + C_P + \frac{C_2 C_L}{C_2 + C_L}} + \frac{\left(\frac{C_2 C_L}{C_2 + C_L}\right)\left(V_{CL}\left(t_0\right) - V_{c2}\left(t_0\right)\right)}{C_1 + C_P + \frac{C_2 C_L}{C_2 + C_L}}. \tag{5}$$

In (5), $V_{CL}\left(t_0\right)$ represents the initial voltage at C_L, and $V_i\left(t_{0+}\right)$ corresponds to the input voltage right after the input pulse is applied. Usually $V_{CP}\left(t_0\right)$ is small compared with the other terms and can be safely ignored for a sake of simplification in the analysis. It is worth mentioning that the amount of current that discharges $V_x(t_{0+})$ is smaller than the maximum amplifier output current, I_B, since there is a current divider effect due to the presence of C_L. The amplifier's input voltage $V_x\left(t\right)$ returns to its steady state according to:

$$V_x\left(t\right) = V_x\left(t_0\right) - \left(\frac{I_B}{1 + C_L\left(\frac{1}{C_2} + \frac{1}{C_1 + C_P}\right)}\right) \times \left(\frac{t - t_0}{C_1 + C_P}\right) \quad if \;\; \left|V_x\left(t\right)\right| \geq V_{ds_{sat}}. \tag{6}$$

The rate of variation of amplifier's input voltage V_x is then dictated by

$$SR_{Vx} = -\left(\frac{I_B}{1 + C_L\left(\frac{1}{C_2} + \frac{1}{C_1 + C_P}\right)}\right) \cdot \left(\frac{1}{C_1 + C_P}\right). \tag{7}$$

Equation (7) shows the (dis)charging feedback current is a portion of the maximum output current I_B. The slew-rate is determined by the current divider gain between C_L and the series of C_2 and the parallel of C_1 and C_p; the portion of the current flowing through C_2 is then integrated by $C_1 + C_p$ and determines the speed of the variation at node V_x. The larger the load capacitor C_L is, the smaller the slew-rate. In a first

approximation, the slew time is then computed as follows:

$$T_{slew} = \left(V_x\left(t_{0+}\right) - V_{ds\_sat}\right) \times \left(\frac{C_1 + C_P + C_L\left(1 + \frac{C_1+C_P}{C_2}\right)}{I_B}\right). \quad (8)$$

According to (5) and (8), slew time is a function of the capacitor's initial conditions as well as the amplitude of the input signal. The slew-time increases with large capacitors C_L, C_1 and C_P; it also increases when reducing C_2.

To get more insight on the design trade-offs, let us consider the case of a residue amplifier used in a 4.5-bit pipelined stage. For this case, assume that the feedback factor $\beta = \frac{C_2}{C_1+C_2} = 1/16$, amplifier's gain-bandwidth product $GBW = 4.5\ GHz$, $C_1 = 825\,fF$, $C_2 = 55\,fF$, $C_L = 420fF$, Amplifier $DCGain = 43\ dB$, and sampling frequency $F_s = 400\,MHz$. The C_1 and C_2 values were based on the maximum total allowed input referred noise limit to satisfy the thermal noise requirement for the first 4.5-bit pipelined stage in a 12-bit pipelined ADC. The C_L value was based on minimum unit capacitance for satisfying the mismatch requirement, input referred noise, and considering $100\,fF$ parasitic capacitance from sub-ADC in the second 4.5-bit pipelined stage of a 12-bit pipelined ADC. The target is to achieve a settling error under 0.25% in *Ts/2* secs (1.25 nsecs). Fig. 5 displays the amplifier's transient response for three different initial conditions on the load capacitor. According to these results, it is evident that we have to consider the very worst case when computing the required settling time. The 0.25% settling time for each one of these cases is 0.8 nsecs, 1.25 nsecs and 1.75 nsecs, respectively. The worst-case condition takes more than twice the settling time of the best case.

According to equation (8), the slew time can be reduced by increasing V_{ds_sat}; this approach, however, is not advisable since linear settling time will be affected and limitation on voltage headroom. Although the quadratic equation is not accurate for short channel devices, it can help us to get some intuition on the amplifier's design tradeoffs; the transistor's small signal transconductance of a differential pair is approximated as $g_m \approx 2I_B/V_{ds\_sat}$. The larger the saturation voltage, the smaller the transconductance. On the other hand, decreasing further the overdrive voltage of the differential pair has a negative impact on the slew time the since transistor may enter into a subthreshold region, thereby reducing its current driving capability. Optimizing V_{ds_sat} is recommended for best bandwidth and required noise level; usually, a good compromise is to keep its value in a range between 80 mV and 200 mV for the TSMC 40nm technology under 1.1V supply voltage. The proposed design strategy is to make the design procedure independent for the best possible slew rate and faster linear settling.

III. Slew-Rate Boosting Employing an Auxiliary Class-B Amplifier

In high-gain broadband amplifiers, class-AB solutions are desirable to save power. The output stage must be optimized for both small signal performance and high GBW

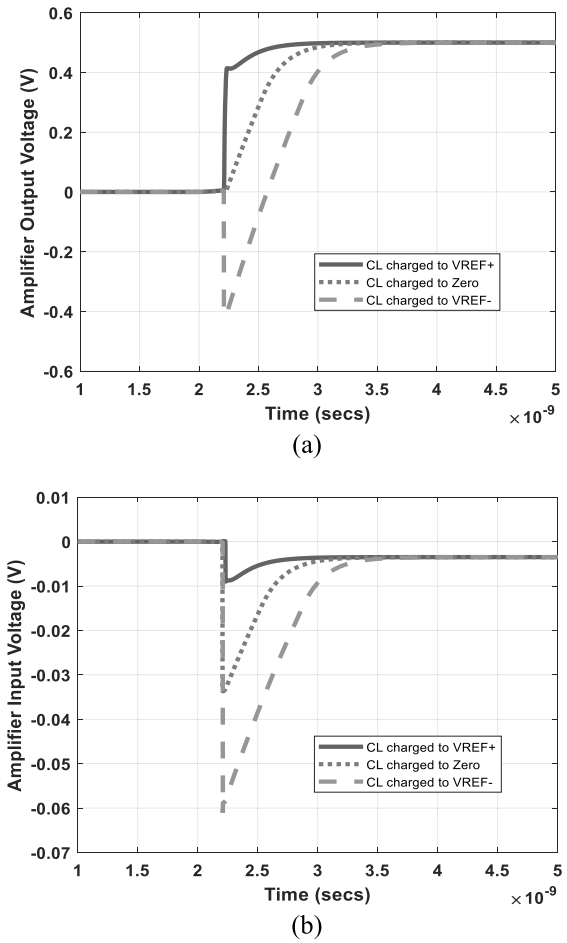


Fig. 5. Different slewing-time of the class-A residue amplifier based on the initial stored-voltage on the load capacitor: (a) differential amplifier input voltage V_x and (b) amplifier's output voltage. The 0.25% settling time for each case is 0.8 nsecs, 1.25 nsecs and 1.75 nsecs, respectively.

for linear settling; this last parameter usually demands significant power consumption that limits the power efficiency of the class-AB topology. Usually the class-AB amplifier suffers from crossover distortion, which limits its linearity and increases its design complexity when minimized. Also, in the two-stage class-AB stage, the first stage must be very fast and must provide high gain at the same time; these two requirements conflict with each other. In the proposed topology, two amplifiers work in parallel where the main amplifier is solely optimized for a linear settling, while the auxiliary two-stage amplifier operates for slew rate boosting. The architecture utilizes a low-power high speed pre-amp in cascade with a class-B stage that allows boosting main amplifier's slew-rate. Unlike the conventional slew-rate boosting that relies on the tail-current, in the proposed topology, the slew rate is based on the injection of a highly dynamic current, which is available on demand from the class-B auxiliary amplifier. Thus, the main amplifier is designed to satisfy the required linear settling and DC gain while the auxiliary amplifier determines architecture's slew rate when driving large voltage variations.

The proposed topology employs a high-speed, low-power pre-amplifier followed by a low-power class-B auxiliary amplifier as displayed in Fig. 6. The class-B amplifier turns on when

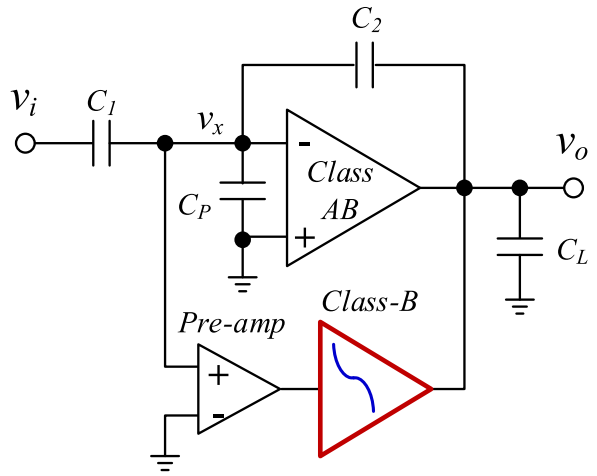


Fig. 6. Simplified schematic of the proposed amplifier aided with an axillary pre-amp followed by a class-B amplifier to boost its overall slew rate.

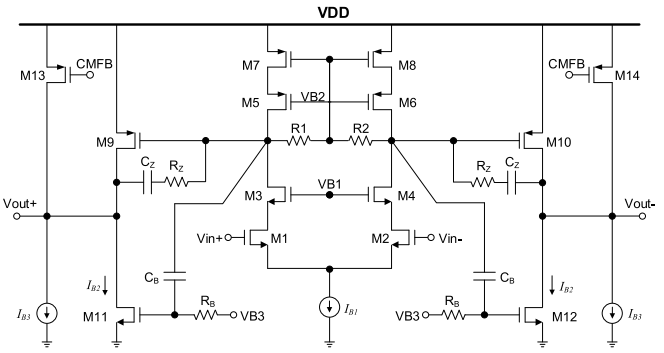


Fig. 7. The low-power, high-performance pseudo class-AB architecture utilized as the main amplifier in the proposed topology in the multi-bit/stage pipelined ADC.

TABLE II
AMPLIFIER DEVICE SIZES

Transistor	W/L (μm/μm)	Drain Current (μA)
M1-M2	20/0.08	750
M3-M4	15/0.12	750
M5-M6	30/0.08	750
M7-M8	30/0.12	750
M9-M10	16/0.06	400
M11-M12	8/0.06	400

Component	Value
R_B	20 kΩ
C_B	200 fF
R_Z	400 Ω
C_Z	100 fF

the main amplifier's input voltage exceeds a 16 mV differential signal swing. When activated, the class-AB amplifier delivers most of the current demanded by the load and feedback capacitor. When the amplifier's input voltage is reduced, the class-B amplifier is less effective, and the linear settling is dominated by the action of the primary amplifier. The auxiliary circuit is OFF when processing small signals. Thus, the AC response of the overall circuit would be almost the same as the one of the main amplifier; some small parasitics are the difference. Linear settling behavior of the overall circuit would be same as linear settling behavior of the main amplifier.

The primary amplifier consists of the cascade of a class-A pre-amp and a class-AB output stage. The main amplifier is optimized for linear settling by satisfying the minimum required DC gain and small signal transconductance while the class-B amplifier shows a large current capability when activated.

A. Main Amplifier

A two-stage pseudo class AB (class A cascaded with class AB) amplifier was chosen as the main amplifier as shown in Fig. 7. The first stage, composed by transistors M1–M8, achieves high gain due to the cascode nature of its components. Resistors R1 and R2 are used to set the bias point without the need of a CMFB circuit. The first stage is DC connected to the P-type outage (transistors M9 and M10) and the AC is also coupled to the N-type amplifier realized through transistors M11 and M12. The AC connection through CB boost the high frequency AC transconductance by 6 dB. This high-frequency signal path enables the architecture to operate as a true class AB amplifier with the ability to sink and deliver large amounts of output current improving its slew-rate. Transistors M11 and M12 are biased through the resistor RB and VB3. The net AC effect of CB, RB, M11, and M12 working together is to increase the small signal transconductance at medium and high frequencies.

The amplifier's targeted specifications are: DC gain > 48 dB (which correspond to gain error $1=1/2^8$), GBW > 3.5 GHz and a 0.25% settling time under 1.8 nsecs. The transconductance requirement can be satisfied by delivering enough current at the input transistors small signal behavior such as DC gain and GBW. The minimum required GBW for the amplifier is achieved employing 1.5 mA at the tail current in the first stage. The output stage of the main amplifier consists just two transistors to provide maximum swing. Then, a small dc-current (0.5 mA) is set as the output stage current to provide enough small signal transconductance since the output resistance of the first stage is high. Then, Miller compensation through Cz and Rz is used. Thus, the dominant pole is placed at the output node of the amplifier's first stage. An external resistor is used for the generation of the reference DC current, and weighted current mirrors are employed to generate the bias current needed in each stage. Table II shows the amplifier device sizes including dimensions and bias conditions for the relevant transistors and component values. Total power consumption is 2.75 mW. Simulated results show that 0.25% settling time is under 1.8 nsecs, while the DC gain is over 49 dB.

B. Slew-Rate Booster

The proposed slew rate boosting auxiliary circuit employs simple circuitry to detect the need for injecting high-dynamic current at the output load by implementing a pre-amp followed

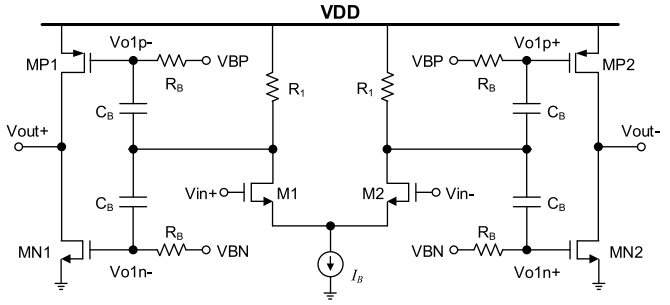


Fig. 8. The proposed auxiliary circuit for boosting main amplifier's slew rate.

TABLE III
SLEW-RATE BOOSTER DEVICE SIZES

Transistor	W/L (μm/μm)	Drain Current (μA)
M1-M2	5/0.08	200
MN1-MN2	20/0.06	50
MP1-MP2	40/0.06	50

Component	Value
R_1	2.25 kΩ
C_B	500 fF
R_B	20 kΩ
I_{drain} (MN1, MP1)	0.15mA

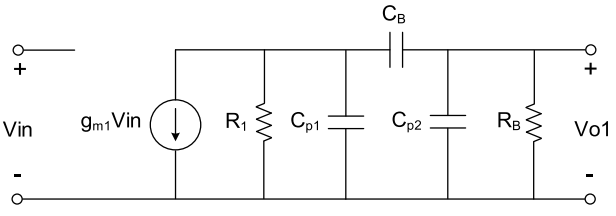


Fig. 9. Small-signal model of the pre-amplifier and coupling network including C_B and R_B.

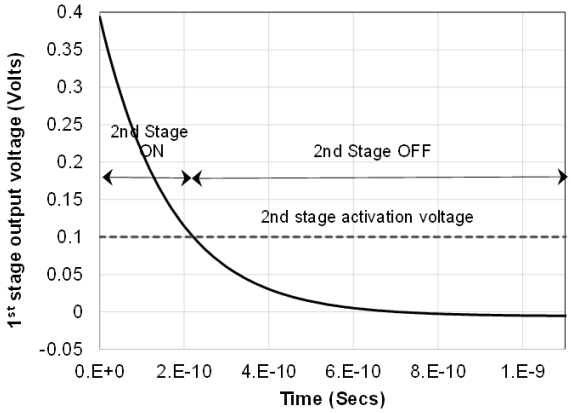


Fig. 10. Impulse response of a 2nd order amplifier (eqn. 11) showing the activation voltage for the amplifier's second stage (dashed line).

by a class-AB amplifier. The simplified schematic is shown in the Fig. 8. The high-speed pre-amp amplifies the error signal present at the input of the main amplifier and then increases the sensitivity of the class-B output stage (MN1-MN2 and MP1-MP2). The class-B output stage operates in a subthreshold region to reduce power consumption; it also enables slew-rate booster circuit operation with a defined hysteresis around 16 mV. For that purpose, VBN and VBP voltages are properly set. The transistors are computed such that MP1, MP2, MN1, and MN2, can provide up to five times of the main amplifier output current in the slew mode and in the presence of large signals. Although the disadvantage of the class-B amplifiers is the cross-over distortion, our proposed technique does not suffer from this effect because the proposed class-B amplifier is activated if and only if the signal swing at the input of the main amplifier exceeds 16 mV, and that happen when the signal is large; this stage remains OFF during small signal operation.

The tail current of the pre-amp in the slew-rate booster is 0.4 mA; this current is smaller than the 1.5 mA tail current of the main amplifier's first stage. The in-band gain of the front-end amplifier is 8 V/V, and the $-$ 3dB bandwidth is as high as 1 GHz. Also, the input capacitance of the pre-amp is around 15 fF, which is small compared to the 65 fF of the input capacitance of the main amplifier. This additional capacitance does not have a major effect on either the loop gain or the amplifier's settling time. Table III displays the device sizes including dimensions and bias conditions for the relevant transistors and component values. The overhead power consumption is 0.55 mW after utilizing this auxiliary circuit, which is only 20% of the main amplifier power consumption.

The small signal model of the preamplifier and coupling network to the class-B output stage (see Fig. 8) used in the proposed slew-rate booster circuit is shown in the Fig. 9. The transfer function would be derived as

$$H(s) = gm_1 \times \frac{R_1 R_B C_B s}{\begin{array}{l}[(R_1 R_B C_{p1} C_{p2} + R_1 R_B C_B (C_{p1} + C_{p2}))]s^2 \cdot \\ +[R_1 C_{p1} + R_B C_{p2} + (R_1 + R_B) C_B]s + 1\end{array}} \tag{9}$$

In (9), C_{p1} and C_{p2} are the parasitic capacitances at the drain of the M1 and gate of the MP1/MN1, respectively. Since the parasitic capacitances are much smaller than C_B, equation (9) can be simplified as

$$H(s) = \frac{gm_1 R_1 R_B C_B s}{(1 + \frac{s}{\omega_{P1}})(1 + \frac{s}{\omega_{P2}})} \tag{10}$$

where $\omega_{P1} \cong \frac{1}{R_B C_B}$ and $\omega_{P2} \cong \frac{1}{R_1 (C_{p1} + C_{p2})}$. The dominant pole ω_{p1} is placed at low frequency, while the non-dominant pole ω_{P2} is placed at the highest possible frequency. At intermediate frequencies, the voltage gain is flat and dominated by $gm_1 R_1$ if $R_B \gg R_1$. Although the small signal analysis is interesting, it is not very useful since this circuit is not active for small signals. More interesting is the large signal analysis of its impulse and pulse response.

It can be shown that when enabled, the unity impulse response of the 2nd order function represented by (10), follows

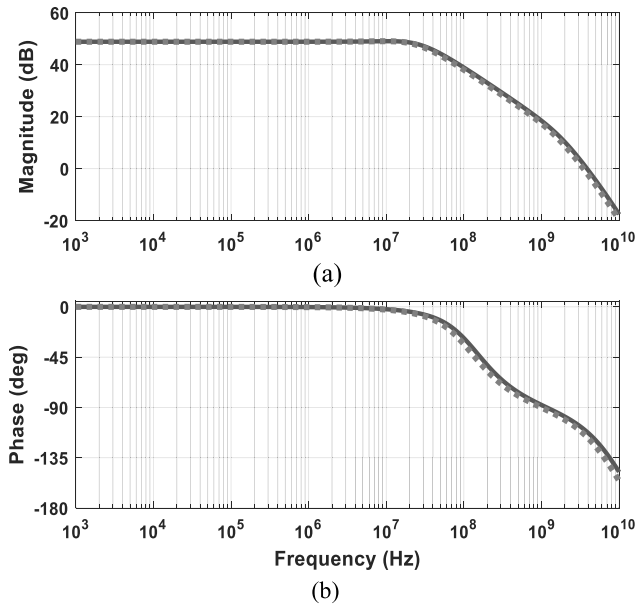


Fig. 11. Main amplifier's (solid line) and the main amplifier's with SR boosting (dotted line) frequency response: (a) magnitude and (b) phase.

the behavior determined by

$$v_{o1}(t) \cong (v_{o1}|_{t=0}) \left(e^{-\omega_{P2} t} - \left(\frac{\omega_{P1}}{\omega_{P2}} \right) e^{-\omega_{P1} t} \right) \qquad (11)$$

Significant slow components may result from this circuit unless $\omega_{P2} \gg \omega_{P1}$. For this case, ω_{P1} is set at 100 Mrad/sec while ω_{P2} is set around 6 Grad/sec. Thus, the peak value of the slow component is 60 times smaller than the component lumped to the fast exponential component in equation (11). This equation is plot in Fig. 10; the dash line shows the activation voltage set at 100 mV for the class B (second-stage) amplifier, which correspond to a threshold voltage of around 16 mV at first amplifier input. The first part of the transient is dominated by the term $e^{-\omega_{P2} t}$; after 1% settling time, the behavior is dominated by the slow component $e^{-\omega_{P1} t}$. Notice in this figure that the slow settling component does not play a major role on the operation of the class-B amplifier; even 10% settling is enough for the proper functionality of the architecture. The speed of the overall circuit is dominated by the fast exponential component. Fig. 11 shows the main amplifier's frequency response versus the main amplifier with SR boosting frequency response. Since the auxiliary circuit is OFF when processing small signals, the AC response of the overall circuit would be almost the same as the one of the main amplifier; some small parasitics are the difference.

Fig. 12 shows the differential output current (from Cadence) versus the input voltage for both the main amplifier and the auxiliary amplifier. The auxiliary amplifier is turned OFF when the main amplifier's input voltage is less than 16 mV. For small signal variations, the slew phase is not critical; hence, the final settling time is determined by the parameters of the main amplifier. When the input step voltage exceeds the threshold voltage, the auxiliary amplifier delivers a high dynamic current—more than triple of main amplifier's output

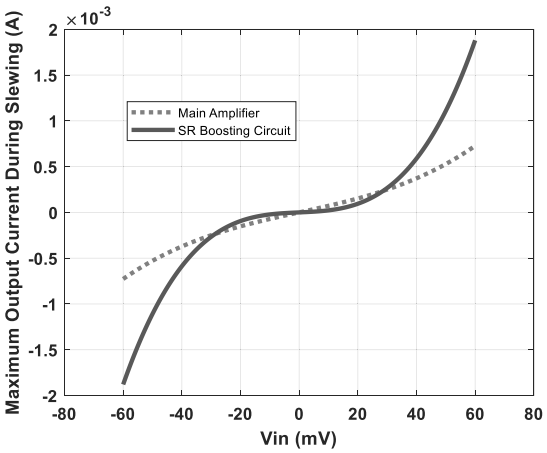


Fig. 12. Differential output current versus the input voltage for both the main amplifier (dotted line) and the auxiliary amplifier (solid line); cadence results.

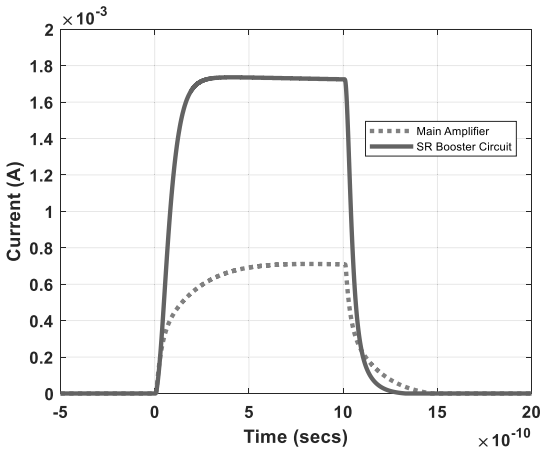


Fig. 13. Pulse response current of the main amplifier (dotted line) and slew-rate booster circuit (solid line): output current.

current and over 10 times greater than class-B amplifier bias current.

To compare the current capability of the current booster, a differential narrow input pulse with 1 nsec width and 60 mV amplitude was used. For this simulation, amplifier's output was connected to a small resistor to measure the time delay and amount of current delivered by the amplifier components. Fig. 13 shows the results. The auxiliary class-B amplifier takes less 300 psecs delay to deliver/sink more than 1.7 mA and takes around 700 psecs for 1% settling; main amplifier delivers around 0.7 mA and settles (1%) in around 1500 psecs.

To verify the circuit behavior under a practical case, a 4.5-bit stage used in pipelined ADCs was used as a testbed; the very small feedback factor $\beta = 1/16$ [30]. The input capacitance ($C_1 = 16C_2$ in Fig. 6) was set at 880 fF while the feedback capacitor was set at $C_2 = 55$ fF; capacitive amplification factor is 16. The capacitors were fully discharged, and the input signal was pulsed from zero to 62.5 mV. Fig. 14 shows the differential output current when the auxiliary amplifier is enabled and for the case of the standalone amplifier. The peak current of the enhanced architecture surpasses the

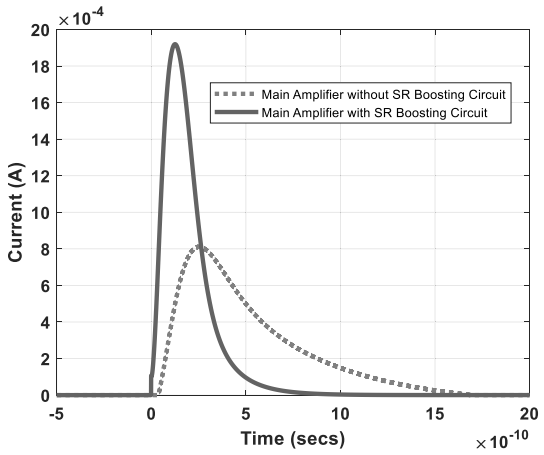


Fig. 14. Differential output current for the standalone amplifier (dotted line) and for the main amplifier with auxiliary amplifier enabled (solid line).

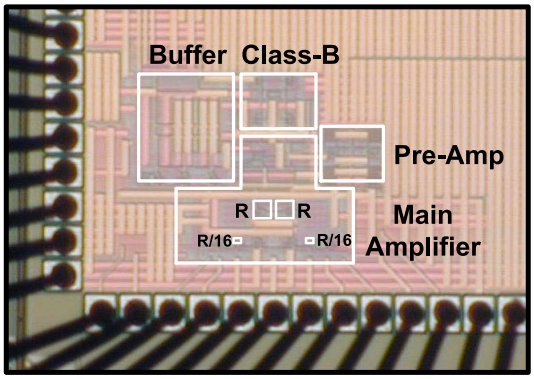


Fig. 15. Chip micrograph.

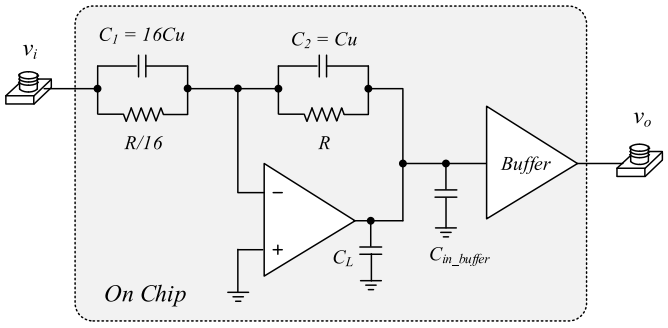


Fig. 16. Simplified (single-ended) version of the amplifier characterization setup used to measure the performance of the slew-rate boosting technique.

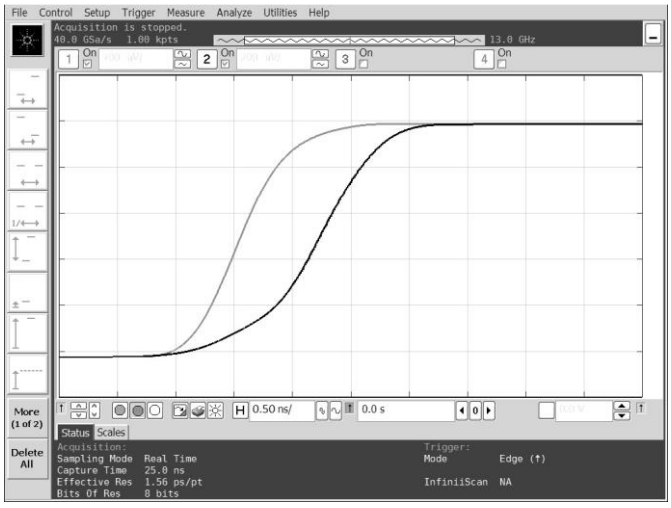


Fig. 17. Measurement results of a large input step voltage for the pseudo class-AB amplifier with SR boosted technique and the conventional pseudo class-AB amplifier in the prototype of a 4.5-bit/stage pipelined ADC.

one of the conventional one by a factor of 240%. For the proposed architecture, the current's peak value is reached in 180 psecs compared to 380 psecs when the main amplifier was operating alone. The superior performance of the proposed amplifier is more evident if we consider the slew time for the capacitive amplifier: 400 psecs for the proposed amplifier with slew boosting technique vs. 1050 psecs required for the conventional architecture.

IV. Experimental Results

The amplifier along with the slew-rate boosting auxiliary circuit was fabricated in the TSMC 40 nm CMOS process using core devices with a nominal value of 1.1 V. Fig. 15 shows the die photo of the amplifier along with the slew-rate boosting auxiliary circuit, where the core occupies 0.05 mm^2. The single-ended test setup used to characterize the performance of the amplifiers in the 4.5-bit/stage pipelined stage prototype is shown in Fig. 16. The actual chip is fully differential. An Agilent E8267D PSG vector signal generator was used to supply the input signal and the output was captured using the Agilent Infiniium DSA91304A oscilloscope. To preserve the high output impedance of the amplifiers and set the DC value at the amplifier's input, R was set to be 5 $M\Omega$. As for C_1 and C_2 they were set to 880 fF and 55 fF, respectively, to resemble the operation of a capacitive amplifier of 16 V/V. The capacitor values were based on the maximum total allowed input referred noise limit to satisfy the thermal noise requirement for the first 4.5-bit pipelined stage for a 12-bit pipelined ADC. The load impedance from the bond wire, pads, and equipment was driven by an extra buffer placed at the output of the gain stage. The buffer's input capacitance is around 180 fF, which introduces an additional load to the gain stage amplifiers.

A 62.5 mVpp input step voltage was applied to generate a 1Vpp output step variation. The measured output waveform results were compared to the amplifier without the slew-rate booster in Fig. 17. The proposed architecture shows a 0.8 nsecs shorter slew time (45% smaller than the amplifier without SR boosting) and 0.7 nsecs shorter 1% settling time, which is 28% smaller than the conventional solution. These results include the effect of the on-chip buffer, bondwire inductance and input impedance of the test equipment; 1% settling time is around 1.8 nsecs but simulation results show that standalone amplifier's 1% settling time is around 1 nsec.

The linearity of the ×16 capacitive amplifier was characterized as well. Fig. 18 shows the output harmonic components for both circuits with a 500 MHz input signal and

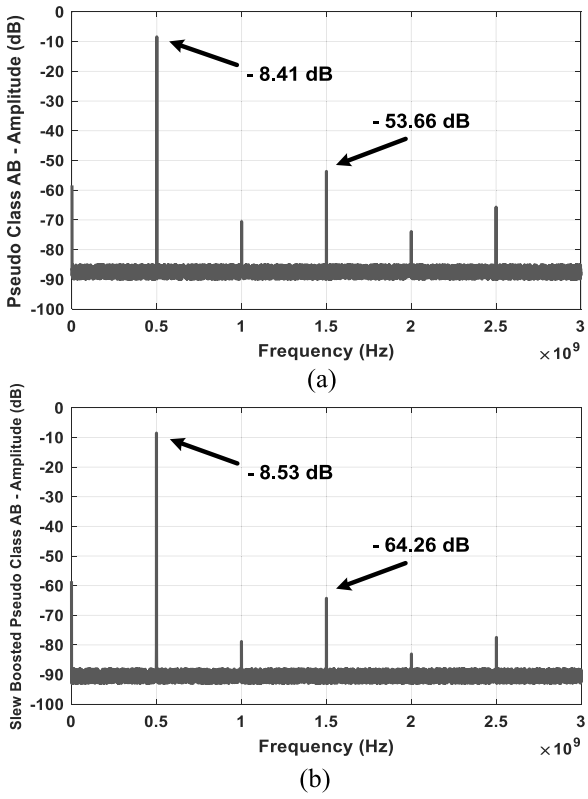


Fig. 18. Measured spectrums for a 500 MHz tone for a) an amplifier and b) an amplifier with the SR boosting SR technique enabled.

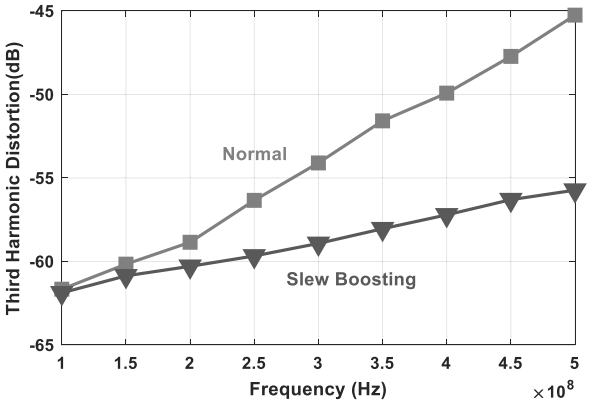


Fig. 19. Third harmonic distortion comparison of class-AB amplifier with and without SR boosting technique.

62.5 mVpp amplitude. High frequency large signals demand a larger amplifier slew-rate to follow the fast signal variations. According to these results, the proposed architecture surpasses the linearity of the conventional amplifier by more than 10 dB. The linearity of both amplifiers was compared for different frequencies in the range of 100 MHz to 500 MHz. The results are plotted in Fig. 19. The third harmonic distortion of the two amplifiers is similar for low frequency conditions since signal variation is not very slew demanding. Table IV compares the measured results for the class-AB amplifier with and without boosted SR technique. For the same loading and same core amplifier, the proposed architecture shows an improvement of 100% in slew-rate and a reduction of 28% in the 1% settling time. The proposed architecture's HD3 is maintained under − 48 dB (8 bits resolution) up to 780 MHz, while the conventional amplifier can only operate properly until 400 MHz. The cost of these benefits represents an increase in power consumption of 20% and a 1 dB increase in noise level.

TABLE IV
COMPARISON OF EXPERIMENTAL RESULTS

Parameter	[24]	Pseudo Class-AB Amplifier	Pseudo Class-AB Amplifier with SR Boosting
Technology	0.18 µm CMOS	TSMC 40 nm	TSMC 40 nm
Supply Voltage	1.8	1.1 V	1.1 V
Static Current	0.194 mA	2.5 mA	3 mA
DC Gain	60 dB	49 dB	49 dB
Small signal GBW	160 MHz	3.6 GHz	3.6 GHz
Open Loop PM*	75 degrees	65 degrees	65 degrees
Capacitive Load	1750 fF	500 fF	500 fF
Slew Rate (average)	26.7 [V/µs]	625 [V/µs]	1250 [V/µs]
Input Referred Noise* (1Hz – 250 MHz)	N/A	36.2 µVrms	40.8 µVrms
1% Settling Time	≅ 100 ns	2.5 ns	1.8 ns
HD3 (Fin = 500 MHz) Vout = $1V_{pk\text{-}pk}$	N/A	− 45.25 dB	− 55.73 dB
Max Frequency Providing the 8-bit Output Linearity	≅ 40 MHz	400 MHz	780 MHz
FoM ((V/µs)pF/mA)	137.6	125	208.33

V. CONCLUSIONS

A new technique for slew-rate boosting based on high injection of the dynamic current only when the high slew-rate is demanded is proposed in this paper. The proposed technique makes use of a high-speed pre-amp followed by a class-B auxiliary amplifier that delivers high output current only when high slew-rate is demanded when large input signals arise.

The proposed technique is suitable for high-speed, low-supply voltage low-power multi-bit/stage pipelined ADC applications. Measurement results for the proposed architecture demonstrate that the proposed scheme shortens by 28% the amplifier's 1% settling time. Also, utilizing this technique provided more than 10 dB better linearity for a 500 MHz input signal, while only a 20% power consumption overhead is reported due to the extra circuitry.

ACKNOWLEDGMENTS

The authors would acknowledge TSMC for chip fabrication and Eric Soenen and Martin Kinyua for fruitful discussions.

REFERENCES

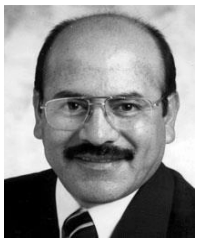
[1] S. Woo and J.-K. Cho, "A switched-capacitor filter with reduced sensitivity to reference noise for audio-band sigma-delta D/A converters," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 4, pp. 361–365, Apr. 2016.

[2] Y. Xu and P. R. Kinget, "A switched-capacitor RF front end with embedded programmable high-order filtering," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1154–1167, May 2016.
[3] L. Kull *et al.*, "A 10 b 1.5 GS/s pipelined-SAR ADC with background second-stage common-mode regulation and offset calibration in 14 nm CMOS FinFET," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2017, pp. 474–475.
[4] H. Mo and M. P. Kennedy, "Masked dithering of MASH digital delta-sigma modulators with constant inputs using multiple linear feedback shift registers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 6, pp. 1390–1399, Jun. 2017.
[5] P. Payandehnia *et al.*, "A 0.49–13.3 MHz tunable fourth-order LPF with complex poles achieving 28.7 dBm OIP3," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 8, pp. 2353–2364, Aug. 2018.
[6] E. Bonizzoni, A. Patra, and F. Maloberti, "Two-path quadrature cascaded band-pass sigma-delta modulators," in *Proc. 26th Int. Conf. VLSI Design 12th Int. Conf. Embedded Syst.*, Pune, MA, USA, Jan. 2013, pp. 221–226.
[7] X. Meng, Y. Zhang, T. He, P. Payandehnia, and G. C. Temes, "A noise-coupled time-interleaved delta-sigma modulator with shifted loop delays," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Lisbon, Portugal, May 2015, pp. 2045–2048.
[8] S. Moallemi and A. Jannesari, "The design of reconfigurable delta-sigma modulator for software defined radio applications," in *Proc. IEEE Int. Conf. Circuits Syst. (ICCAS)*, Kuala Lumpur, Malaysia, Oct. 2012, pp. 254–257.
[9] H. Ghaedrahmati and J. Zhou, "160 MS/s 20 MHz bandwidth third-order noise shaping SAR ADC," *Electron. Lett.*, vol. 54, no. 3, pp. 128–130, 2018.
[10] P. Mahmoudidaryan and A. Medi, "Codesign of Ka-band integrated limiter and low noise amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 9, pp. 2843–2852, Sep. 2016.
[11] B. W. Lee and B. J. Sheu, "A high slew-rate CMOS amplifier for analog signal processing," *IEEE J. Solid-State Circuits*, vol. 25, no. 3, pp. 885–889, Jun. 1990.
[12] K. N. Leung and P. K. T. Mok, "Nested Miller compensation in low-power CMOS design," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 48, no. 4, pp. 388–394, Apr. 2001.
[13] R. Nguyen and B. Murmann, "The design of fast-settling three-stage amplifiers using the open-loop damping factor as a design parameter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 6, pp. 1244–1254, Jun. 2010.
[14] S. Seth and B. Murmann, "Settling time and noise optimization of a three-stage operational transconductance amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 5, pp. 1168–1174, May 2013.
[15] S. Moallemi and A. Jannesari, "A new architecture for two-stage OTA with no-Miller capacitor compensation," in *Proc. IEEE Int. Conf. Circuits Syst. (ICCAS)*, Kuala Lumpur, Malaysia, Oct. 2012, pp. 180–183.
[16] J. Adut, J. Silva-Martinez, and M. Rocha-Perez, "A 10.7-MHz sixth-order SC ladder filter in 0.35-μm CMOS technology," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 53, no. 8, pp. 1625–1635, Aug. 2006.
[17] R. S. Assaad and J. Silva-Martinez, "The recycling folded cascode: A general enhancement of the folded cascode amplifier," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2535–2542, Sep. 2009.
[18] A. K. Dubey, R. K. Nagaria, P. K. Pal, and R. K. Singh, "Enhanced slew rate, constant-g_m rail-to-rail OpAmp using 1:2 current mirror biasing technique," in *Proc. Int. Conf. Comput., Commun. Automat. (ICCCA)*, Noida, Uttar Pradesh, Apr. 2016, pp. 1612–1618.
[19] K. H. Mak and K. N. Leung, "A signal- and transient-current boosting amplifier for large capacitive load applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 10, pp. 2777–2785, Oct. 2014.
[20] H. Lee and P. K. T. Mok, "A CMOS current-mirror amplifier with compact slew rate enhancement circuit for large capacitive load applications," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Sydney, NSW, Australia, vol. 1, May 2001, pp. 220–223.
[21] S. S. Chong and P. K. Chan, "Cross feedforward cascode compensation for low-power three-stage amplifier with large capacitive load," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2227–2234, Sep. 2012.
[22] S. Bu, H. W. Tse, K. N. Leung, J. Guo, and M. Ho, "Gain and slew rate enhancement for amplifiers through current starving and feeding," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Lisbon, Portugal, May 2015, pp. 2073–2076.
[23] J. Xu, M. Zhao, X. Wu, and X. Yan, "Low voltage low power current mirror OTA for sigma-delta modulator," in *Proc. IEEE Conf. Electron Devices Solid-State Circuits (EDSSC)*, Tainan, Taiwan, Dec. 2007, pp. 875–879.
[24] A. P. Perez, Y. B. N. Kumar, E. Bonizzoni, and F. Maloberti, "Slew-rate and gain enhancement in two stage operational amplifiers," in *Proc. IEEE Int. Symp. Circuits Syst.*, Taipei, Taiwan, May 2009, pp. 2485–2488.
[25] M. Rezaei, E. Zhian-Tabasy, and S. J. Ashtiani, "Slew rate enhancement method for folded-cascode amplifiers," *Electron. Lett.*, vol. 44, no. 21, pp. 1226–1228, Oct. 2008.
[26] J. Silva-Martinez, J. Adut, and M. Rocha-Perez, "A 58 dB SNR 6th order broadband 10.7 MHz SC ladder filter," in *Proc. IEEE Custom Integr. Circuits Conf.*, Oct. 2003, pp. 13–16.
[27] K. Honda, M. Furuta, and S. Kawahito, "A 1 V 10 b 125 MSample/s A/D converter using cascade amp-sharing and capacitance coupling techniues," in *Proc. IEEE Int. Symp. Circuits Syst.*, Kos, Greece, May 2006, pp. 1031–1034.
[28] J. K.-R. Kim and B. Murmann, "A 12-b, 30-MS/s, 2.95-mW pipelined ADC using single-stage class-AB amplifiers and deterministic background calibration," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2141–2151, Sep. 2012.
[29] H. Venkatram, T. Oh, K. Sobue, K. Hamashita, and U.-K. Moon, "A 48 fJ/CS, 74 dB SNDR, 87 dB SFDR, 85 dB THD, 30 MS/s pipelined ADC using hybrid dynamic amplifier," in *Symp. VLSI Circuits Dig. Tech. Papers*, Honolulu, HI, USA, Jun. 2014, pp. 1–2.
[30] M. H. Naderi and J. Silva-Martinez, "Algorithmic-pipelined ADC with a modified residue curve for better linearity," in *Proc. IEEE 60th Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Boston, MA, USA, Aug. 2017, pp. 1446–1449.

Mohammad H. Naderi (S'09) received the B.Sc. and M.Sc. degrees in electrical engineering, circuit and systems electronics from the University of Tehran, Iran, in 2008 and 2011, respectively. He is currently pursuing the Ph.D. degree with Texas A&M University. In 2014, he was an IC Design Intern with Qualcomm Corporation, San Diego, CA, USA, involved in data converters. He currently holds a granted U.S. patent on error-feedback digital-to-analog converter (DAC). He was a recipient of Texas Instruments and Broadcom Fellowships.

He is currently a Senior IC Design Engineer with Qualcomm Corporation involved in 5G and IoT projects. His research interests include analog/mixed signal integrated circuits, data converters ($\Sigma\Delta$, Pipeline, SAR, and DAC), data processing, and VCOs.

Suraj Prakash (S'15) received the B.Sc. degree in electrical engineering from IIT Roorkee, Roorkee, India. He is currently pursuing the Ph.D. degree with Texas A&M University since 2012. He was a Senior IC Design Engineer with STMicroelectronics for around five years. He was an Intern with Cirrus Logic during Summer 2013. He was also with Qualcomm Technologies during Summer 2017 and Spring 2018. He currently holds two granted patents from USPTO. His research interests include data converters, RF power amplifier, and its supply modulator. He was a recipient of the Cirrus' Hackworth Fellowship and departmental scholarships.



Jose Silva-Martinez (SM'98–F'10) was born in Tecamachalco, México. He received the M.Sc. degree from INAOE, Puebla, in 1981, and the Ph.D. degree from Katholieke Univesiteit Leuven, Leuven, Belgium, in 1992.

In 1993, he joined the Electronics Department, INAOE, where he was the Head of the Electronics Department from 1995 to 1998. He was a co-founder of the Ph.D. Program on electronics in 1993. He is currently a Texas Instruments Professor with the Department of Electrical and Computer Engineering, Texas A&M University, College Station. He has published over 125 and 170 journal and conference papers, respectively, three books and 14 book chapters, three granted patents, and five more filed. His current field of research is in the design and fabrication of integrated circuits for communication, radar, and biomedical applications.

Dr. Silva-MartinezDr. Silva-Martinez served as a member of the CASS Distinguish Lecture Program from 2013 to 2014 and a Senior Editorial Board Member of the IEEE JETCAS from 2014 to 2015. He is a member of the Board of Governors of the IEEE-CASS, from 2017 to 2019. He was a recipient of the 1990 IEEE European Solid-State Circuits Conference Best Paper Award. He was a recipient of the 2005 Outstanding Professor Award by the ECE Department, Texas A&M University, co-author of the papers that received the MWCAS 2011 and RF-IC 2003 Best Student Paper Awards, and co-advised in testing techniques the Ph.D. student who was a recipient of the 2005 Best Doctoral Thesis Award, presented by the IEEE Test Technology Technical Council, IEEE Computer Society. He served as the Conference Chair of MWCAS-2014. He has served as the IEEE CASS Vice President Region-9 from 1997 to 1998. He has served as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS part-II from 1997 to 1998 and from 2002 to 2003 and an Associate Editor for the IEEE TCAS Part-I from 2004 to 2005 and from 2007 to 2008. He served as the Editor in Chief of the IEEE TCAS Part-II from 2014 to 2015. He currently serves on the board of editors of other three major journals.