<https://developer.arm.com/documentation/102202/0300/Overview?lang=en>

CISCO Interview questions

Write a constraints for 4k address space, 5% in lower 1k, 5% in upper 1k.

Write a virtual task so these signals can be transferred from Driver to DUT via interface

Memory\_seq\_item:

rand bit[7:0] addr;

rand bit wr\_en;

rand bit rd\_en;

rand bit [31:0] wr\_data;

bit [31:0] rd\_data, clk, reset;

Code a virtual task drive () with req, `DRIVE\_IF.(This is a driver class)

What are the signals of channel from which I would like to transfer this data “Increment burst type, 3 transfers, 4 byte per transfer, start at addr 0”

Now write the values of signal burst\_type, awsize and awlen for above mentioned question

====================Generic which I found from internet================================

✅**AMBA AHB Protocol**1.Provide an overview of the AMBA AHB protocol and its key features.

2. How does the AHB protocol differ from other bus protocols, and what advantages does it offer?  
3. Explain the concept of master and slave devices in the AHB protocol and how they interact.  
4. Describe the AHB bus architecture and the role of the different channels (data, address, control) in the protocol.  
5. How do you handle bus arbitration in a multi-master AHB system, and what factors influence your arbitration decisions?  
6. Discuss your experience with designing and implementing AHB interfaces for various peripherals.  
7. Explain the significance of burst transfers in the AHB protocol and when they are beneficial.  
8. How do you ensure data coherency and ordering in AHB transactions?  
9. Can you provide an example of a situation where you had to optimize AHB transactions for better system performance?  
10. Discuss your approach to handling errors and ensuring robustness in AHB-based systems.  
  
✅AXI Interview Questions   
  
1. Provide an overview of the AMBA AXI protocol and its key features.  
2. How does the AXI protocol differ from other AMBA protocols like AHB and APB?  
3. Explain the concept of channels in the AXI protocol and their respective roles.  
4. Describe the AXI read and write transactions, including the signals involved in each.  
5. How do you handle burst transfers in AXI, and when is it advantageous to use them?  
6. Discuss the importance of handshaking signals in AXI transactions and how they contribute to reliable communication.  
7. Explain the concept of AXI IDs and how they are utilized in a multi-master system.  
8. Can you elaborate on the different AXI protection levels and when to apply them?  
9. Discuss your experience with addressing latency and throughput concerns in AXI-based designs.  
10. How do you ensure data coherency in a multi-master AXI system, and what strategies do you use to avoid potential conflicts?

1. [What are the key features of AXI protocol?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
2. [Explain AXI architecture. What are the different channels as per AXI protocol?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
3. [Does AXI support existing AHB and APB interface?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
4. [Advantages of AXI over AHB protocol?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
5. [What do you mean by multiple outstanding transactions? why is it useful?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
6. [Why read has only 2 channels?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
7. [What is the minimum and maximum data bus width supported in AXI?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
8. [Why is write data channel treated as buffered?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
9. [Which channels are exclusive to the slave?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
10. [As per AXI terminology differentiate between beat, burst and transaction?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
11. [Can a master can give WLAST in middle of a burst transfer?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
12. [What is easy addition of register stages to provide timing closure?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
13. [What is an interconnect?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
14. [What is control information?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
15. [What are the major actions done by interconnect?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
16. [Topologies using Interconnect?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
17. [what is meant by high latency?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
18. [which component is responsible for calculating subsequent transfers in a burst?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
19. [Difference between Channel and Bus ? If they are same then why two different names?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
20. [What is need of interleaving?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
21. [What is the meaning of point to point interconnect?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
22. [Is there any chance is getting the same ID with different master?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
23. [What does AXLEN and AXSIZE represents?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
24. [Mention the LOW POWER INTERFACE SIGNALS supported by AXI3 AXI4 protocols?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
25. [What is the purpose of byte lane strobe ? Is strobe used for both read and write operation?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
26. [What's the purpose of LAST signal during a transaction? Does both read and write operation use it? If yes, which channel is used to send this signal?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
27. [Explain the basic handshaking mechanism in AXI.](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
28. [Does VALID and READY signal have dependencies on each other?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
29. [When should the VALID signal go high and low?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
30. [When must the slave give write response?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
31. [What is deadlock condition?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
32. [Why there was no write response for each beat in burst Write. But there is a separate read response for each beat in a read burst?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
33. [How to ensure data integrity on AXI?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
34. [Is there a possibility that A Read transaction can complete in One Cycle?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
35. [What will happen if last is not asserted after completion of the transfer?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
36. [In AXI we have any time-out condition w.r.t channel handshake.](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
37. [What is 4KB address boundary in AXI?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
38. [Importance of RRESP and BRESP?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
39. [Types of responses?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
40. [If master is sending a address but none of the slave is having that address. So which response will you get?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
41. [With respect to the assertion of valid and ready signals, which order of assertion provides most efficient handshaking?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
42. [Why the specification recommends default state of AWREADY as High?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
43. [RVALID to be asserted before ARVALID? Explain if the statement is right or not?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
44. [The address phase is followed by the data transfer phase.So why a master must not wait for AWREADY to be asserted before driving WVALID?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
45. [What are the rules governing the use of bursts as per AXI protocol?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
46. [What's the significance of AxBURST signal? What's the different burst types supported in AXI?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
47. [For a read transaction if the Slave generates an error response midway of the transaction, will the remaining transfers of the burst cancelled?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
48. [Who usually generates decode error?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
49. [How to proceed with the further transfers if the Start Address issued by the MASTER is UNALIGNED?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
50. [What happens in the case of WRAP BURST if FIRST ADDRESS is higher than the wrap boundary.](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
51. [What happens when unalinged addr is given for wrap brust type?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
52. [Should valid and ready be deasserted after a every successful handshaking is done.if yes,why?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
53. [Which type of burst supports cache line access?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
54. [Where we can use INCR And Fixed burst?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
55. [What is max bytes which can be transfer in a single burst?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
56. [What is restriction on size of any transfer?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
57. [What is upper byte lane and lower byte lane?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
58. [AXLEN = 4 then burst length?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
59. [AXI supports for burst length for the incr burst type is 1-256 bytes and for fixed, wrap is 1-16 bytes.(True/False)](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
60. [How the address is defined as Aligned or unaligned?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
61. [Is 0110 strobe is valid?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
62. [If the AXI Bus is wider than the burst size then how the transfer is done? What's a narrow transfer and how is it performed?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
63. [What is the value of WSTRB when WVALID is LOW?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
64. [What is WRAP and How to Calculate Address in WRAP Burst?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
65. [What do you understand by outstanding transactions?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
66. [What does high initial latency devices mean?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
67. [What is a byte strobe?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
68. [What is an out of order response?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
69. [Can we generate address information from slave?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
70. [Both the read data channel and the write data channel also include a LAST signal to indicate when the transfer of the final data item within a transaction takes place. Elaborate this statement.](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
71. [Explain the significance of AWSIZE.](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
72. [Difference between rvalid, araddr, arvalid?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
73. [If the size of the each transafer is 4 bytes, then what is the total transaction size in bytes if AWLEN value is 4.](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
74. [What is the maximum amount of allowable data that can be sent in a single Write transaction from an AXI Master as per the protocol?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
75. [Explain how a WRAP burst is an example of cache line access?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
76. [Is EBT supported in AXI ? How can the AXI Master disable further writing of the transfer ? How can this be handled in READ transfer?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
77. [What is the simple definition of cache coherency ?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
78. [What is the role of system software with respect to the cache address allotment?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
79. [What will happen if the address is not present in the cache?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
80. [Explain the need for cache coherency](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
81. [Explain cache prefetching.](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
82. [What is the purpose of RA and WA?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
83. [How a protection mechanism is provided in AXI protocol?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
84. [Master1 performing EX-READ to a slave address. At the same time, another master2 performs an EX-READ on the same addrs of the same slave before EX-WRITE of Master1. What will happen in this scenario in terms of EX access result?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
85. [M1 performing EX-RD towards slave address, M2 performing WR(normal) to the same address, what will happen if M1 tried EX-WR on the same location later?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
86. [How does the slave treat the EX RD operation initiated by the master?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
87. [What are the restrictions applied for WRAP bursts?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
88. [In the response signalling mechanism, what is the difference between the responses for READ & WRITE?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
89. [How does AXI interconnect ensures that ID tags from all the masters are unique?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
90. [Why is write data treated as buffered?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
91. [Does the slave should provide the responses to bufferable transactions all the time in a system?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
92. [Where is WLAST asserted?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
93. [An AXI slave MUST NOT give read data unless read address phase completes. Is it TRUE? Explain how?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
94. [What is address boundary calculation?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)
95. [How to set all the WSTRB bits to ‘1’?](https://theartofverification.com/understanding-with-axi-protocol-and-cache-coherency/)