



**PROJECT – 2**  
**Phase-2**

**EEE 234: Digital Integrated Circuit Design**

**Submitted To: Prof. Perry Heedley**

**FALL 2022**

**Date of Submission: 12-04-2022**

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## **(1) PROJECT OVERVIEW**

The purpose of Project is to design, simulate, and build up a "Digital Controller Circuit for a Vending Machine" in 45nm CMOS. This controller must set the signal OUT=1 in order to start dispensing the product when the consumer deposits more money than 75 cents.

A 4-bit code C [3:0] with a value of 1111, which represents 75 cents, is also shown by the controller at all times to indicate the amount of money that has been placed (15 nickels). Only nickels, dimes, and quarters are accepted by the machine. The machine has three distinct sensors, one for each of the three coins. Sensor Q is activated by a quarter, sensor D by a dime, and sensor N by a nickel. When it detects a coin being deposited, a sensor transmits a brief high voltage pulse (logic 1) to the controller.

The amount of change to be given to the customer when the product is dispensed should be shown via the 4-bit code C [3:0] (OUT=1). The controller will be promptly reset to the state of C [3:0] = 0000 and OUT = 0 by sending the reset signal RST high once the product and any updates have been distributed.

## **(2) TEAM CONTRIBUTION**

The project began with an analysis of each requirement, followed by group discussions regarding how well each component should be placed and routed. Given that this was a team project and we coordinated to accomplish the goal, it is challenging to point the contribution of individual.(used Single user login for whole project).Although, we started together with the discussion of how compact the design can be. As we followed the identical floorplan mentioned in phase 1. Anusha worked on floorplan, Placement and Routing of elementary units such as, Logic gates and storage elements (built from Latches) like D Flip-Flop and learned to make a compact layout including the solution of DRC and LVS errors like offGriderror.

As following Anusha, Neha began with the floor planning and layout of entire design by taking the reference from Gate-Level schematic from phase 1. As this is a complex design which includes various combinational as well as sequential components, Neha learnt about the detailing of metal layer and P-stampsubstrateerror from DRC and LVS.

The report was written by Anusha, and we both gained new knowledge together, making it easier for an individual to accomplish.

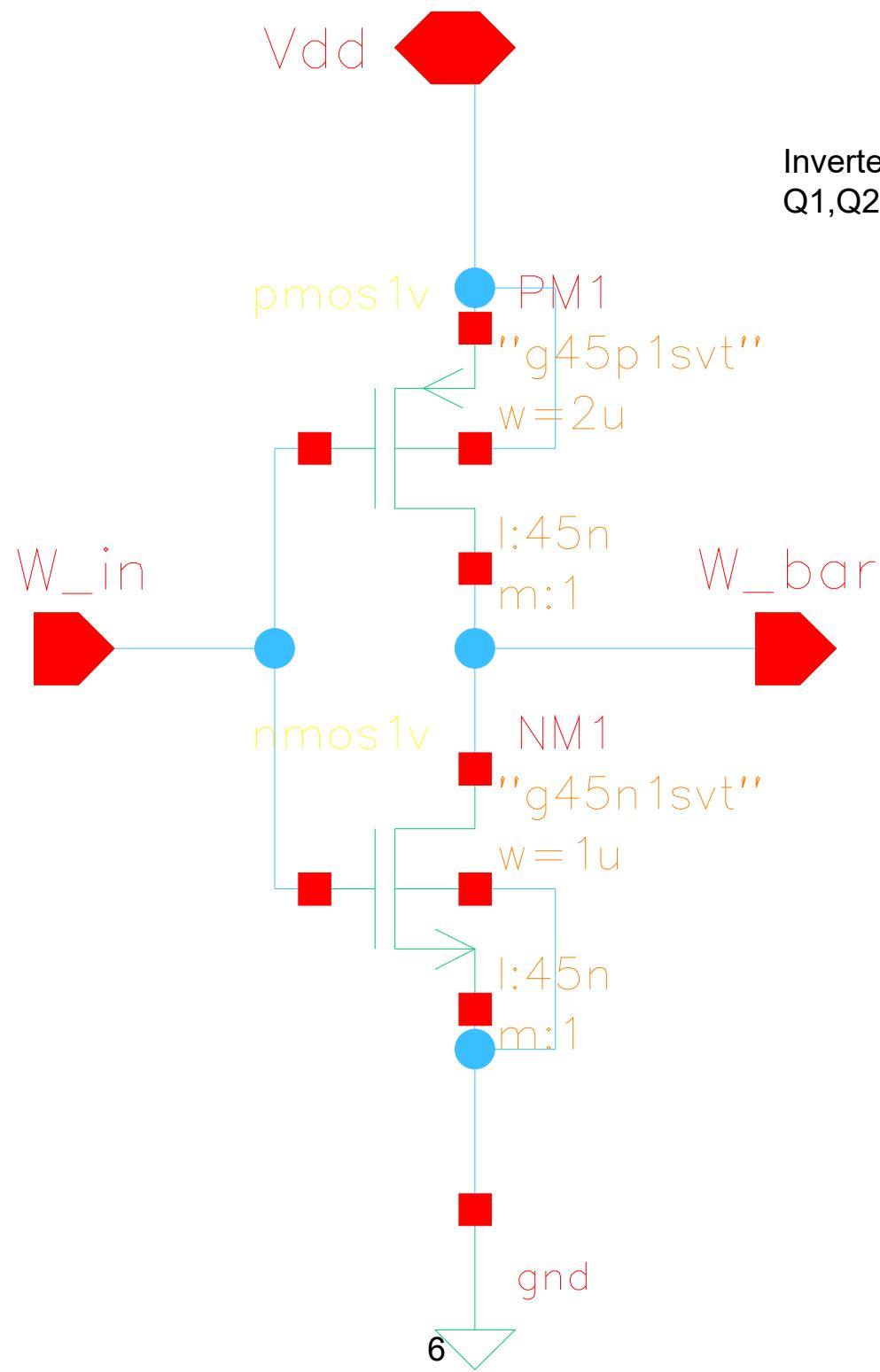
# **TRANSISTOR LEVEL SCHEMATIC OF BUILDING BLOCKS**

Submitted by:

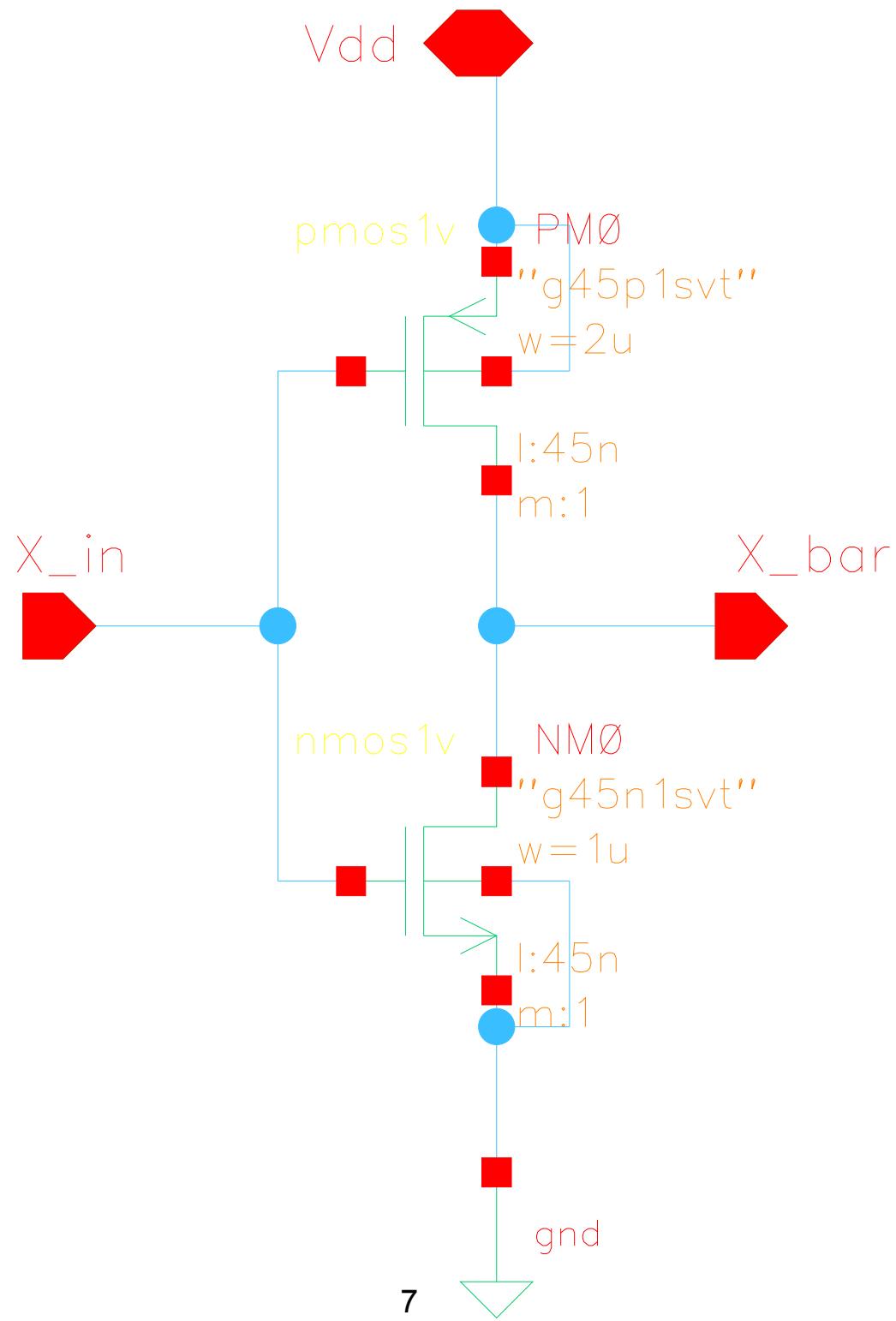
Anusha S

Neha Gour

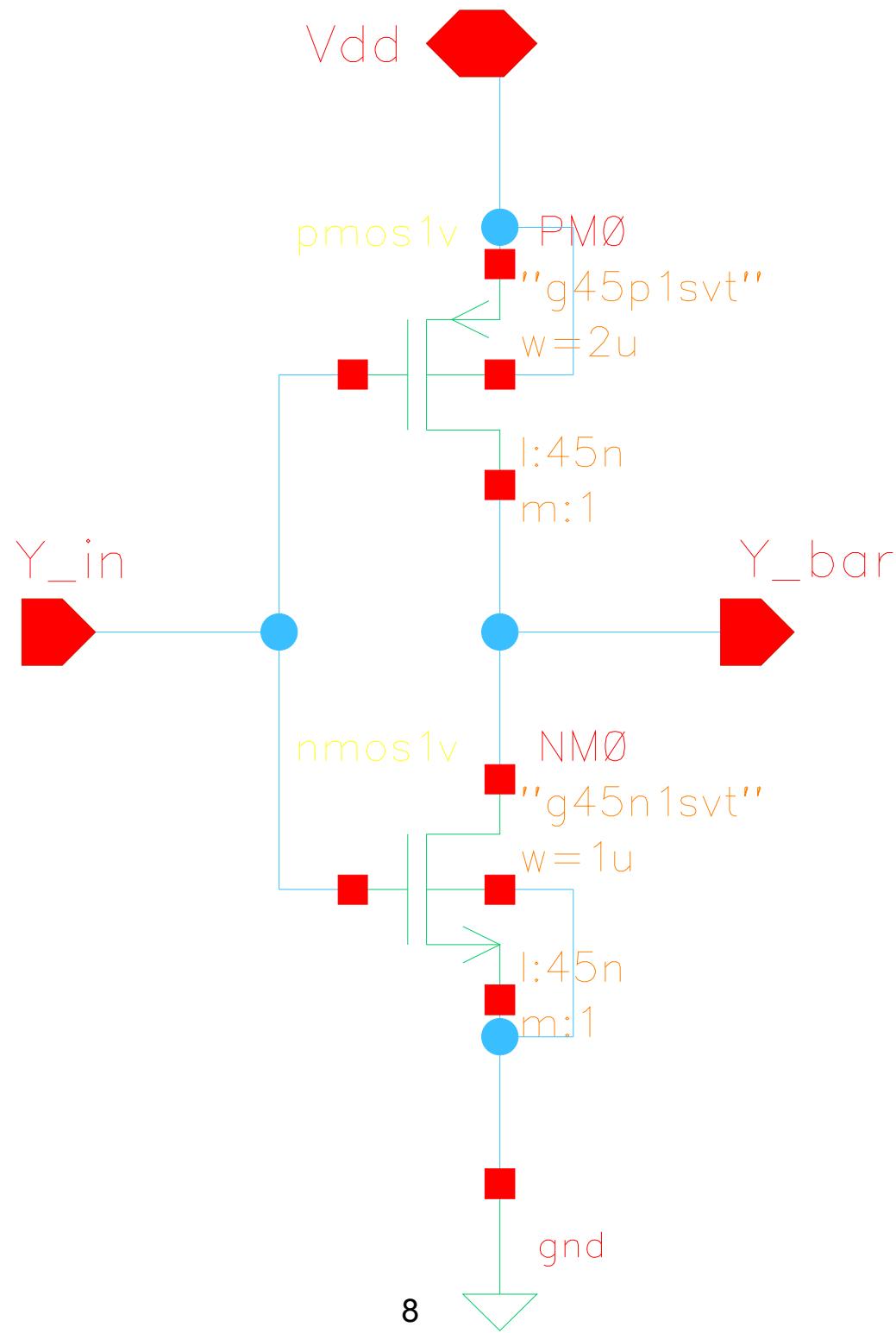
Inverter (same for below  
Q1,Q2,W,X,Y,Z Inputs)



Submitted by:  
Anusha S  
Neha Gour



Submitted by:  
Anusha S  
Neha Gour

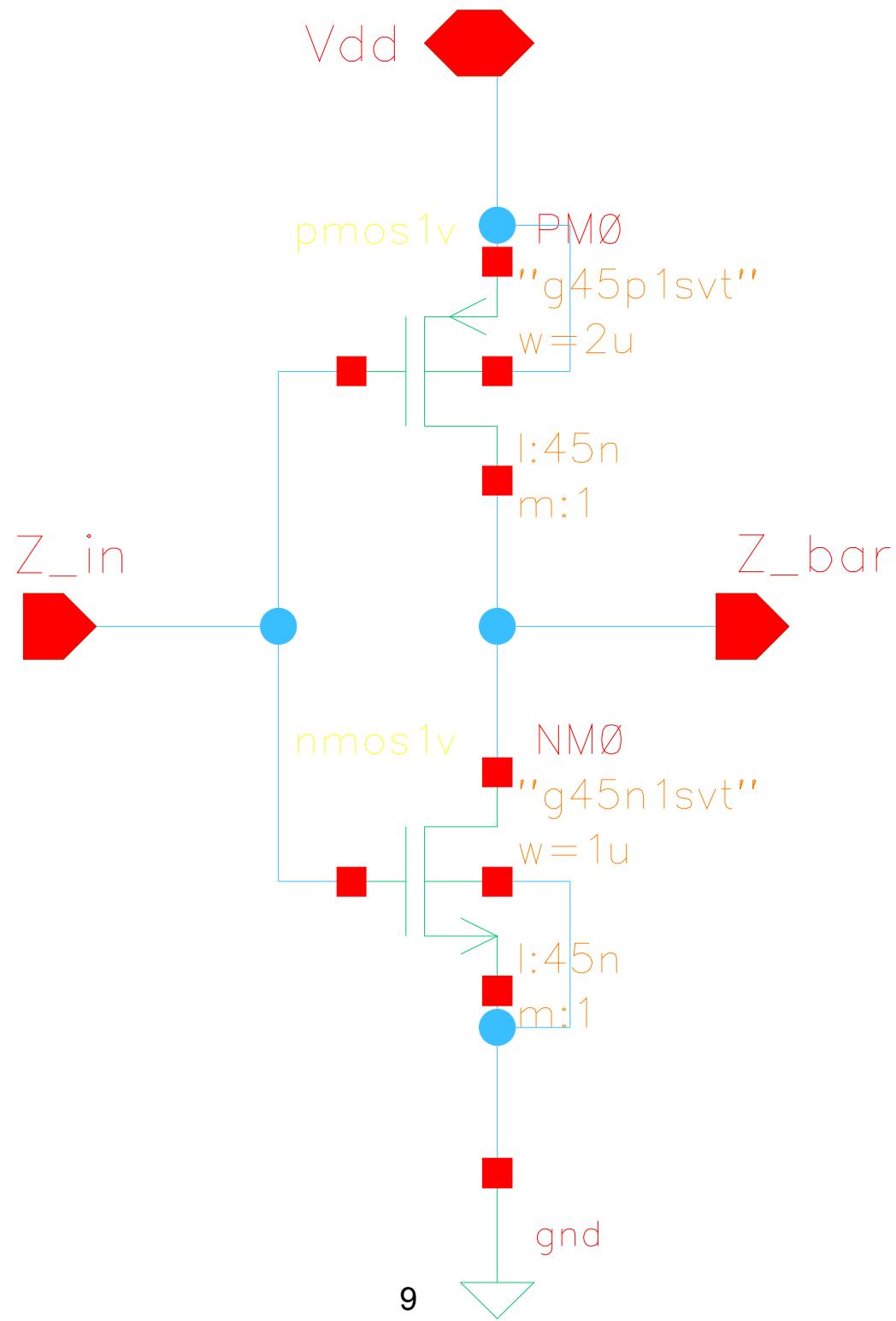


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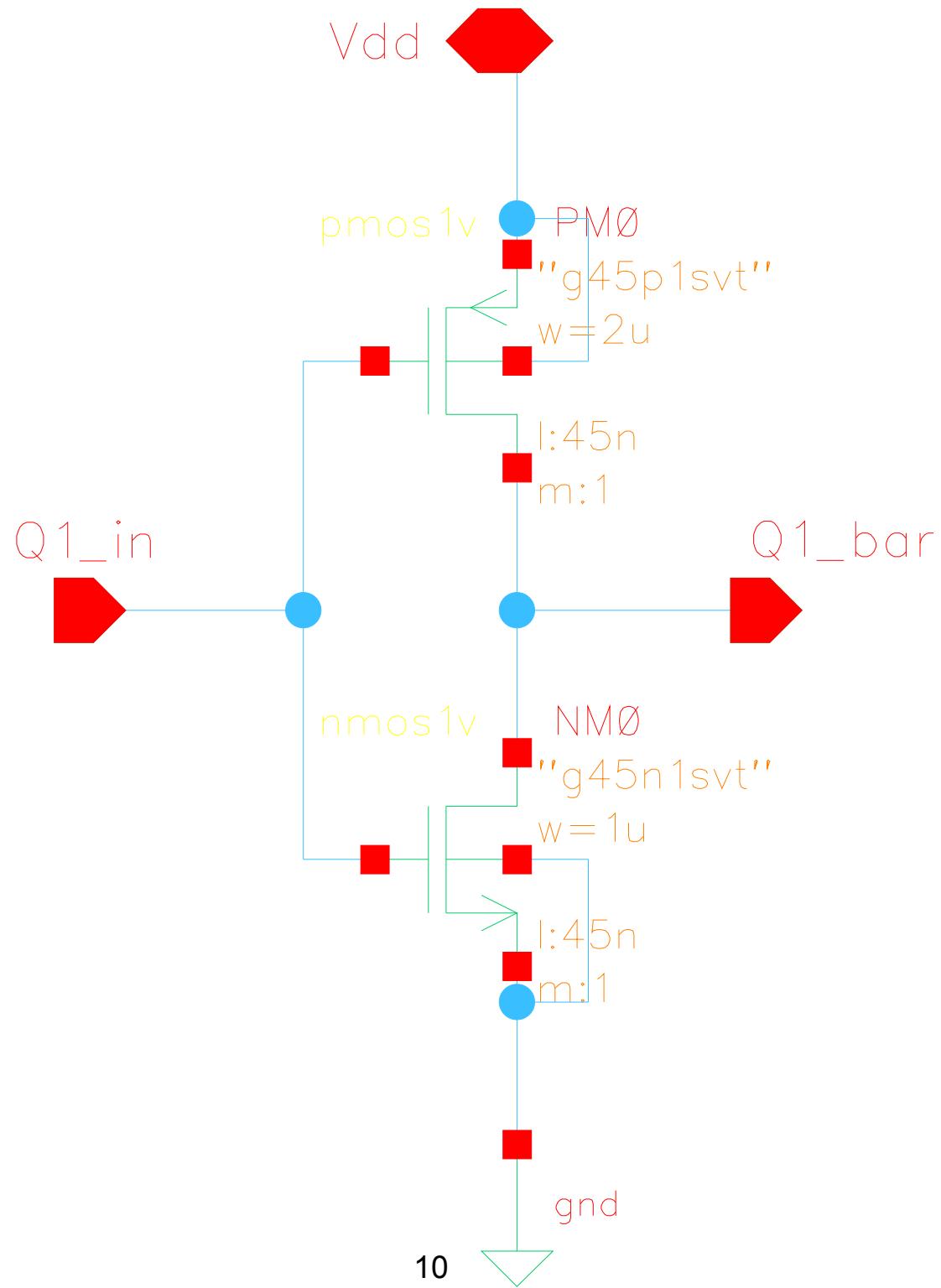
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Anusha S

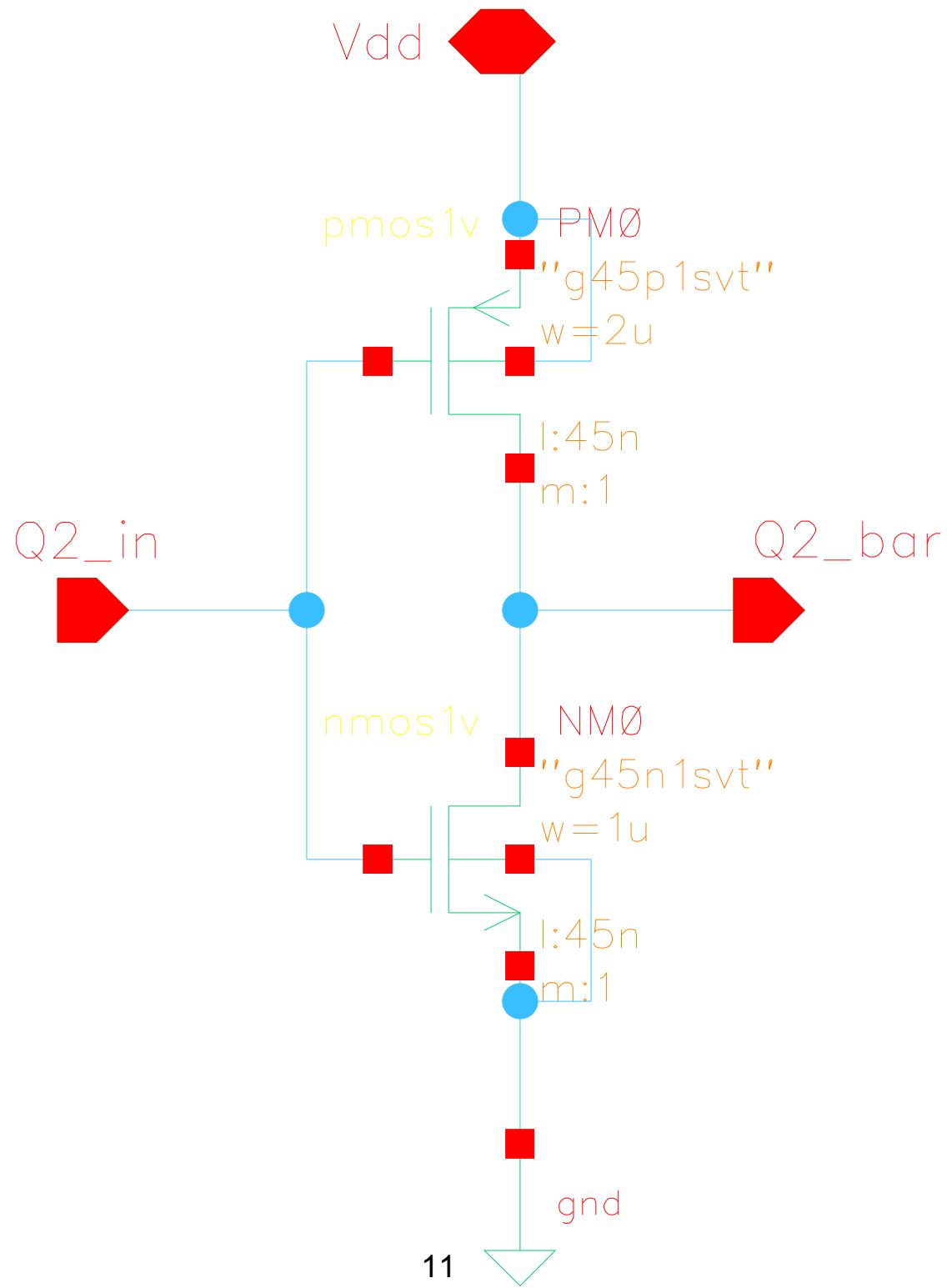
Neha Gour



Submitted by:  
Anusha S  
Neha Gour



Submitted by:  
Anusha S  
Neha Gour



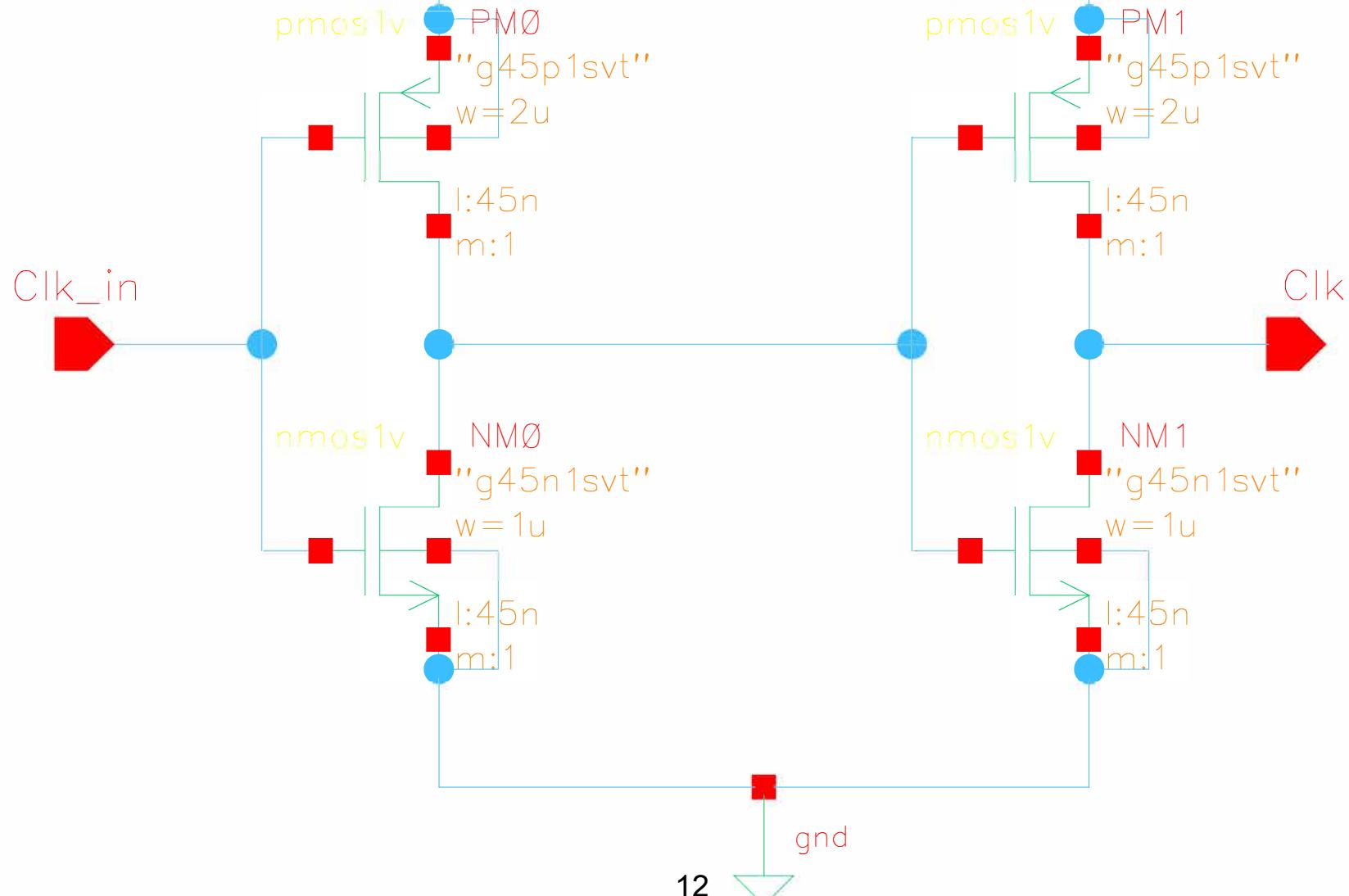
Submitted by:

Anusha S

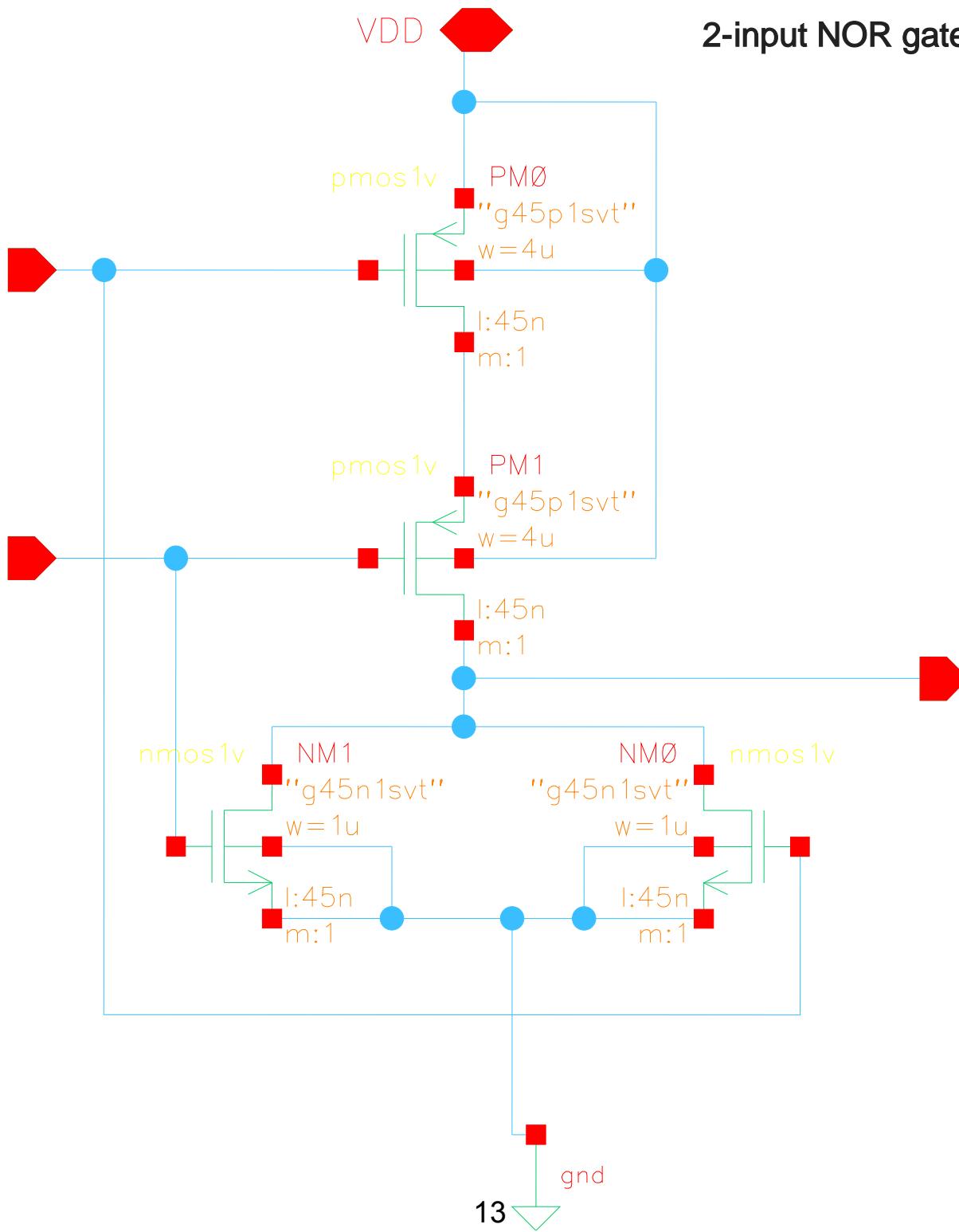
Neha Gour

Vdd

**Clock Input**

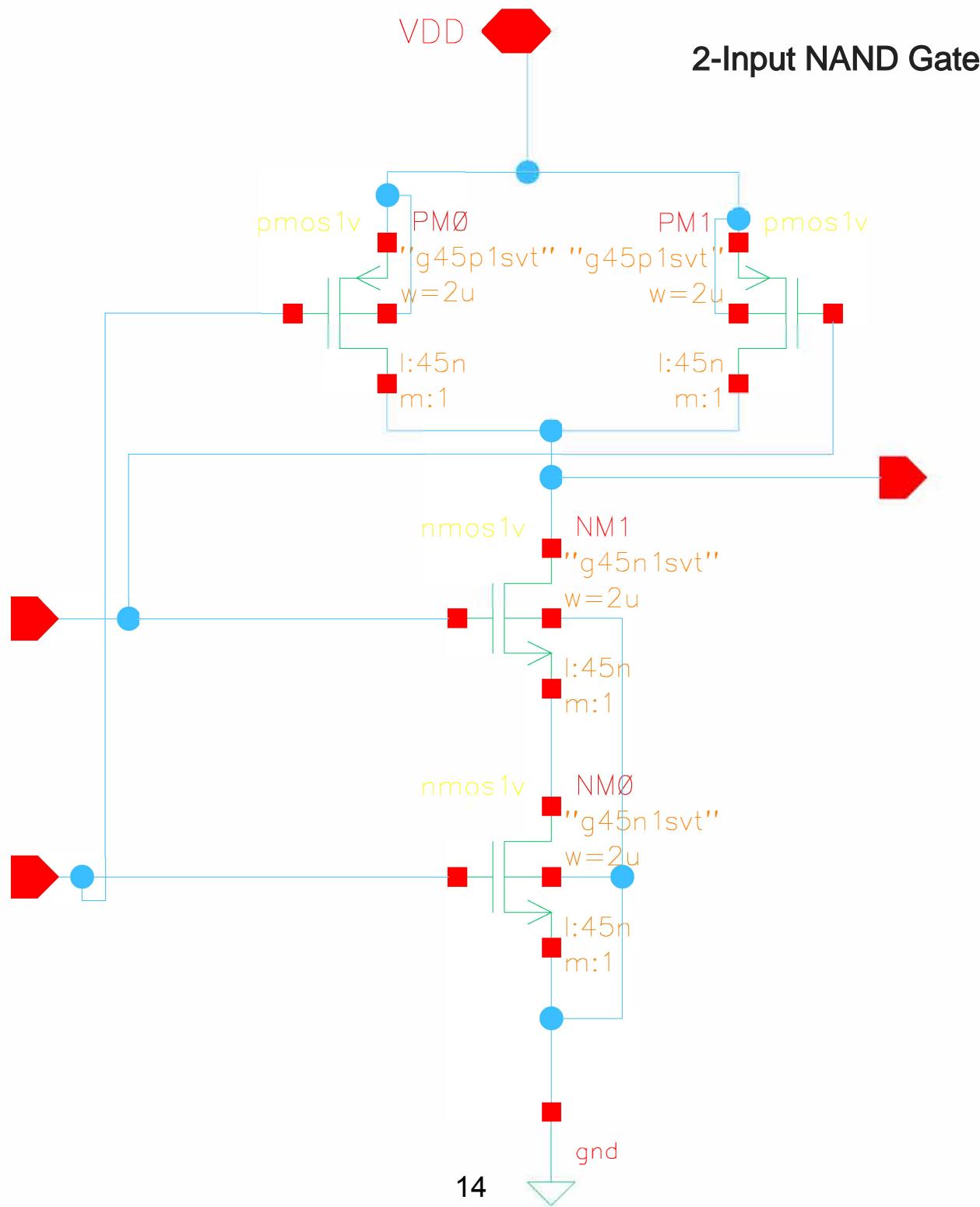


## 2-input NOR gate



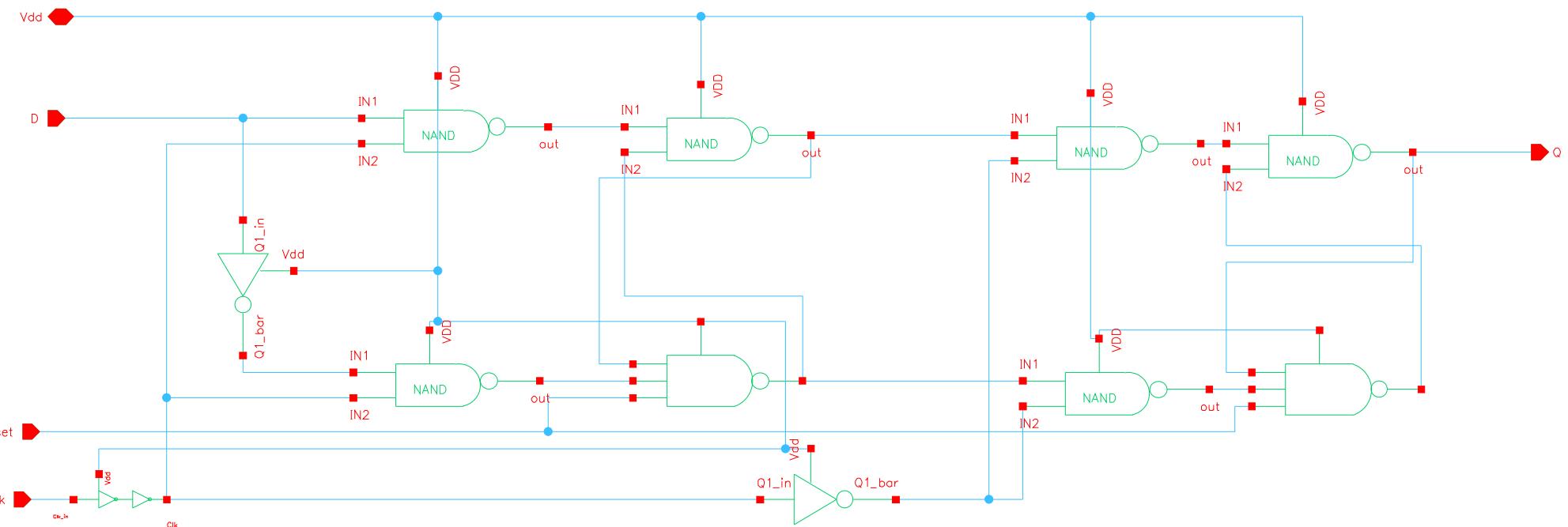
Submitted by:  
Anusha S  
Neha Gour

Submitted by:  
Anusha S  
Neha Gour



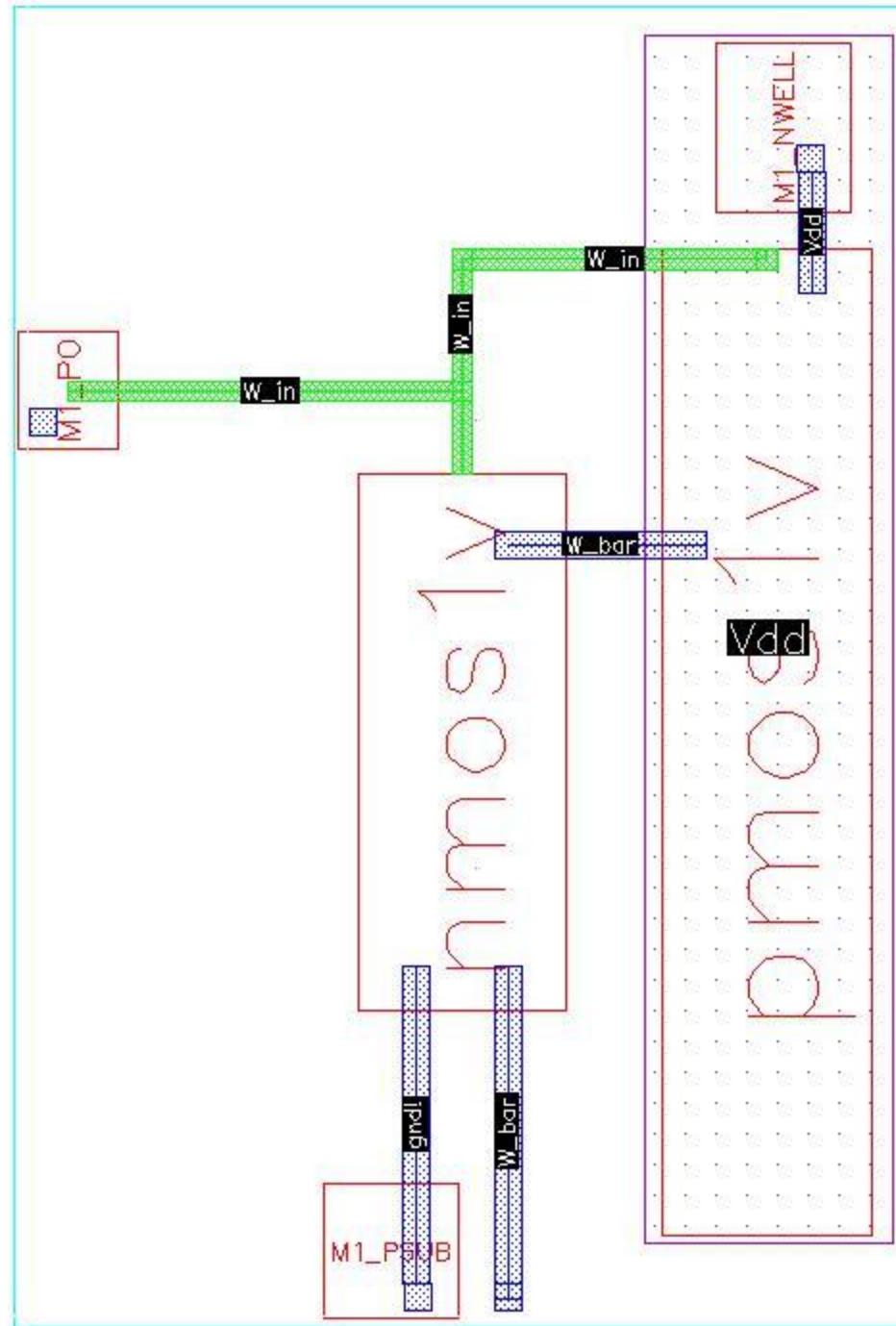
Submitted by:  
Anusha S  
Neha Gour

## D-Flip Flop



## **LAYOUT OF BUILDING BLOCKS**

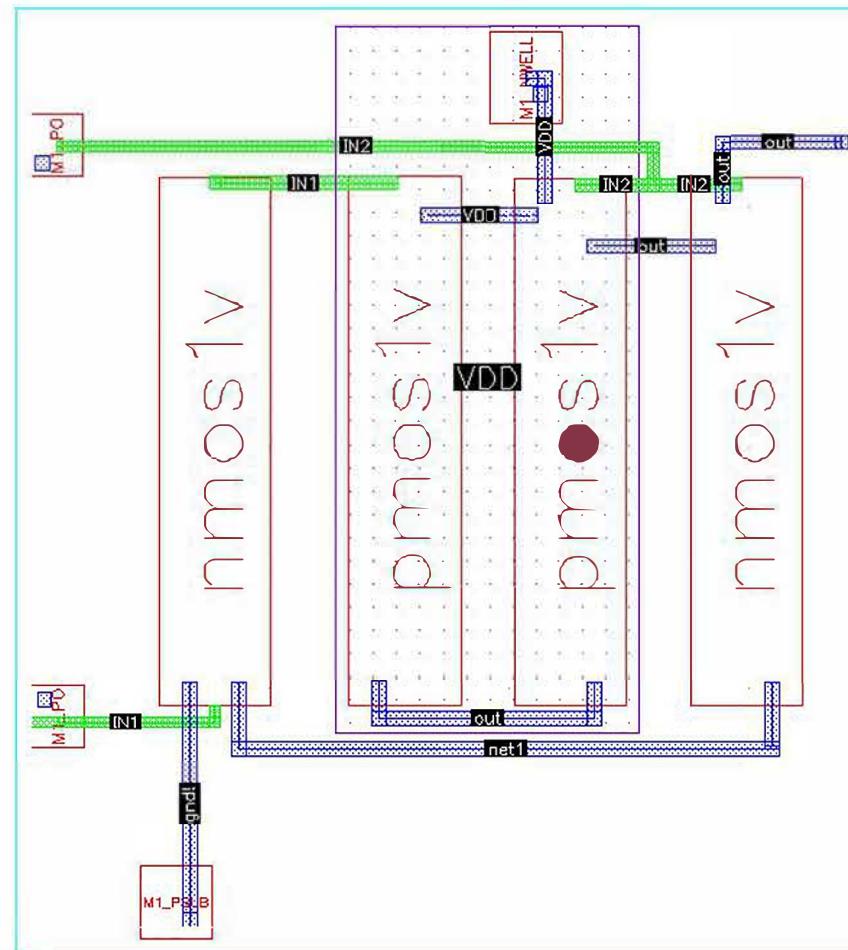
Submitted by:  
Anusha S  
Neha Gour



**Inverter Layout**  
**(Layout is same for Q1, Q2,  
W,X,Y, Z Inputs )**

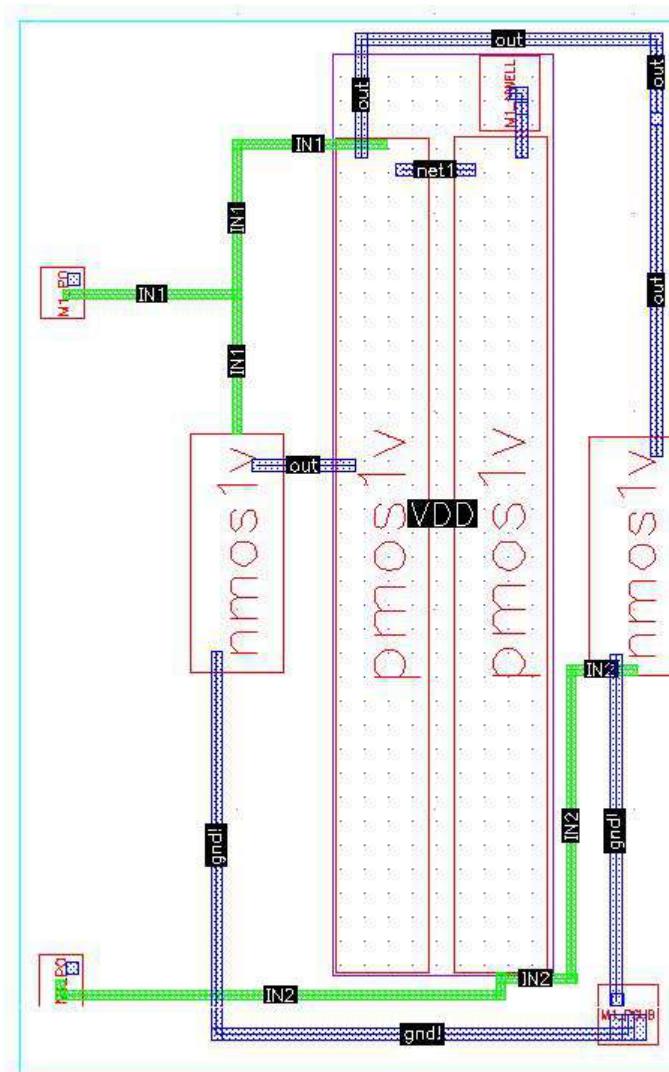
Submitted by:  
Anusha S  
Neha Gour

## 2 - Input NAND Gate



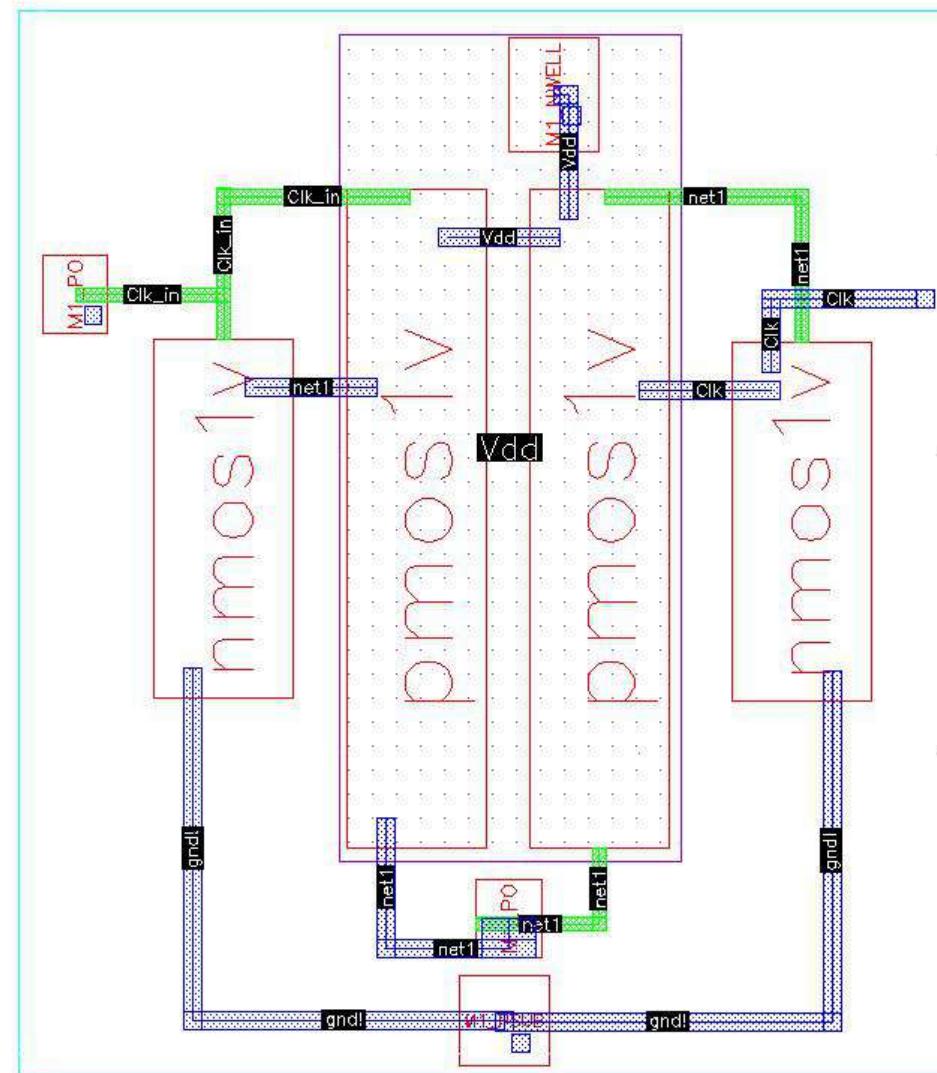
Submitted by:  
Anusha S  
Neha Gour

## 2 - Input NOR Gate



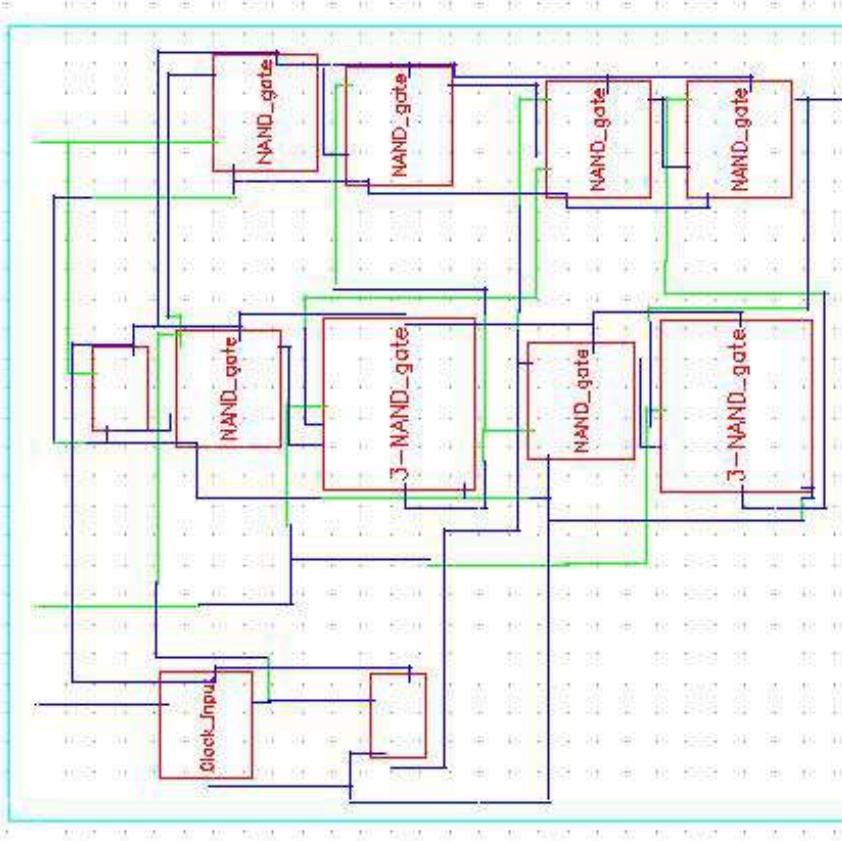
Submitted by:  
Anusha S  
Neha Gour

## Clock Layout



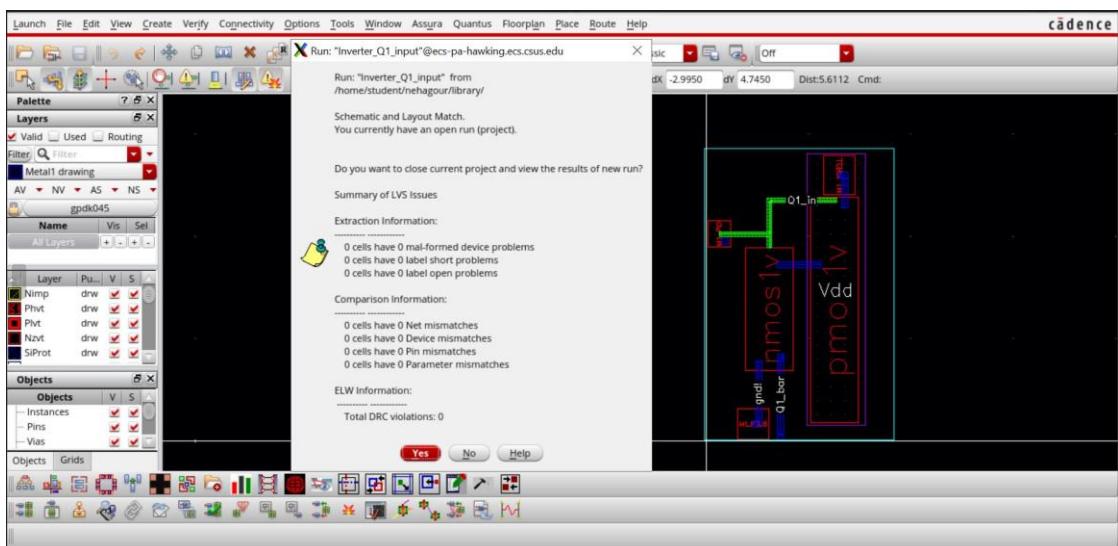
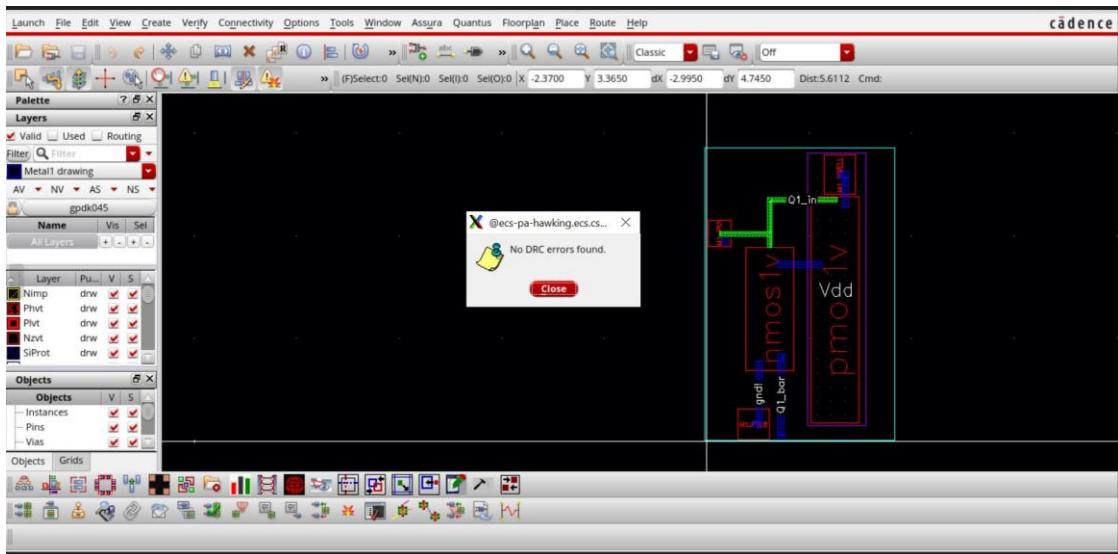
**Submitted by:**  
**Anusha S**  
**Neha Gour**

## D Flip Flop

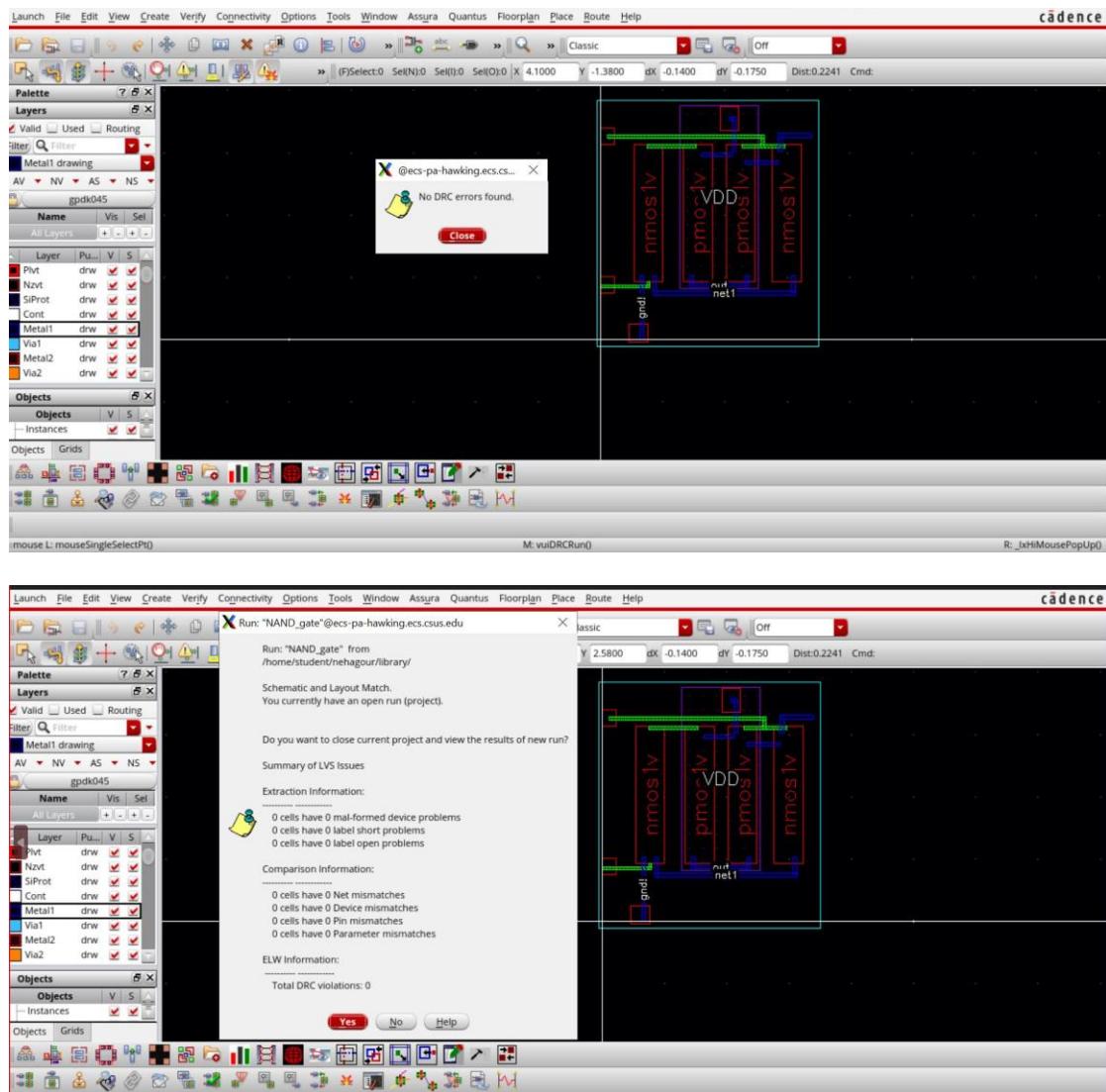


**DRC AND LVS REPORT OF**  
**BUILDING BLOCKS**

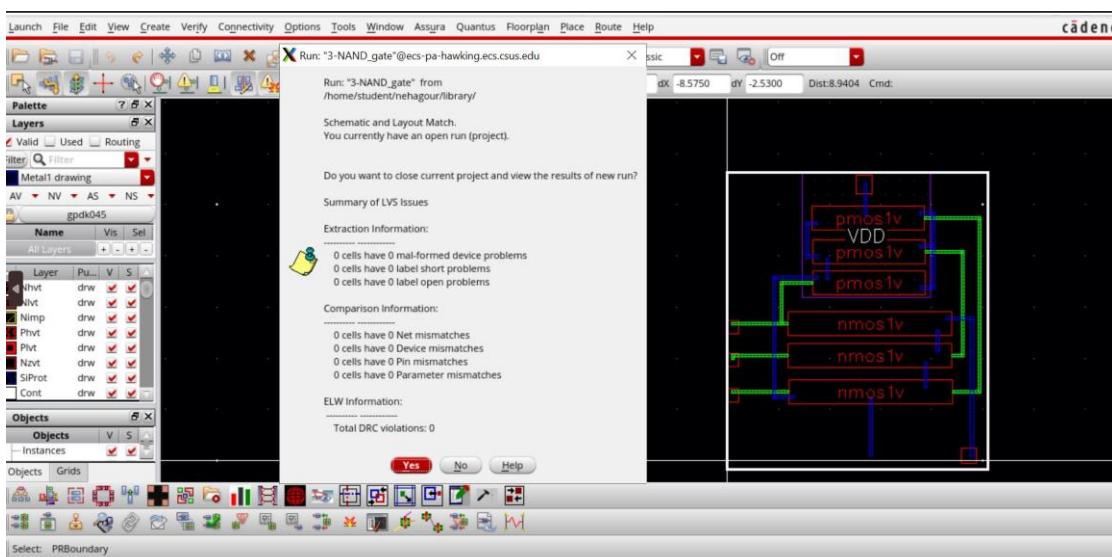
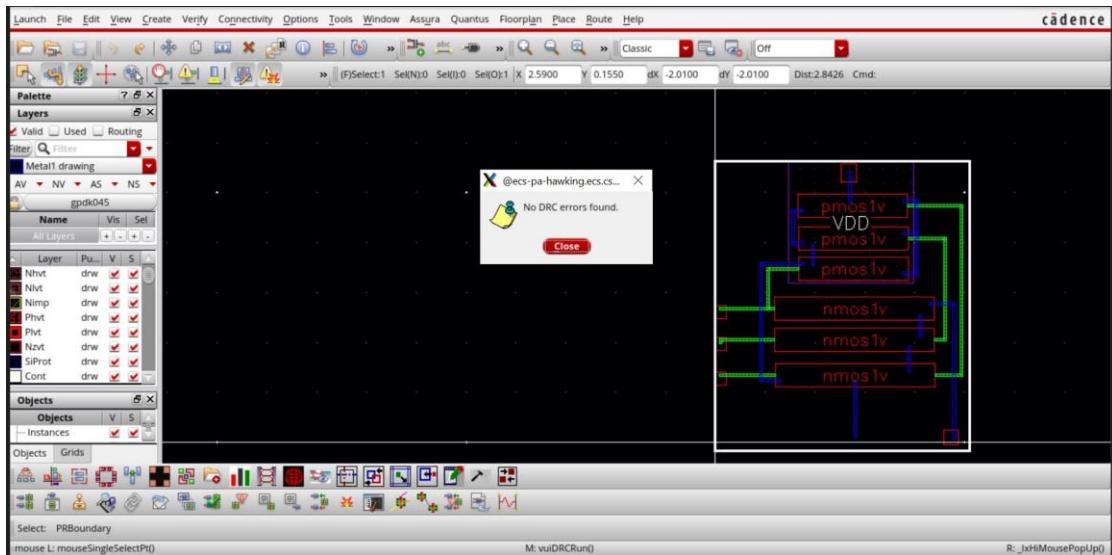
## Q1\_Inverter (Same for Q1, Q2,W,X,Y,Z Inputs)



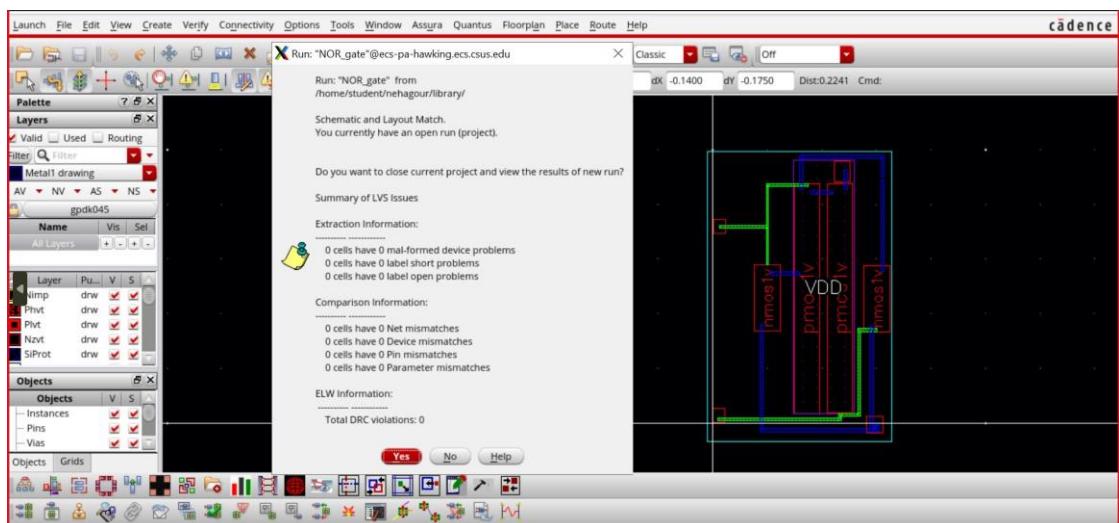
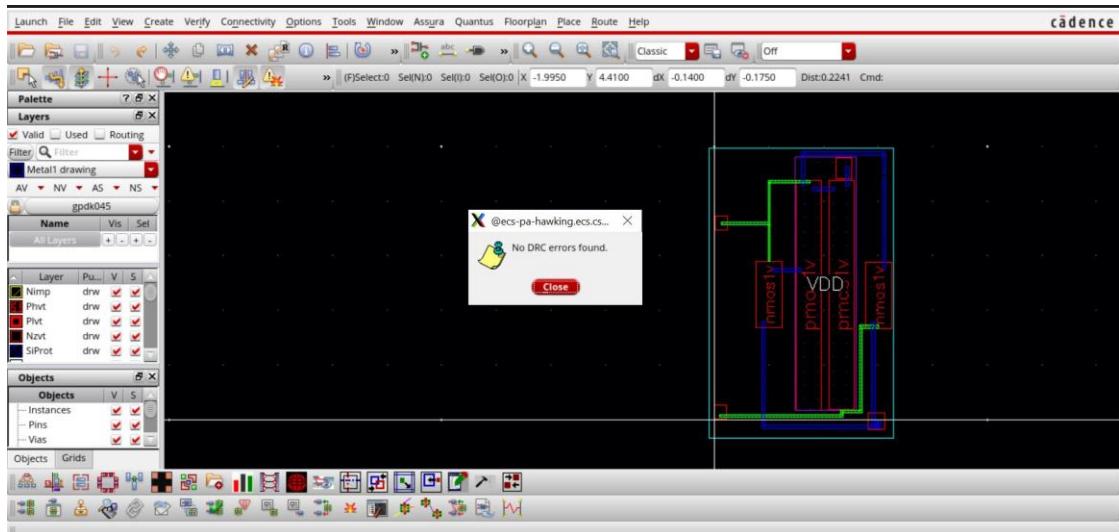
## 2- Input NAND gate:



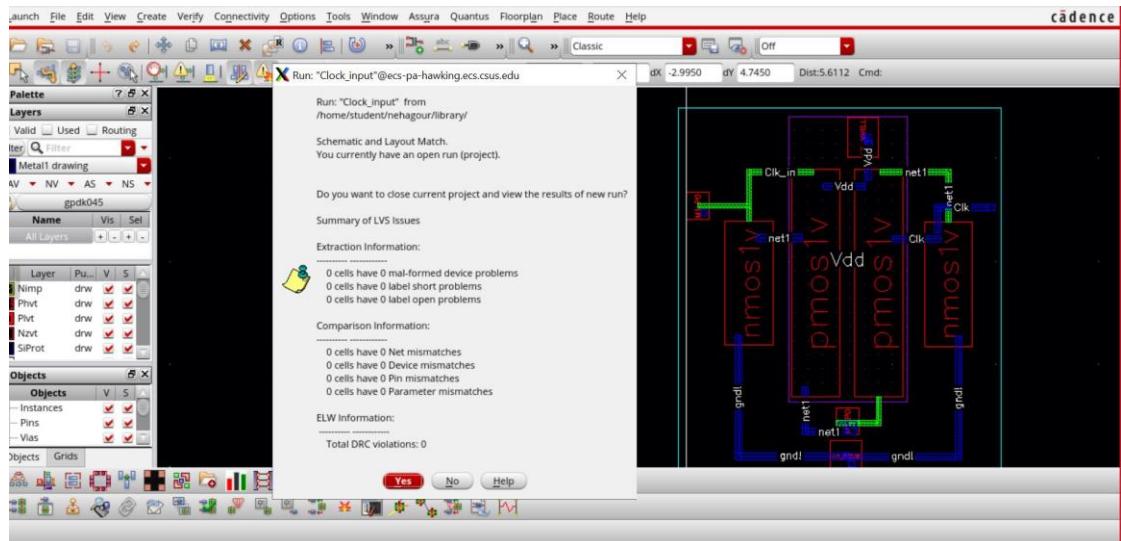
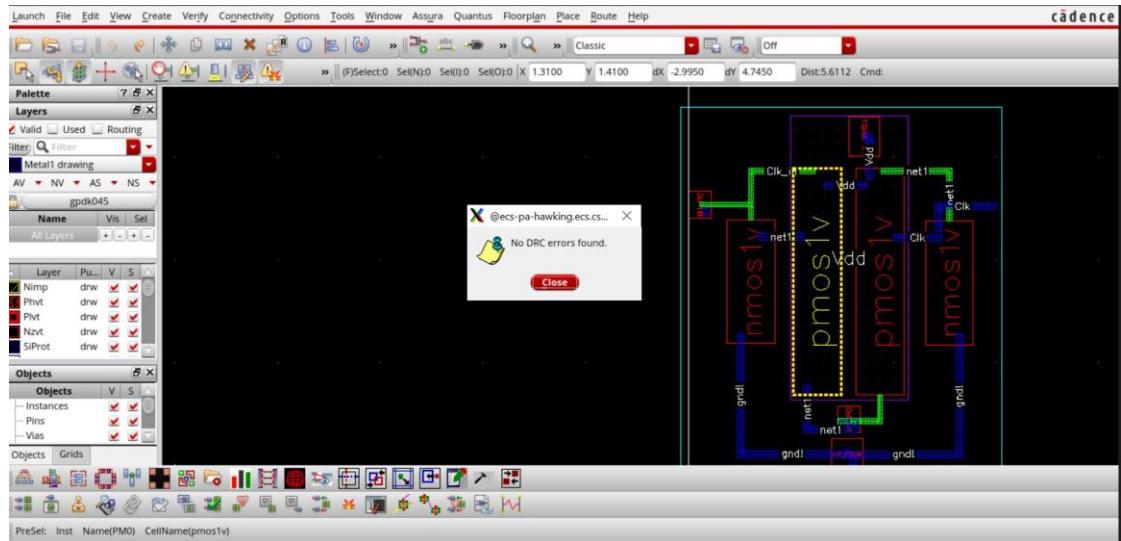
### 3- Input NAND gate:



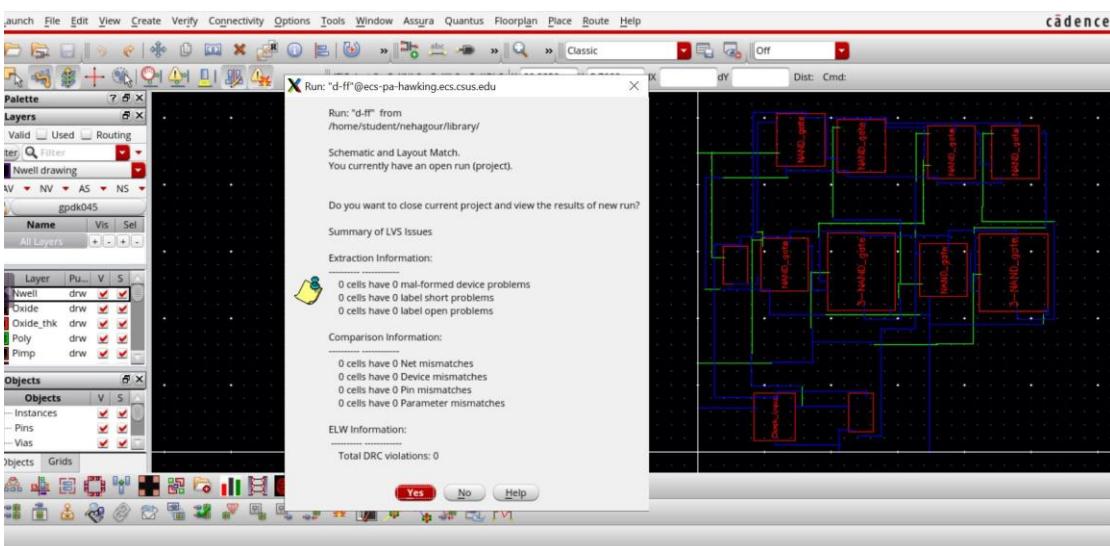
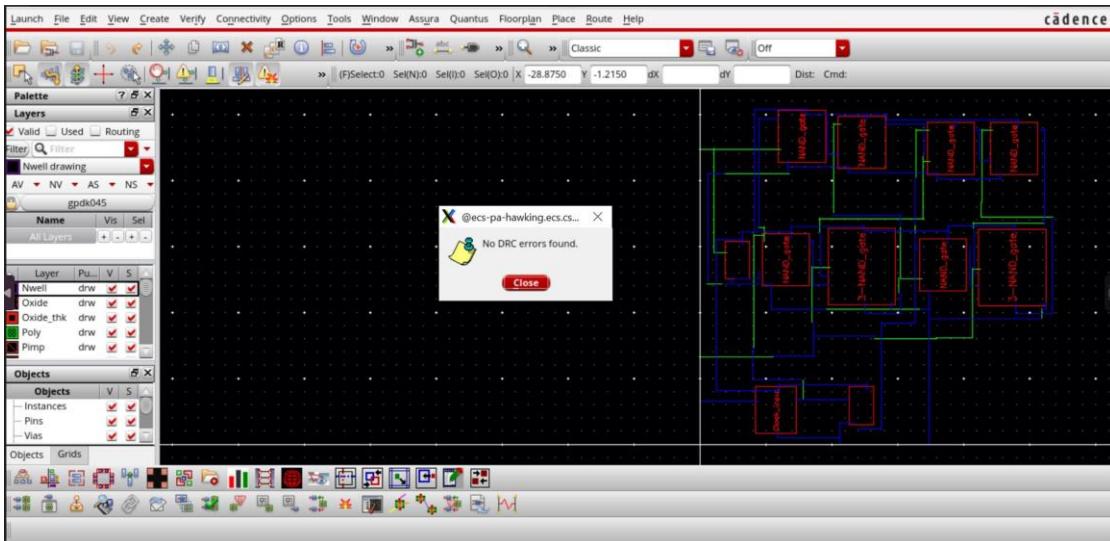
## 2- Input NOR gate:



## Clock Input :



## D- Flip Flop:

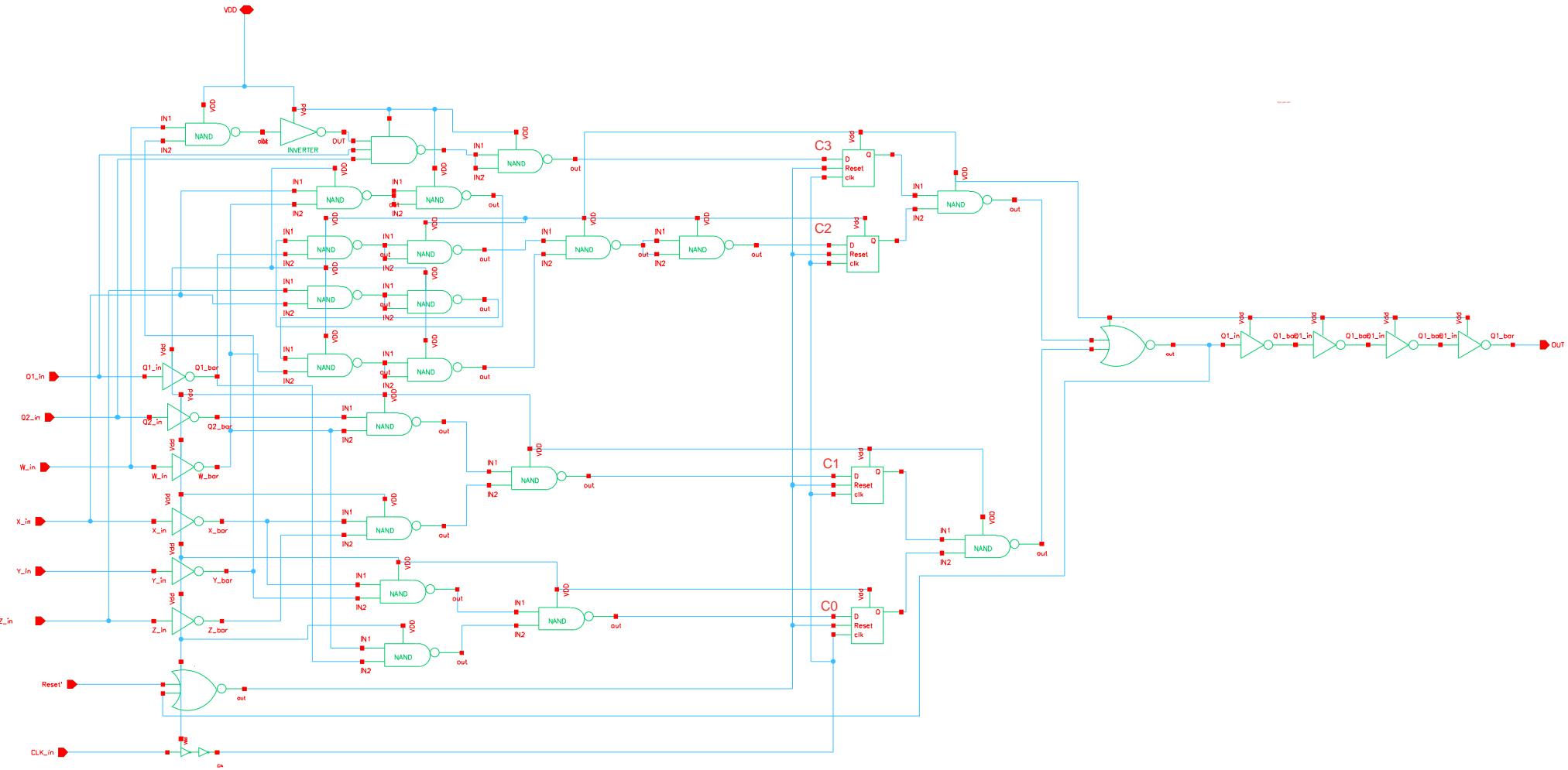


# **GATE LEVEL SCHEMATIC OF**

# **DESIGN**

Submitted by:  
Anusha S  
Neha Gour

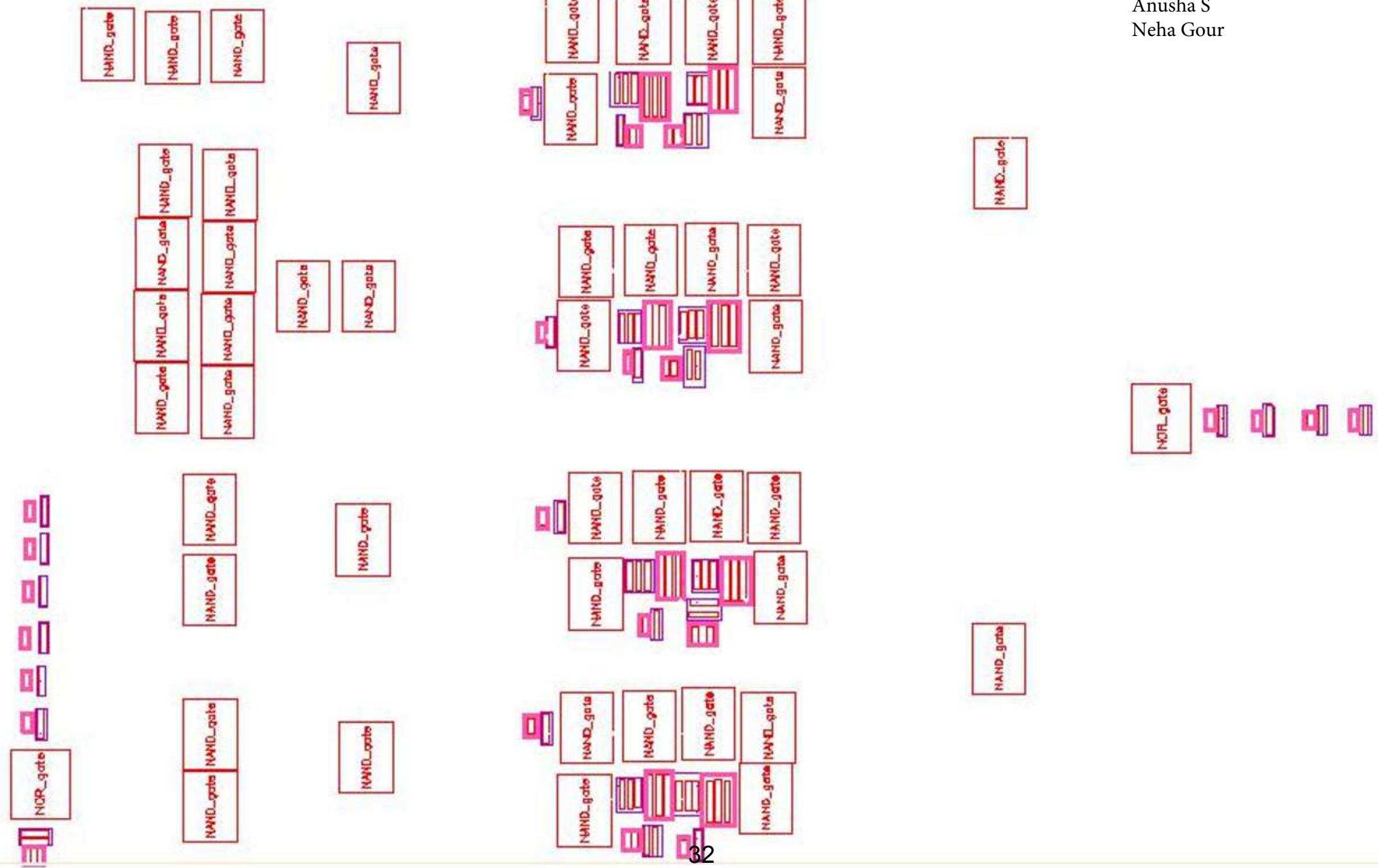
## GATE LEVEL SCHEMATIC



## **FLOOR PLAN OF DESIGN**

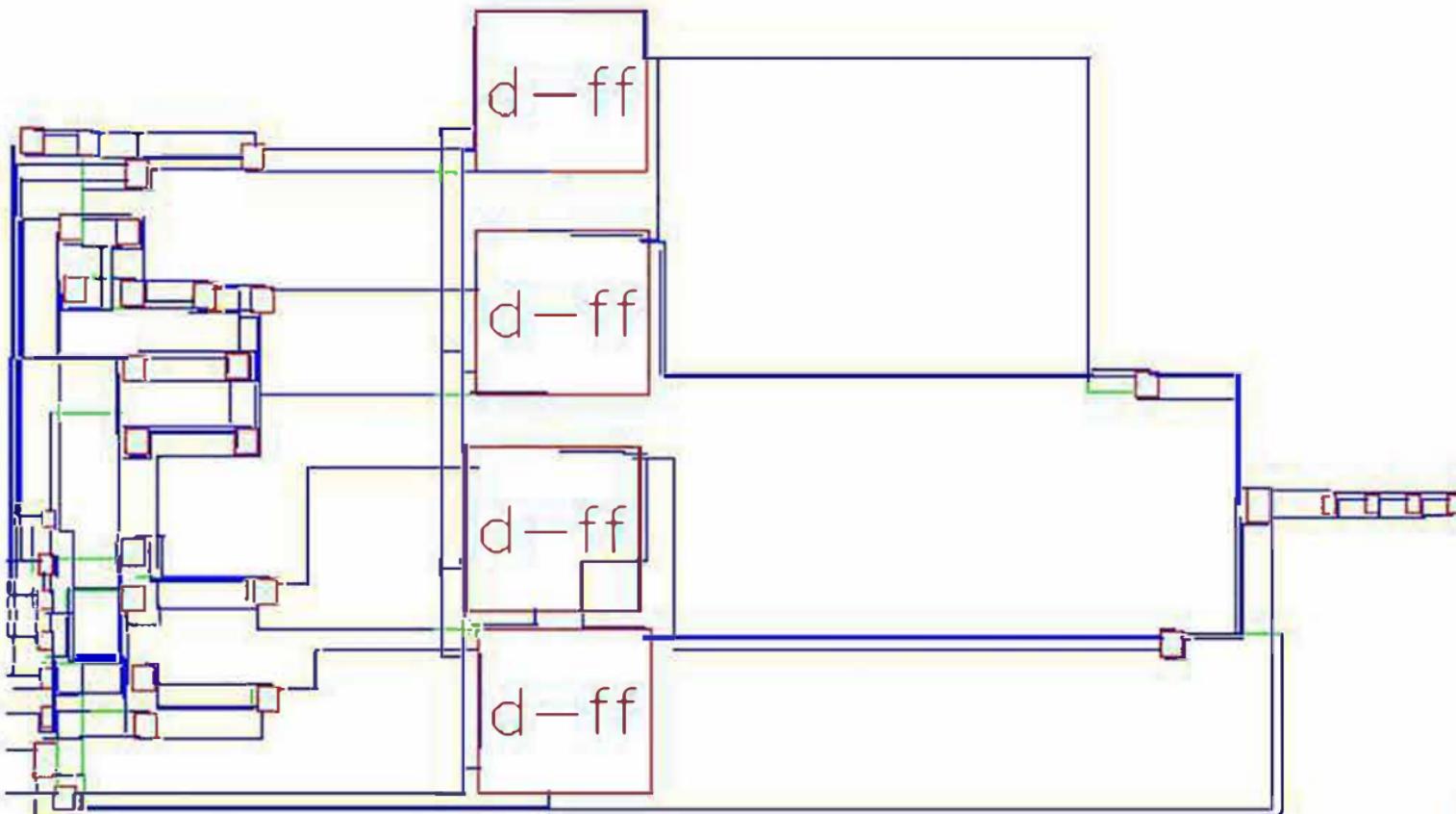
## Floor Plan

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Neha Gour



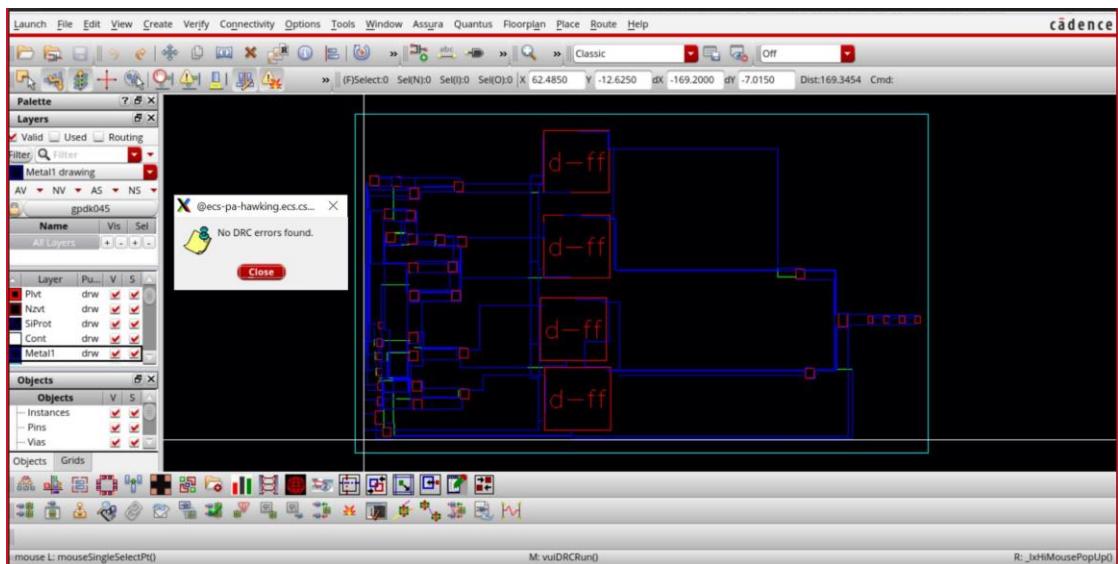
## **LAYOUT OF DESIGN**

Submitted by :  
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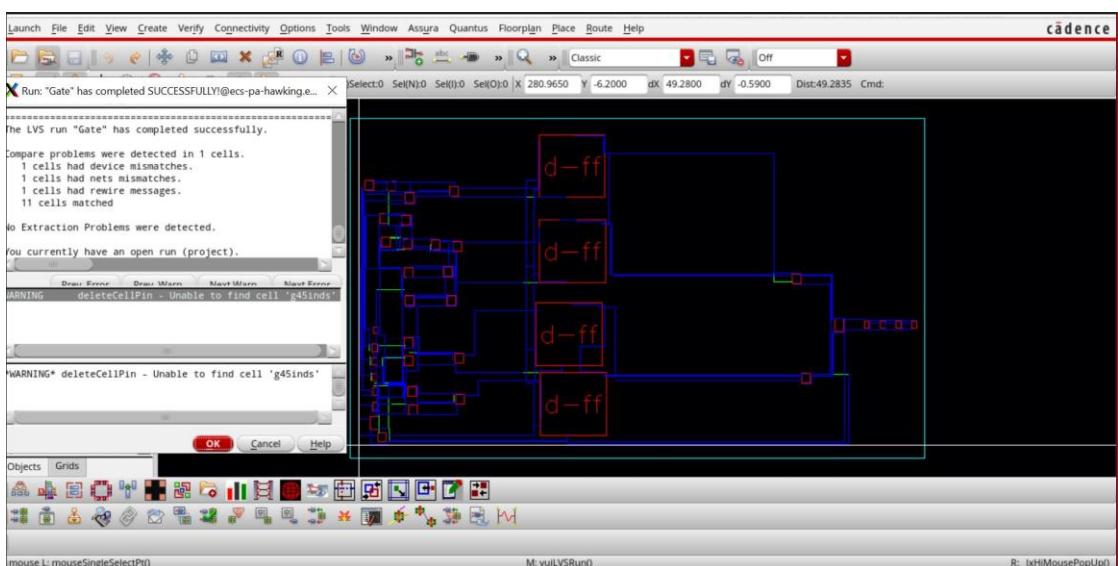


## **DRC AND LVS OF DESIGN**

## DRC :



## LVS :



## **Conclusion:**

Phase 2 of this project taught us Floor planning and layout with the good engineering judgement of Placement & Routing by using minimum white space. As following industry standard, we have used NAND gate to implement the digital vending machine controller.

By using 45nm gdk library we designed transistor level schematics for logic gates, master-slave D Flip-flop and clock. The gate level schematic of building blocks as well as the design are built and simulated in virtuoso. With the given design specifications We implemented floor plan as well as layout of project. Crucial stage in managing circuit design complexity is to route between components and optimise it where the exact connections are determined. Since Poly has a higher resistance than metal, and lesser metals have a higher resistance than the top metal layer. We used poly for short connections, lower metals for long connections, and the top metal layer for power connections and extra-long connections. We have followed all the routing rules to create a compact layout. Instead of rectangle we used polygon to create n-well. DRC and LVS check for all the components is done to ensure the circuit is with zero errors.

Given that this was a team effort, we collaborated to set team goals and meet deadlines.