PROJECT – 2
Phase-1

EEE 234: Digital Integrated Circuit Design
Submitted To: Prof. Perry Heedley
FALL 2022

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(1) PROJECT OVERVIEW

Designing, simulating, and laying up a "***Digital Controller Circuit for a Vending Machine***" in 45nm CMOS is the aim of Project. When the total amount deposited by the consumer exceeds 75 cents, this controller needs to set the signal OUT=1 to start dispensing the product.

In order to show how much money has been placed, the controller also displays a 4-bit code C [3:0] at all times, with a value of 1111 denoting 75 cents (15 nickels). The machine accepts nickels, dimes, and quarters only as input. For each of the three coins, the machine includes three unique sensors. A quarter activates sensor Q, a dime activates sensor D, and a nickel activates sensor N. A sensor sends the controller a brief high voltage pulse (logic 1) when it recognizes a coin being deposited.

The 4-bit code C [3:0] should display the amount of change to be handed to the consumer when the product is dispensed (OUT=1). A reset signal RST will quickly go high after the product and any changes have been dispersed to reset the controller to the state of C [3:0] = 0000 and OUT=0.

(2) STATE ENCODING

We considered Q, D, N sensor as a two bit variable.

Q	D	N	Q1_IN	Q2_IN
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
1	0	0	1	1

Below is the Truth Table for possible state combinations as per design specification:

	Present State				Inputs		Next State				Output
Decimal	W	X	Y	Z	Q1	Q2	C3	C2	C1	C0	OUT
0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	1	0	0	0	1	0
2	0	0	0	0	1	0	0	0	1	0	0
3	0	0	0	0	1	1	0	1	0	1	0
4	0	0	0	1	0	0	0	0	0	1	0
5	0	0	0	1	0	1	0	0	1	0	0
6	0	0	0	1	1	0	0	0	1	1	0
7	0	0	0	1	1	1	0	1	1	0	0
8	0	0	1	0	0	0	0	0	1	0	0
9	0	0	1	0	0	1	0	0	1	1	0
10	0	0	1	0	1	0	0	1	0	0	0
11	0	0	1	0	1	1	0	1	1	1	0
12	0	0	1	1	0	0	0	0	1	1	0
13	0	0	1	1	0	1	0	1	0	0	0
14	0	0	1	1	1	0	0	1	0	1	0
15	0	0	1	1	1	1	1	0	0	0	0
16	0	1	0	0	0	0	0	1	0	0	0
17	0	1	0	0	0	1	0	1	0	1	0
18	0	1	0	0	1	0	0	1	1	0	0
19	0	1	0	0	1	1	1	0	0	1	0
20	0	1	0	1	0	0	0	1	0	1	0
21	0	1	0	1	0	1	0	1	1	0	0
22	0	1	0	1	1	0	0	1	1	1	0
23	0	1	0	1	1	1	1	0	1	0	0
24	0	1	1	0	0	0	0	1	1	0	0
25	0	1	1	0	0	1	0	1	1	1	0
26	0	1	1	0	1	0	1	0	0	0	0
27	0	1	1	0	1	1	1	0	1	1	0

28	0	1	1	1	0	0	0	1	1	1	0
29	0	1	1	1	0	1	1	0	0	0	0
30	0	1	1	1	1	0	1	0	0	1	0
31	0	1	1	1	1	1	1	1	0	0	0
32	1	0	0	0	0	0	1	0	0	0	0
33	1	0	0	0	0	1	1	0	0	1	0
34	1	0	0	0	1	0	1	0	1	0	0
35	1	0	0	0	1	1	1	1	0	1	0
36	1	0	0	1	0	0	1	0	0	1	0
37	1	0	0	1	0	1	1	0	1	0	0
38	1	0	0	1	1	0	1	0	1	1	0
39	1	0	0	1	1	1	1	1	1	0	0
40	1	0	1	0	0	0	1	0	1	0	0
41	1	0	1	0	0	1	1	0	1	1	0
42	1	0	1	0	1	0	1	1	0	0	0
43	1	0	1	0	1	1	1	1	1	1	1
44	1	0	1	1	0	0	1	0	1	1	0
45	1	0	1	1	0	1	1	1	0	0	0
46	1	0	1	1	1	0	1	1	0	1	0
47	1	0	1	1	1	1	-	-	-	-	0
48	1	1	0	0	0	0	1	1	0	0	0
49	1	1	0	0	0	1	1	1	0	1	0
50	1	1	0	0	1	0	1	1	1	0	0
51	1	1	0	0	1	1	-	-	-	-	0
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54	1	1	0	1	1	0	1	1	1	1	1
55	1	1	0	1	1	1	-	-	-	-	0
56	1	1	1	0	0	0	1	1	1	0	0
57	1	1	1	0	0	1	1	1	1	1	1
58	1	1	1	0	1	0	-	-	-	-	0
59	1	1	1	0	1	1	-	-	-	-	0
60	1	1	1	1	0	0	1	1	1	1	1
61	1	1	1	1	0	1	-	-	-	-	0
62	1	1	1	1	1	0	-	-	-	-	0
63	1	1	1	1	1	1	-	-	-	-	0

(3) LOGIC MINIMIZATION:

Logic equations are obtained from state machine by using theorems and laws as per digital logic design.

$$\mathbf{C3} = Q1 + Q2 + W\overline{Y}$$
$$\mathbf{C2} = \overline{W}\,XZ + \overline{W}\,X\,\overline{Q1}$$
$$\mathbf{C1} = \overline{W} + \overline{Z} + \overline{Q2} + \overline{X}$$
$$\mathbf{C0} = \overline{X} + \overline{Y} + \overline{Q1} + \overline{W}$$

(4) TEAM CONTRIBUTION:

The project began with an analysis of each requirement, followed by group discussions regarding how well each requirement was understood. Given that this was a team project and that we coordinated to accomplish the goal, it is challenging to point the contribution of individual. Although, we started together with the discussion of possible states, design specifications and concluded up with the possible state table.

Anusha worked on the Karnaugh map (K-map), which uses Digital Logic Design, Boolean algebra laws and theorems like De Morgan's theorem, to reduce the Boolean algebraic expressions. Later, it was decided to size (W/L) each MOSFET individually for the optimum performance. Secondly, worked on the calculations of the (W/L) ratio, mid-point voltage, rise and fall times, and capacitance for every logic gate (Inverter, NAND,NOR,D-Flip-flops).

Neha began with the designing of project, which included transistor level schematics (inverters, NAND, NOR, clock, D-Flip-flops), functionality check of individual logic gate. Gate level schematics are obtained from the equations given by Anusha of entire project.Cadence virtuoso tool is explored and used to do the simulation for the correct functionality check and compact floorplan by Neha. Anusha created the report, and we worked as a team to finish it.

(5) CALCULATIONS

(5A) W/L ratios of MOSFET

In designing part, we are choosing the MOSFET'S W/L value for the optimum performance.

Best case:

For a two input NAND gate, all NMOS are ON when A=B=1 and all PMOS are ON when A=B=0.Therefore, the best scenario will result from the combination 00 or 11, which means that all transistors will be switched on simultaneously. (Pull up Network or Pull Down network).

Worst case:

Whenever either the output to ground for a pull down network or the Vdd to output for a pull up network has at least one conducting path. In the worst situation, just one path will be taken into account at once.

As it is known that resistance is inversely proportional to MOSFET size (W/L).Total resistance of NMOS (pull down network) is Rn. So each NMOS' resistance is Rn/2 when two NMOS are connected in series. A decrease in resistance will result in an increase in NMOS size in the same proportion, making each NMOS in a pull-down network larger by 2x(W/L). Alternatively, resistance Rn equals size W/L, and resistance reduction equals size (W/L) increase. In worst case analysis we have to consider one path at a time. In each path one PMOS is present. So device size expected to be (W/L).

- Resistance of NMOS is Rn, size=> (**1W/L)**
- Resistance of PMOS is Rp, Size => (**2W/L**) because

$$\mu n = 2\,\mu p$$

In NAND gate considering worst sizing of each PMOS will be 2W/L.

(5B) K' Values

Sl No	Logic Gate	NMOS (Wn)	PMOS(Wp)	k'n	k'p	Vm
1	Inverter	1	2	12.162	3.921	0.51
2	NAND	2	2	6.081	3.921	0.51
3	NOR	1	4	12.162	1.96	0.45

Table 1.a

k'n and k'p values are as mentioned in the above table 1.a which can be calculated by using the below formula and method described below.

$$\mathbf{Id} = \frac{1}{2}\,\mathbf{K'\,(W/L)}(Vgs - Vt)^2$$

Id saturation values are used from the standard 'gpdk045' report found from the Moodle [gpdk045_PDK_Model_Report.pdf]

For NMOS:

Model Spec:

W(um)	L(um)	Vth	Idsat
10	10	0.36	9.01E-05
0.12	0.04	0.36	7.40E-05
10	0.04	0.38	5.96E-03
0.12	10	0.14	1.21E-06

Table 2.4 1.1v Standard Vt NMOS Model Spec

For PMOS:

Model Spec:

W(um)	L(um)	Vth	Idsat
10	10	-0.3	-6.48E-05
0.12	0.04	-0.4	-4.27E-05
10	0.04	-0.43	-3.06E-03
0.12	10	-0.22	-8.67E-07

Table 2.6 1.1v Standard Vt PMOS Model Spec

Calculation for Inverter:

Considering the values:

Wn = 1u, Wp = 2u, L=0.045u, Vgs = 1.1V, Vtn = 0.36V, Vtp = 0.4V

Substituting the above values in the ID (sat) formula yields the value of

As mentioned in table 1.a

K'n =12.162u and K'p=3.921u

(5C) Mid-Point Voltage:

Inverter:

$$V_M = \frac{VDD - |V_{tp}| + V_{tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

Where

$$\frac{\beta_n}{\beta_p} = \frac{k'_n\left(\frac{W}{L}\right)_n}{k'_p\left(\frac{W}{L}\right)_p}$$

Considering the values:

Wn = 1u, Wp = 2u, L = 0.045u, Vgs = Vdd = 1.1V, Vtn = 0.36V, Vtp = 0.4V

Substituting the above values in the above mentioned Vm values yields the value

As mentioned in table 1.a

Vm = 0.511V

NAND GATE:

For N-inputs

$$V_M = \frac{VDD - |V_{tp}| + V_{tn}\frac{1}{N}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \frac{1}{N}\sqrt{\frac{\beta_n}{\beta_p}}}$$

Where

$$\frac{\beta_n}{\beta_p} = \frac{k'_n\left(\frac{W}{L}\right)_n}{k'_p\left(\frac{W}{L}\right)_p}$$

NOR GATE:

For N- inputs

$$V_M = \frac{VDD - |V_{tp}| + NV_{tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + N\sqrt{\frac{\beta_n}{\beta_p}}}$$

Where

$$\frac{\beta_n}{\beta_p} = \frac{k'_n\left(\frac{W}{L}\right)_n}{k'_p\left(\frac{W}{L}\right)_p}$$

Similar to inverter calculation NAND and NOR values are calculated and captured the observation in table 1.a

(5D) Rise and fall time of Logic Gates

Rise time fall time we got from Cadence calculator.

Sl no	Logic Gate	Rise Time(ps)	Fall Time(ps)	Capacitance (fF)
1	Inverter	10.341	11.21	0.5733
2	2- Input NAND	10.125	10.76	0.489
3	2- Input NOR	11.01	10.51	0.305

Table 1.b

(5E) Parasitic Capacitance

Cout values can be found from the Trise and Tfall values and are captured in the table 1.b

The time constant is related to parameter of the RC circuit.

$$\tau = RC$$

$$t_r = 2.2\,\tau_p$$

$$t_f = 2.2\,\tau_n$$

$$Rn = 1/[\beta_n(V_{DD}-Vtn)]$$

$$Rp = 1/[\beta_n(V_{DD}-|Vtp|)]$$

Considering the "Inverter" for the following values

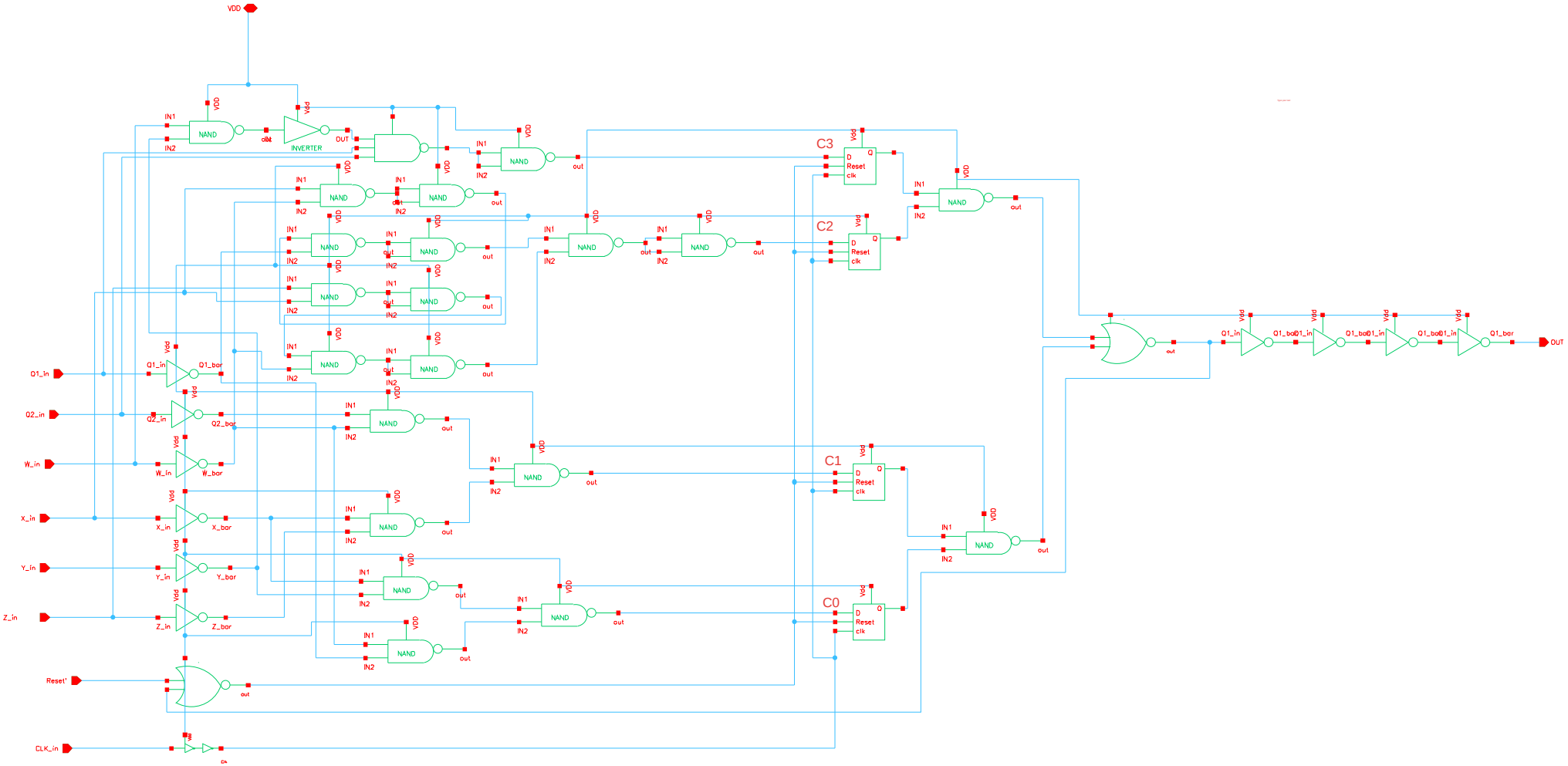
Tr = 10.341ps, β=174.24, Vdd = 1.1V, Vtp=0.4V

Substituting the values in the above equation yields the value of capacitor as mentioned in the table. Similarly the value is calculated for NOR and NAND and captured in the table.

GATE LEVEL SCHEMATIC OF DESIGN

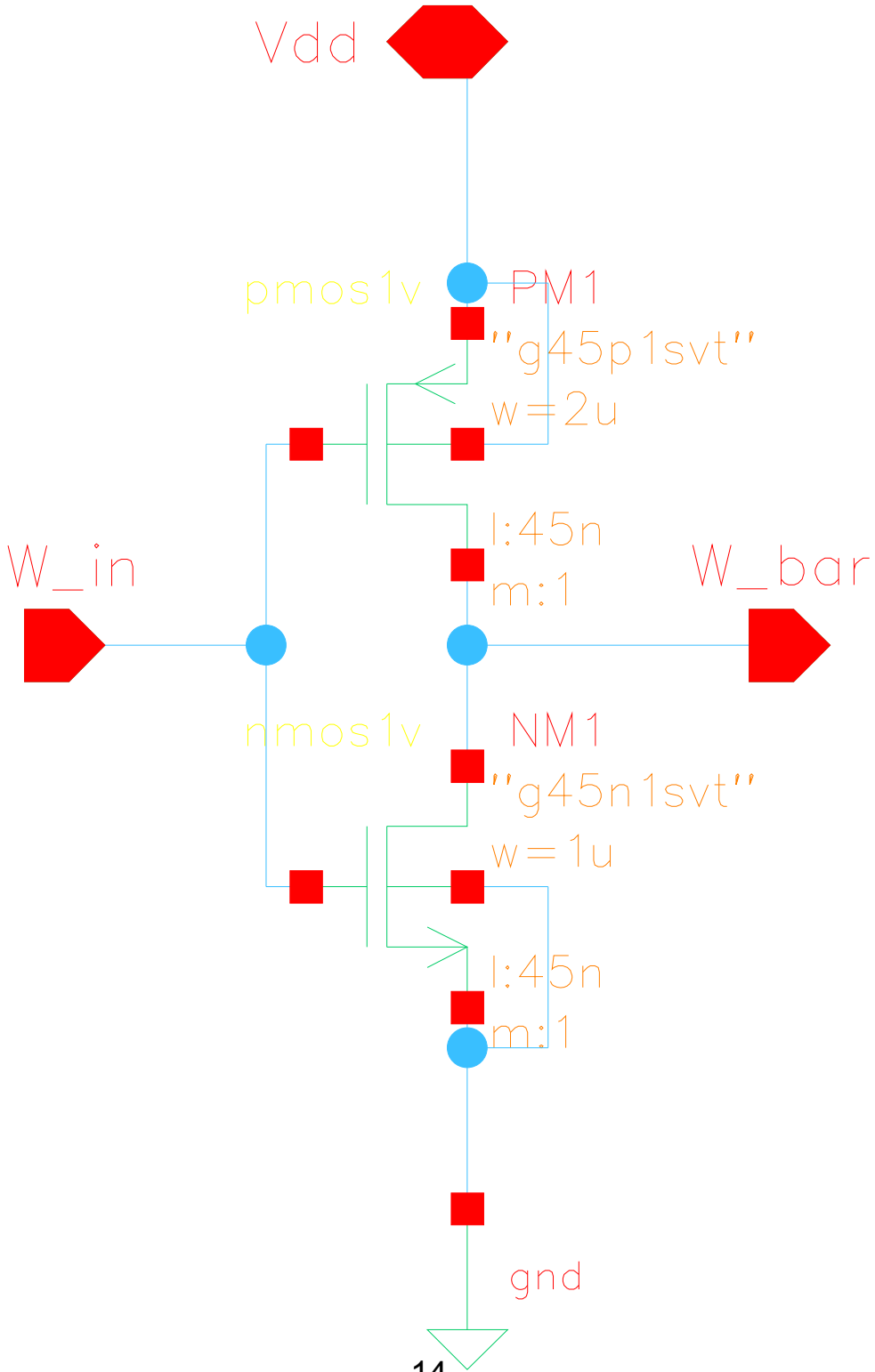
Submitted by:
Anusha S
Neha Gour

GATE LEVEL SCHEMATIC



TRANSISTOR LEVEL SCHEMATIC OF LOGIC GATES

Submitted by:
Anusha S
Neha Gour



Submitted by:
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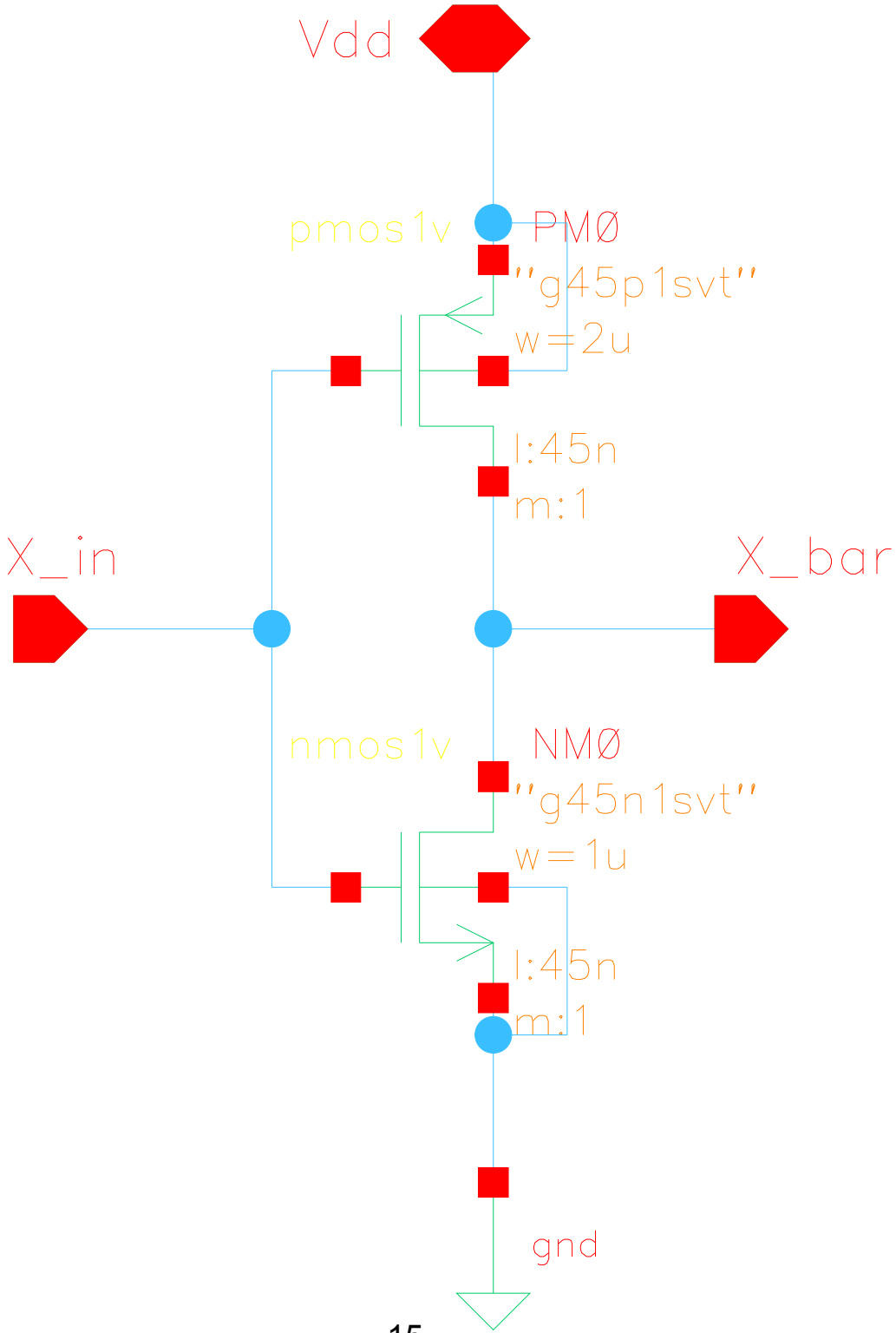
Neha Gour



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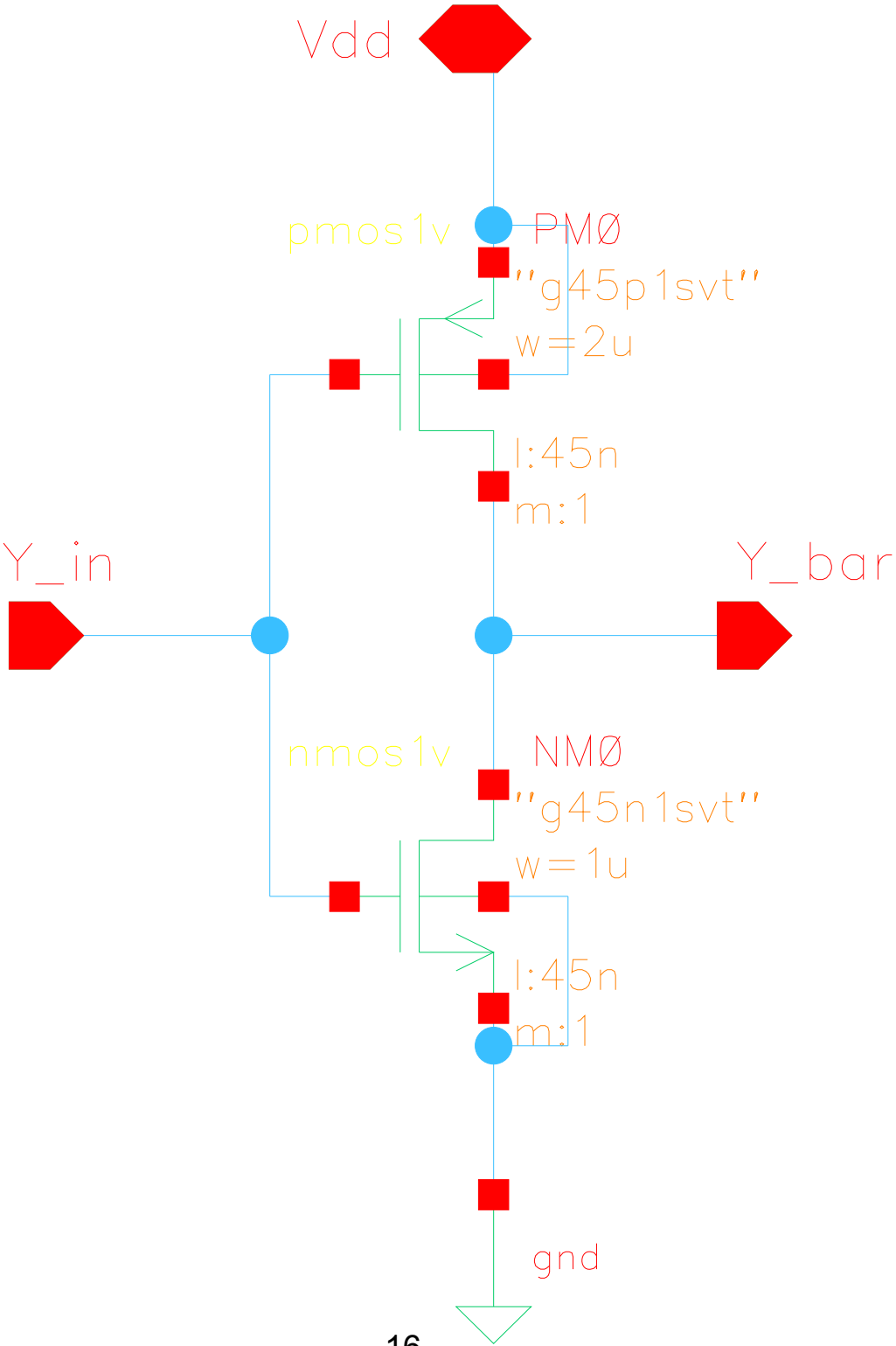
Anusha S
Neha Gour



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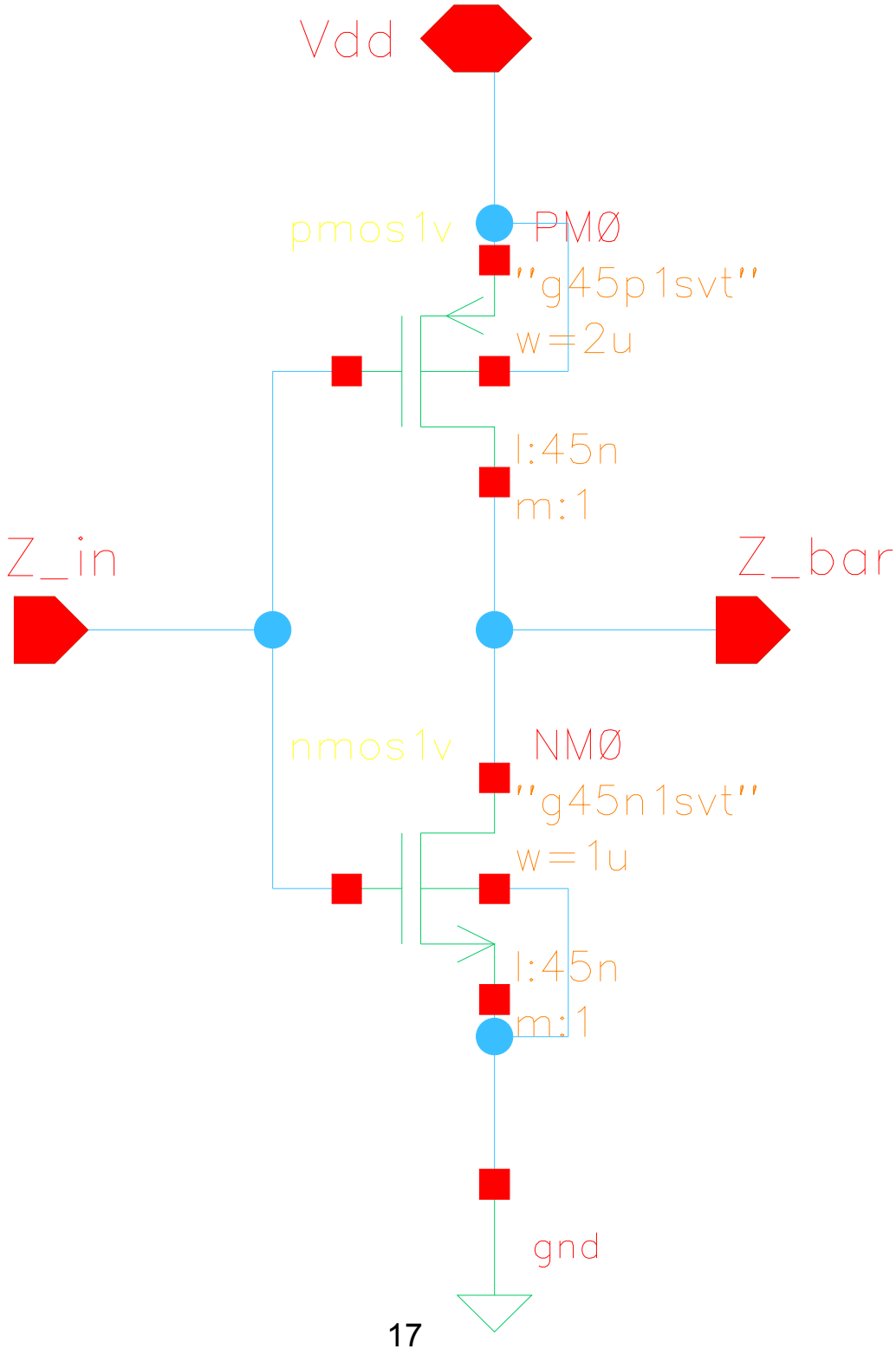
Anusha S
Neha Gour



Submitted by:
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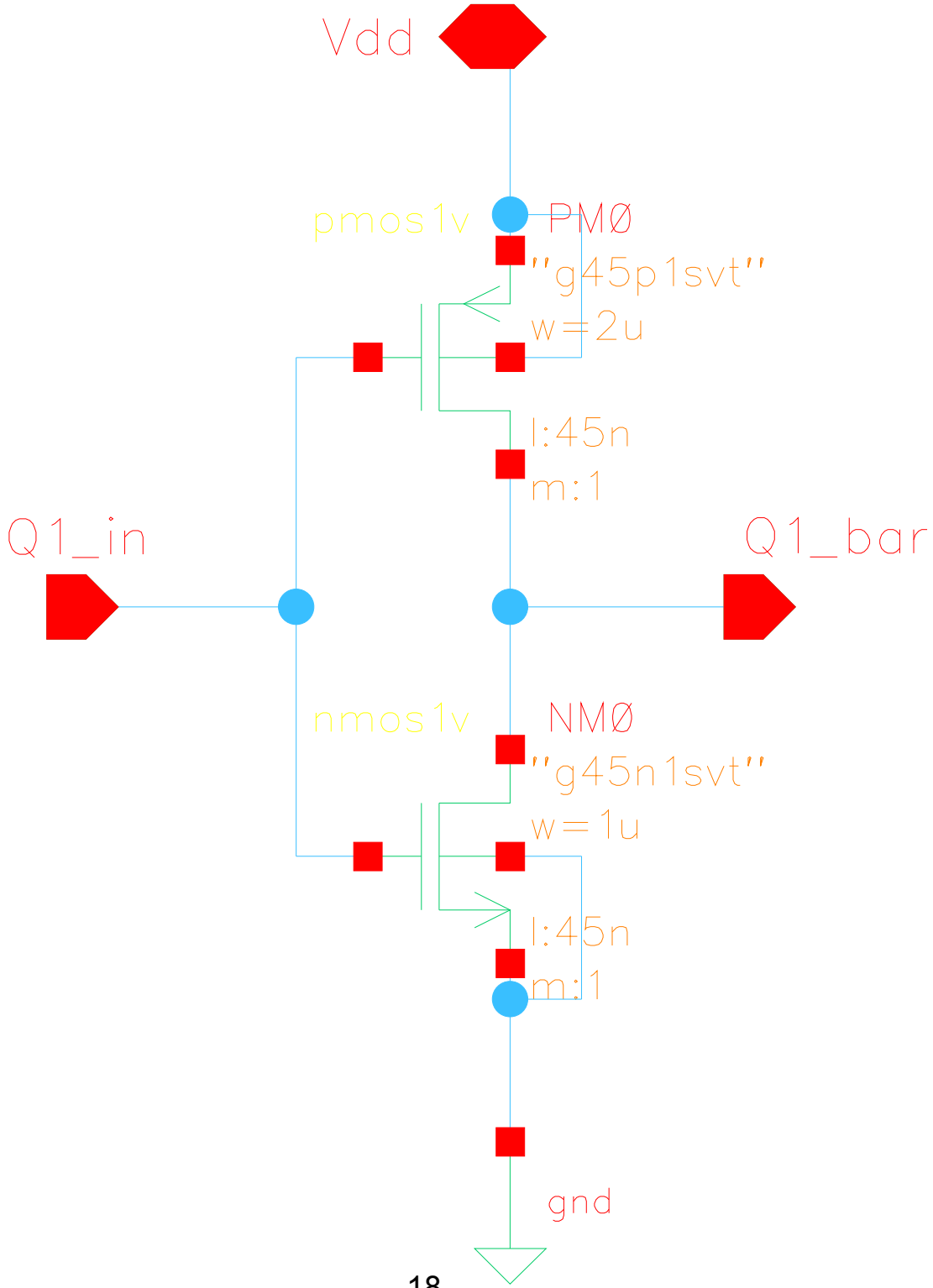

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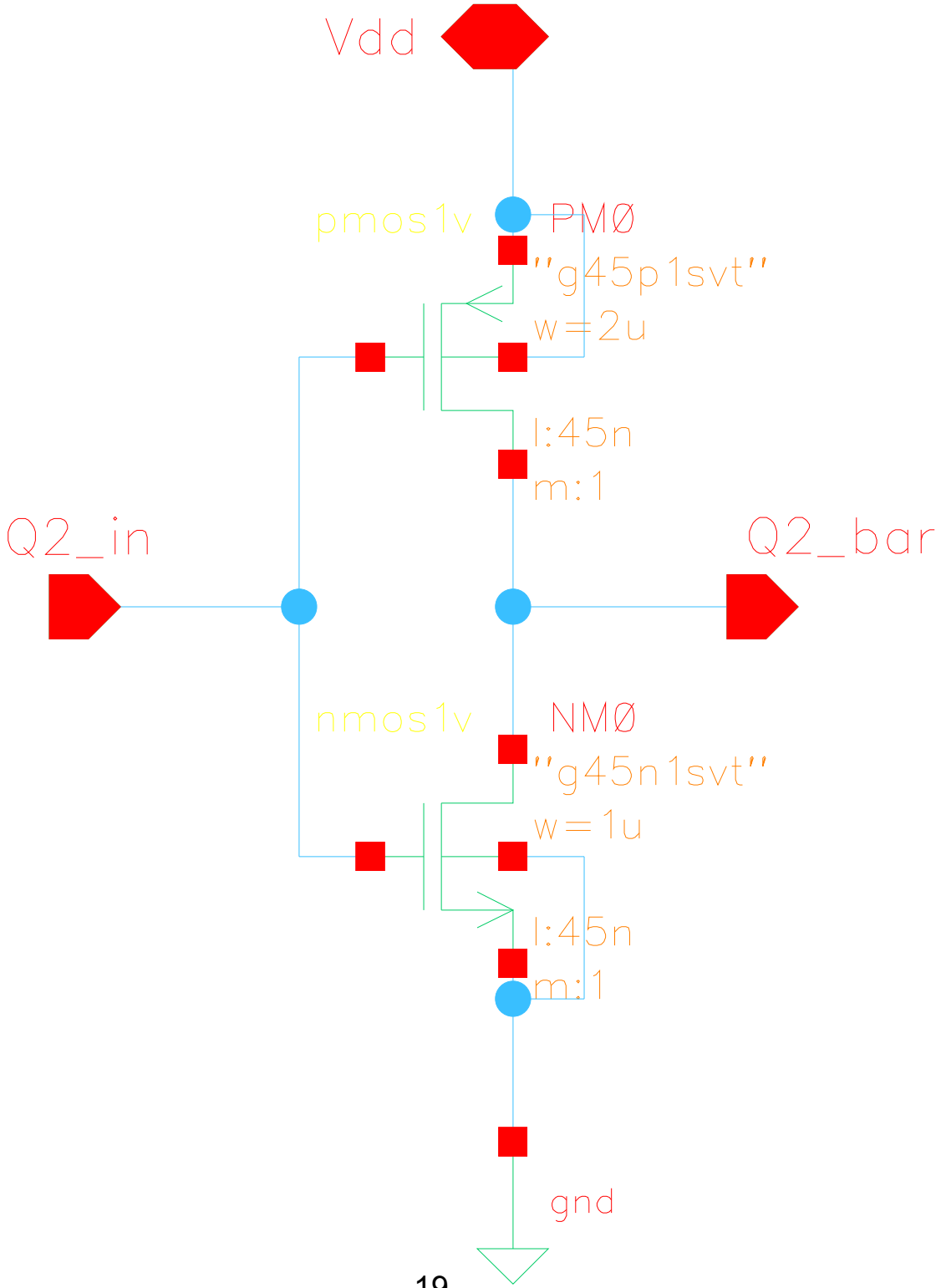

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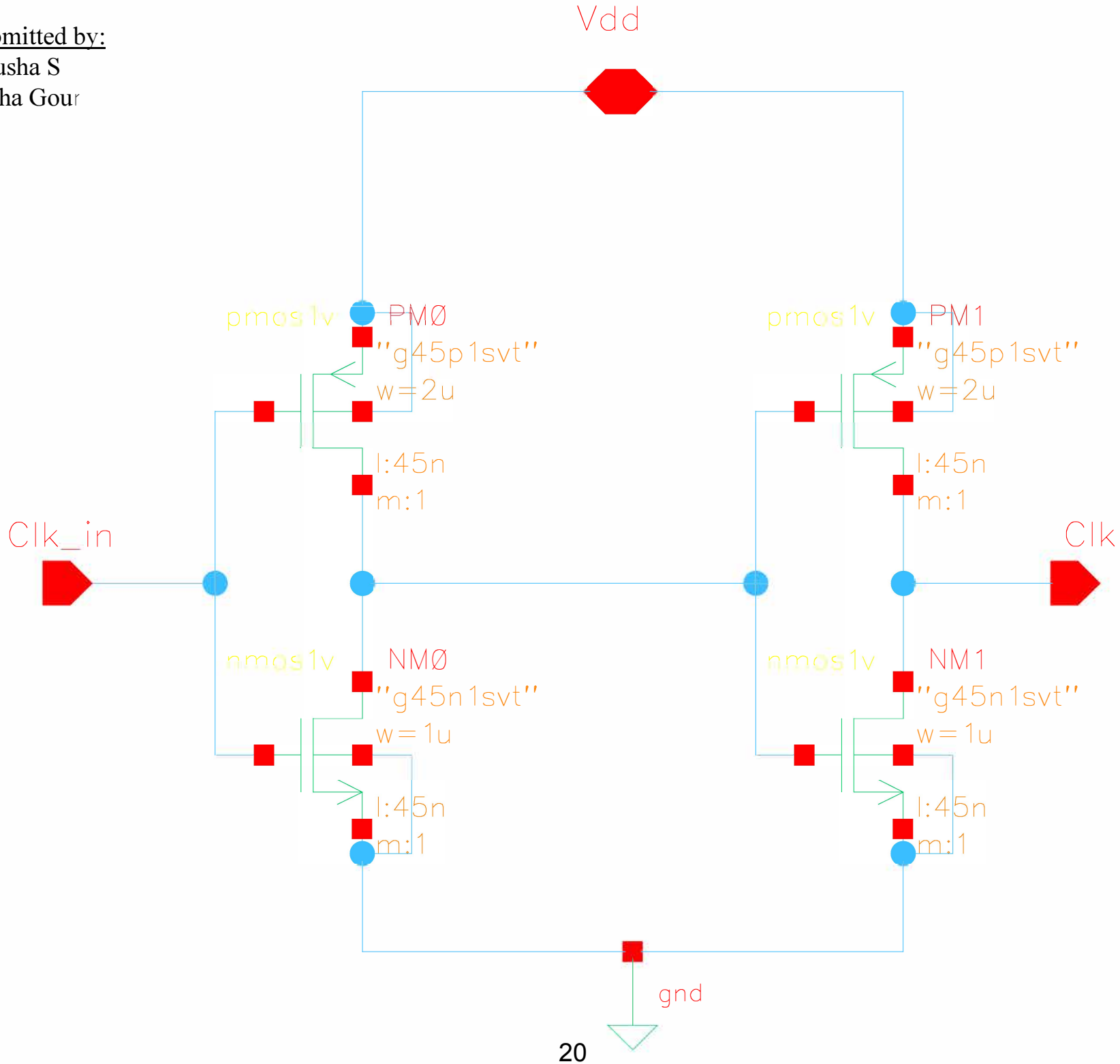

Submitted by:
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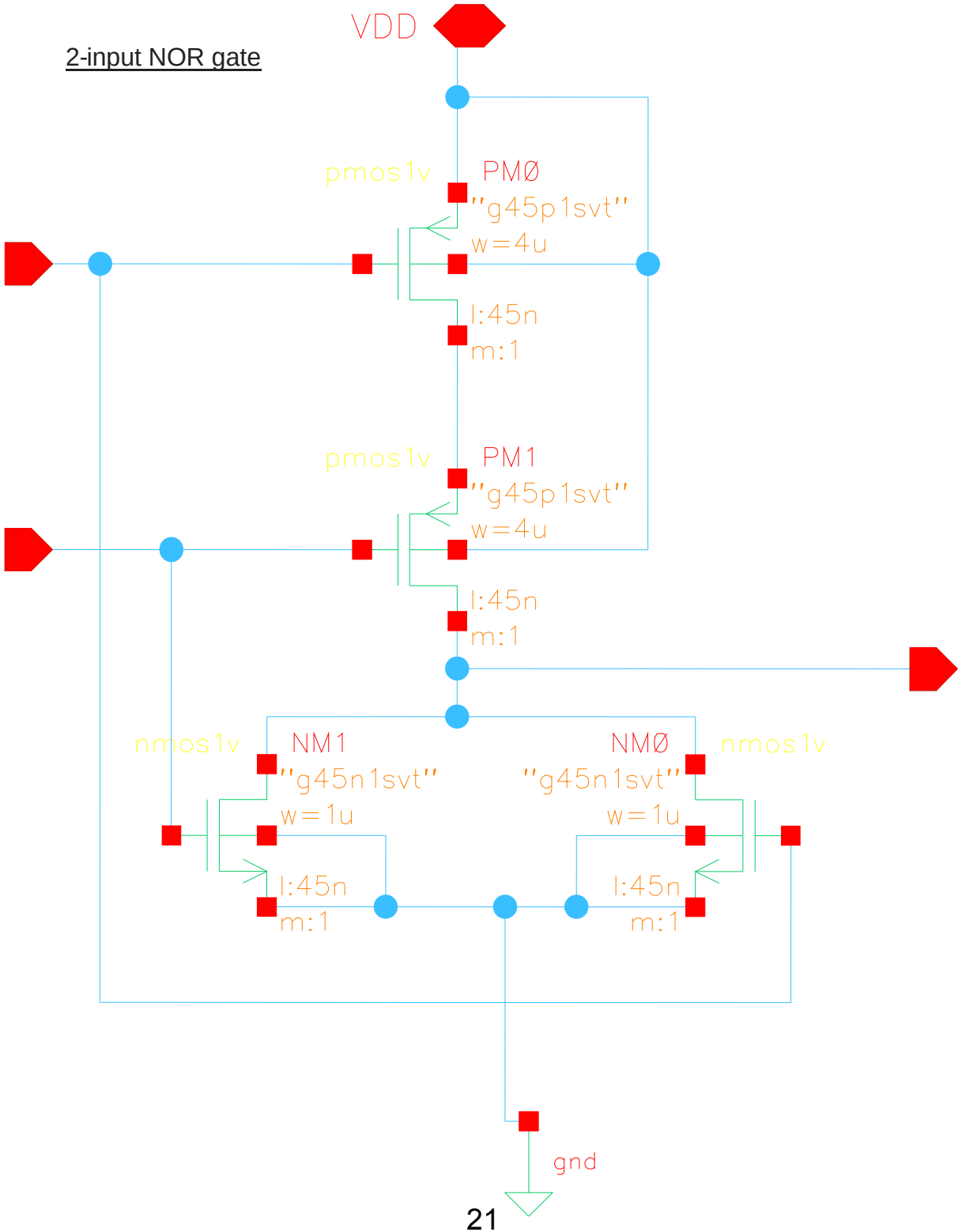
2-input NOR gate



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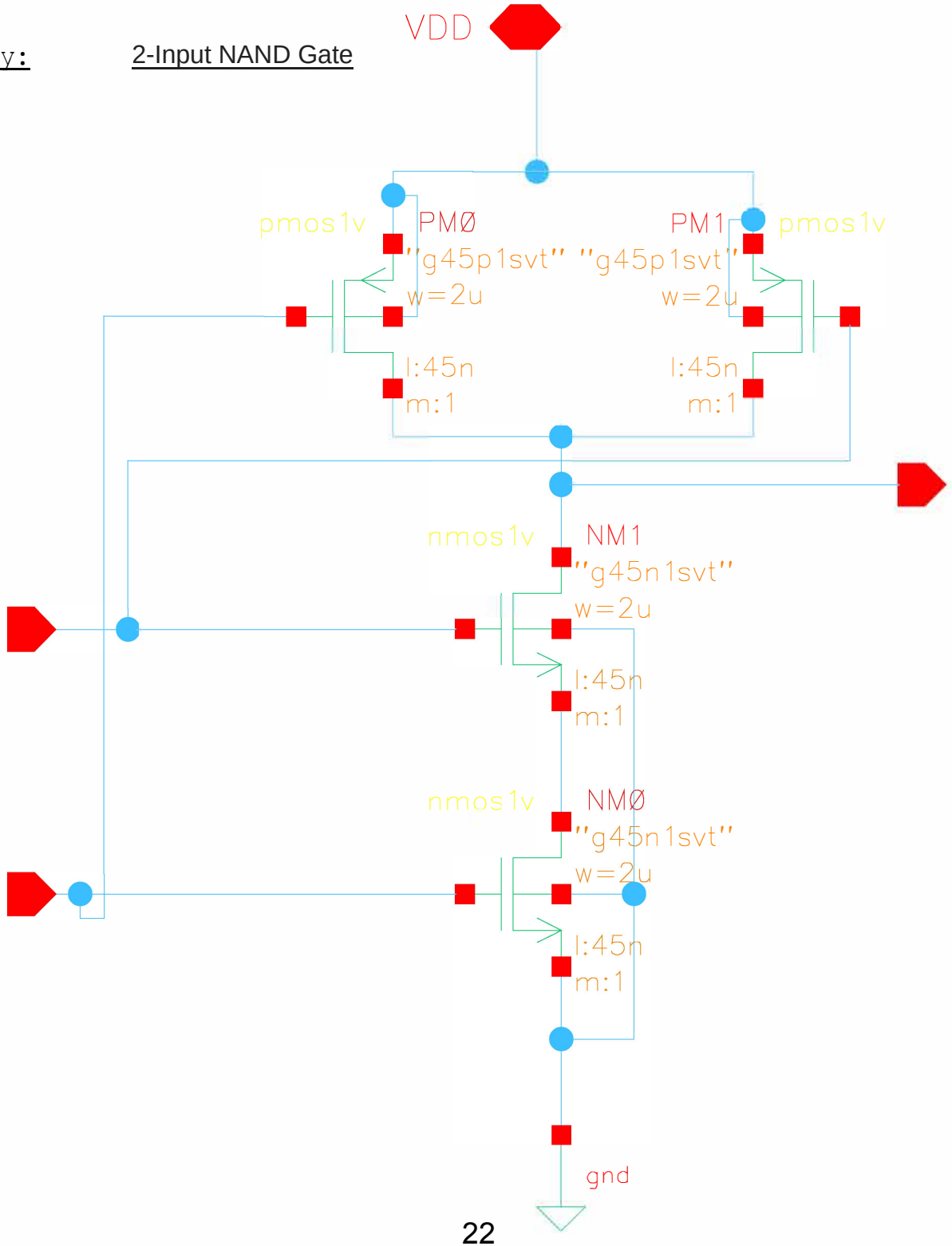
2-Input NAND Gate



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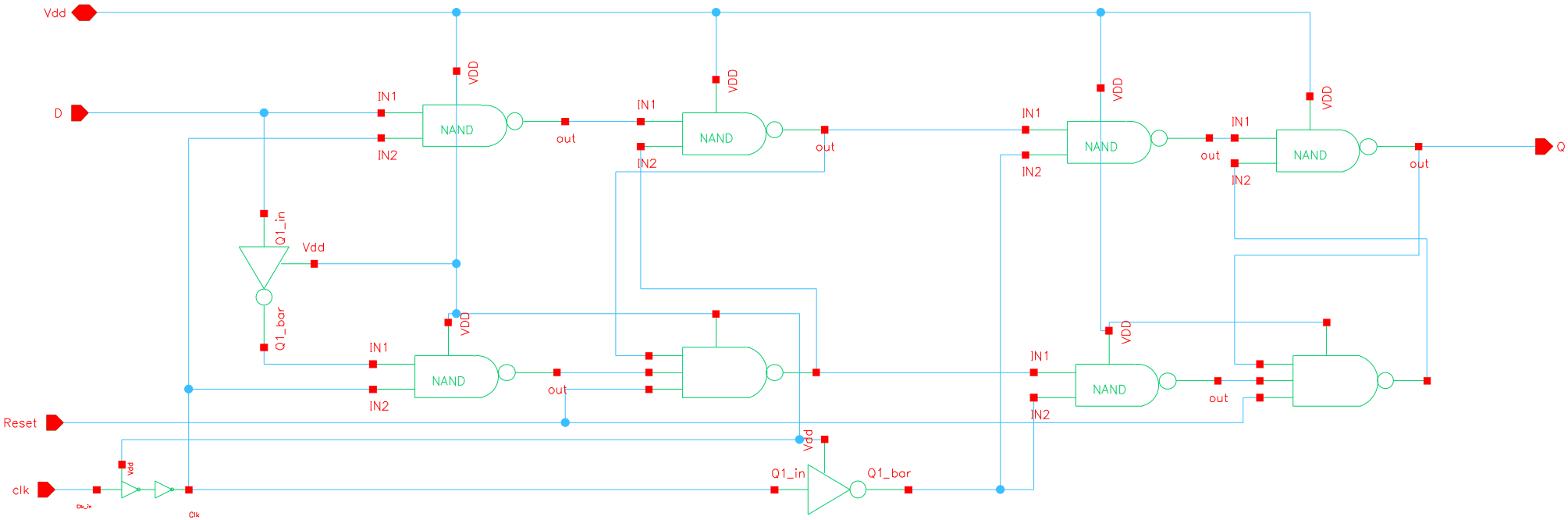
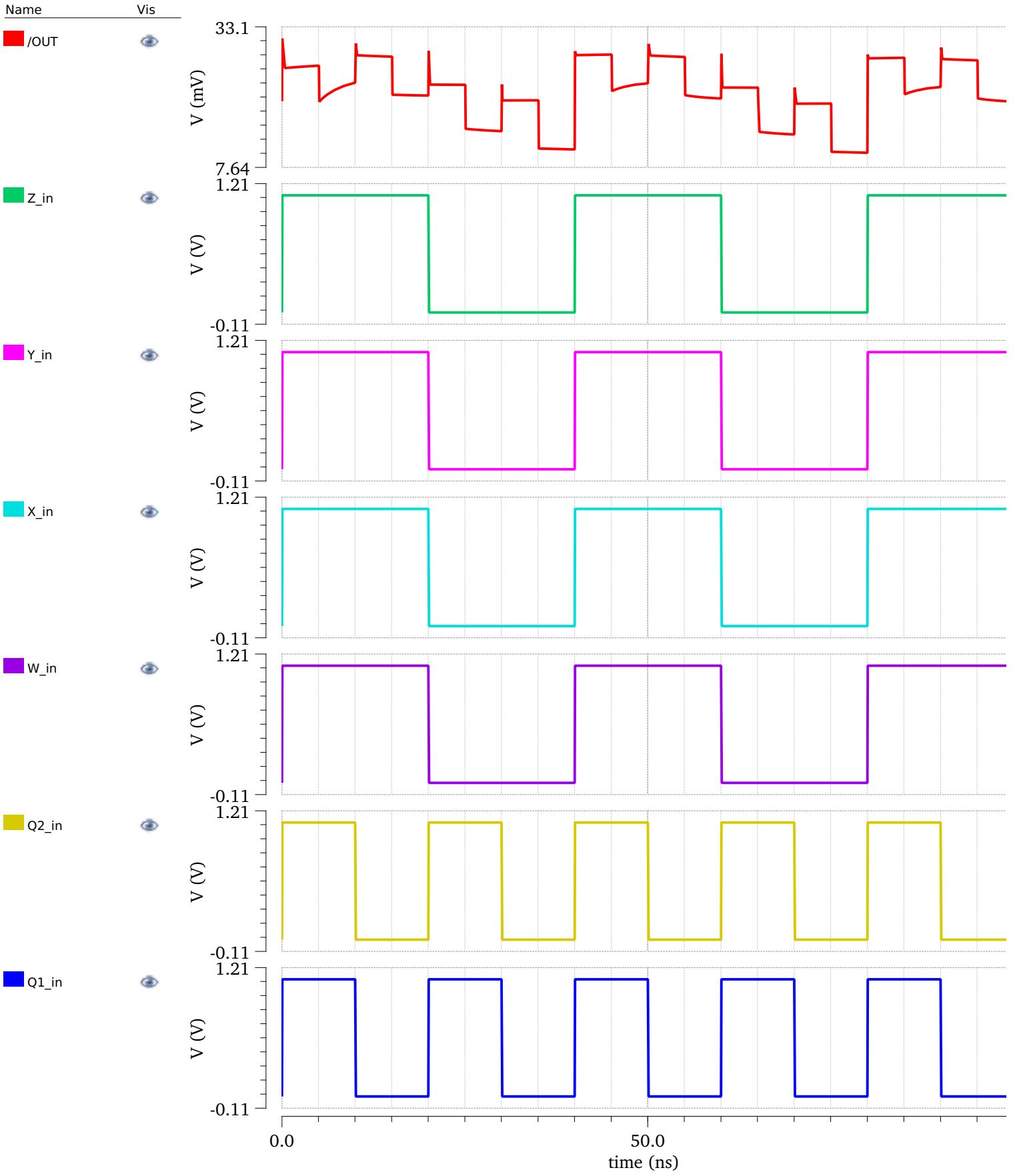
D-Flip Flop

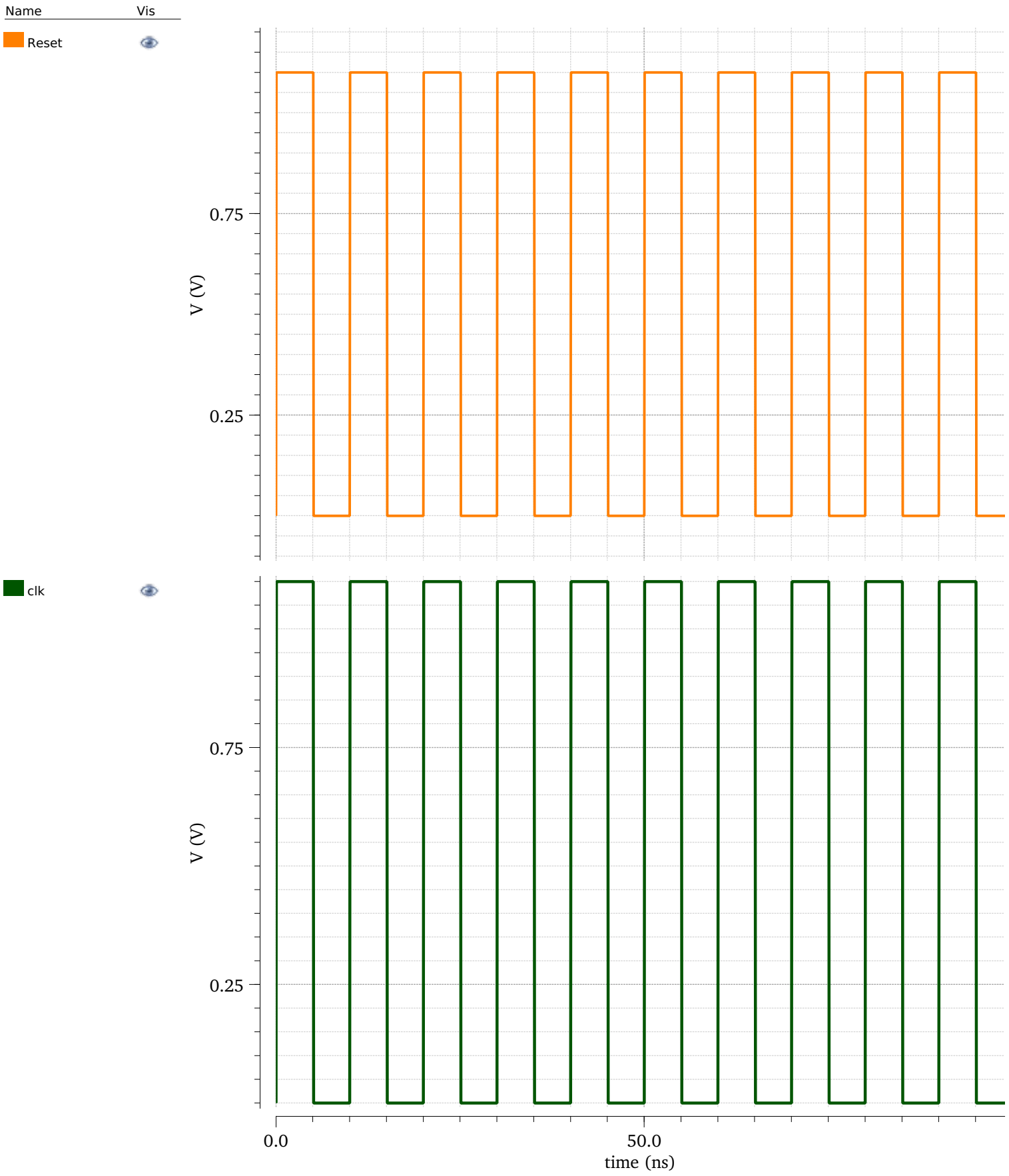


SIMULATION RESULTS OF DESIGN

Transient Response **Fri Nov 11 21:55:53 2022**



Transient Response **Fri Nov 11 21:55:53 2022**



FLOORPLAN OF DESIGN

Floorplan

Submitted by:
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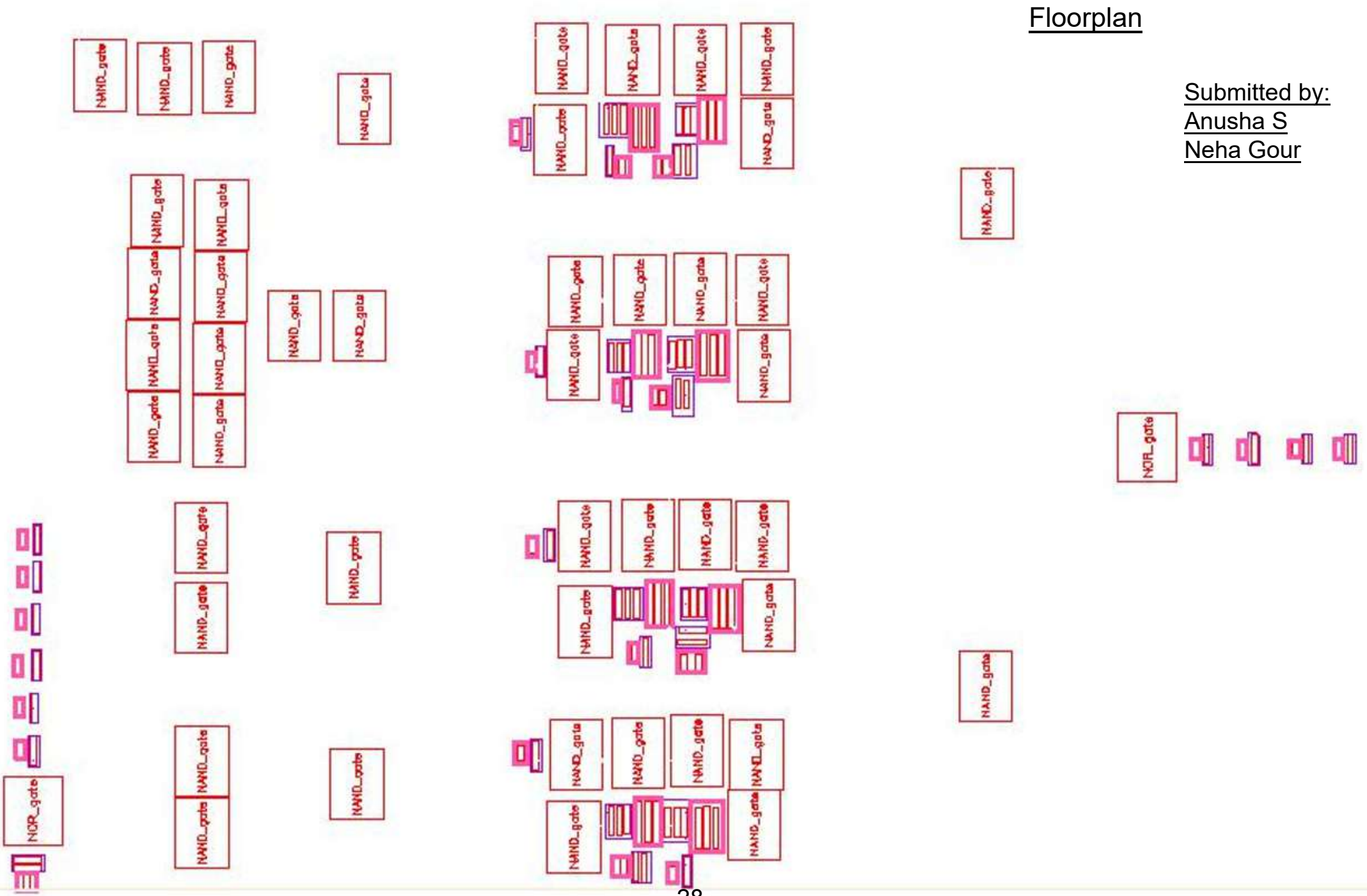

Results and Conclusion:

Phase 1 of this project taught us how to design, simulate, and create a floor plan using 45nm library for digital vending machine.
We also did sizing of MOSFETs and computed the W/L, k', mid-point voltage, rise and fall times, and parasitic capacitance values for every logic gate.
In Virtuoso, we created transistor level schematic for logic gates and simulated to check the functionality. Master-Slave D flip-flop is created by logic gates. Gate level schematic is designed and simulated to fulfil the design specifications. We have constructed floorplan of the design, which is an essential step to manage circuit design complexity such as minimizing the delay and chip area.
We worked together to set goals as a team and to achieve deadlines considering it was a team project.

Sl No	Logic Gate	NMOS (Wn)	PMOS (Wp)	k'n (µA/V^2)	k'p (µA/V^2)	Vm (V)	Rise Time(ps)	Fall Time(ps)	Capacitance (fF)
1	Inverter	1 um	2 um	12.162	3.921	0.51	10.341	11.21	0.5733
2	2-NAND	2 um	2 um	6.081	3.921	0.51	10.125	10.76	0.489
3	2-NOR	1 um	4 um	12.162	1.96	0.45	11.01	10.51	0.305