1. Design, Simulate and Layout of Inverter Use: (W/L)n = 1.0/0.045 and (W/L)p = 2.0/0.045

Inverter: Inverter is a logic circuit which generates the compliment or inverse of the logic input.

Equation:

IN = IN'

where, IN : logic input of inverter
IN' : output of inverter.

In this schematic, input IN is the input and OUT is the inverted output using positive logic.

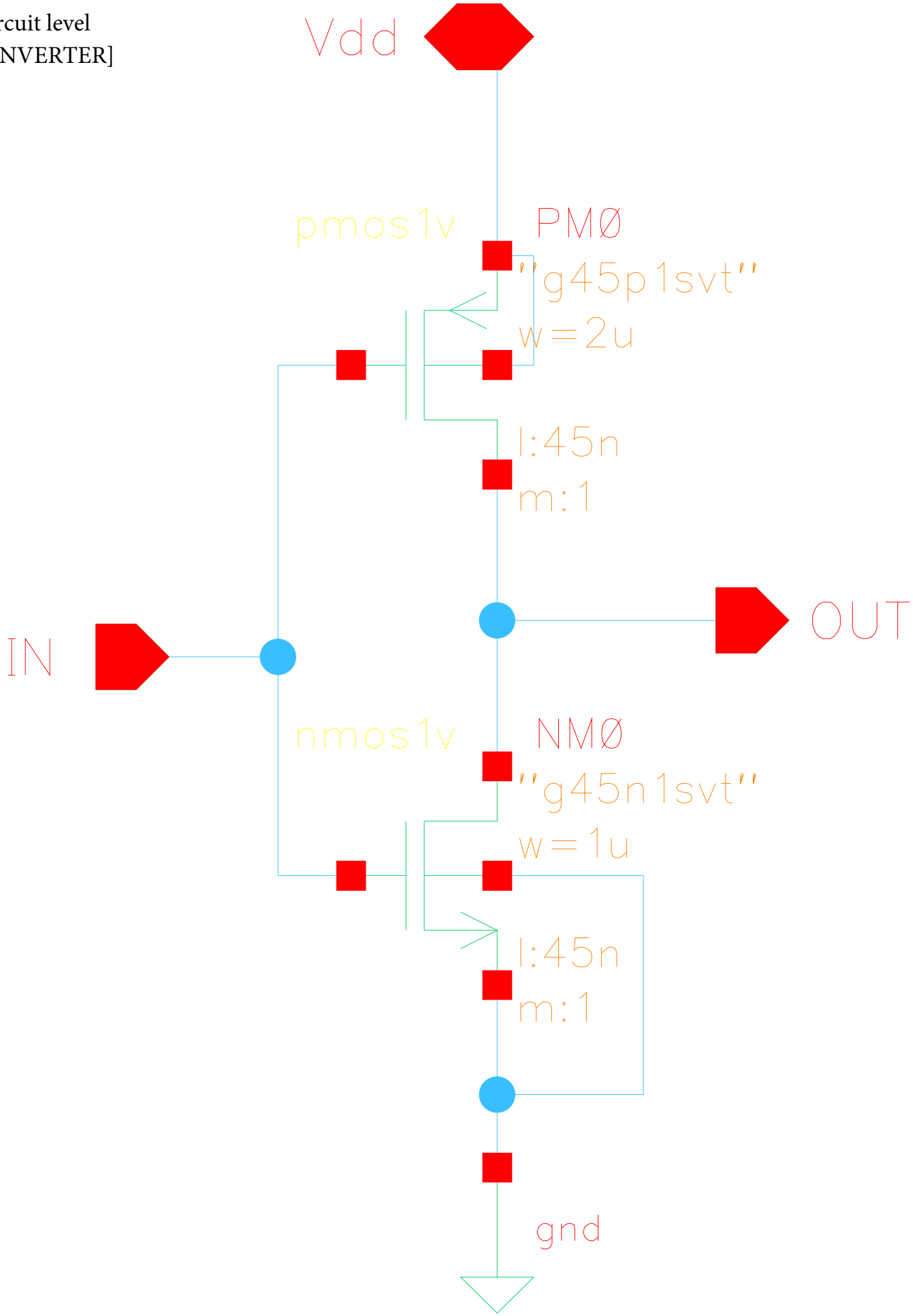
Truth table:

IN	OUT
0	1
1	0

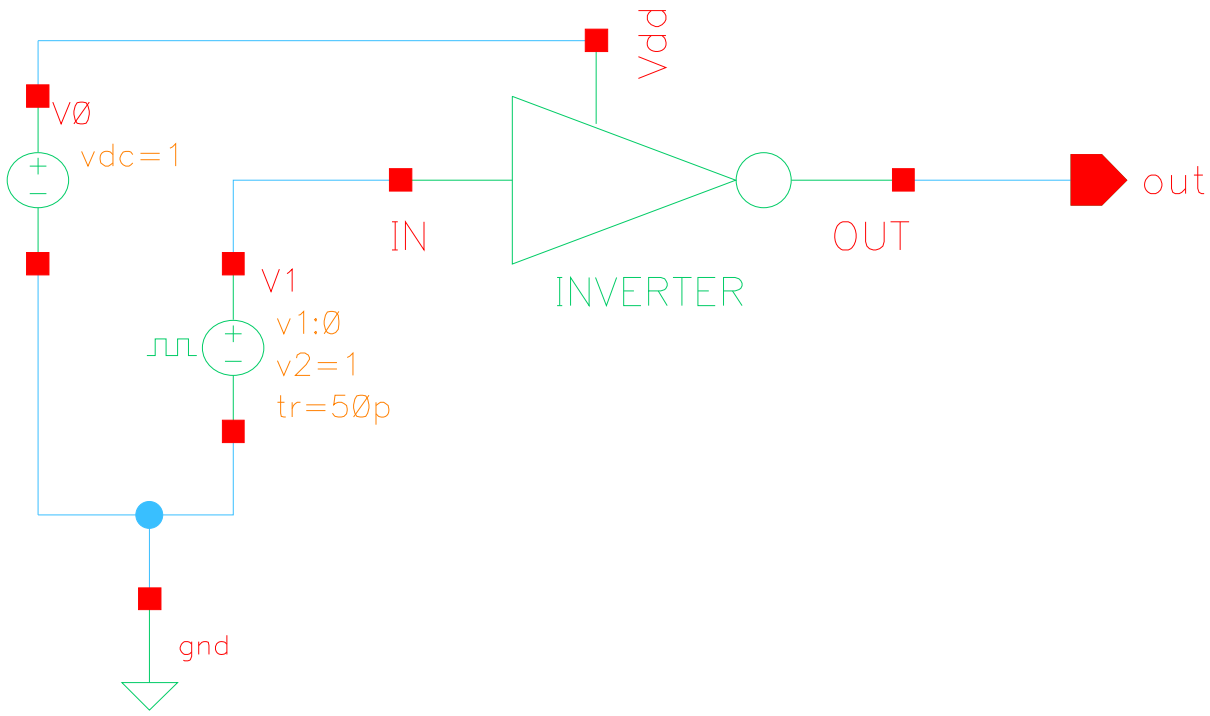
Results obtained from CMOS inverter circuit:

Rise time: t_{rise} = 10.341ps
Fall time t_{fall} = 11.22ps
Input-output delay time = 14.11ps

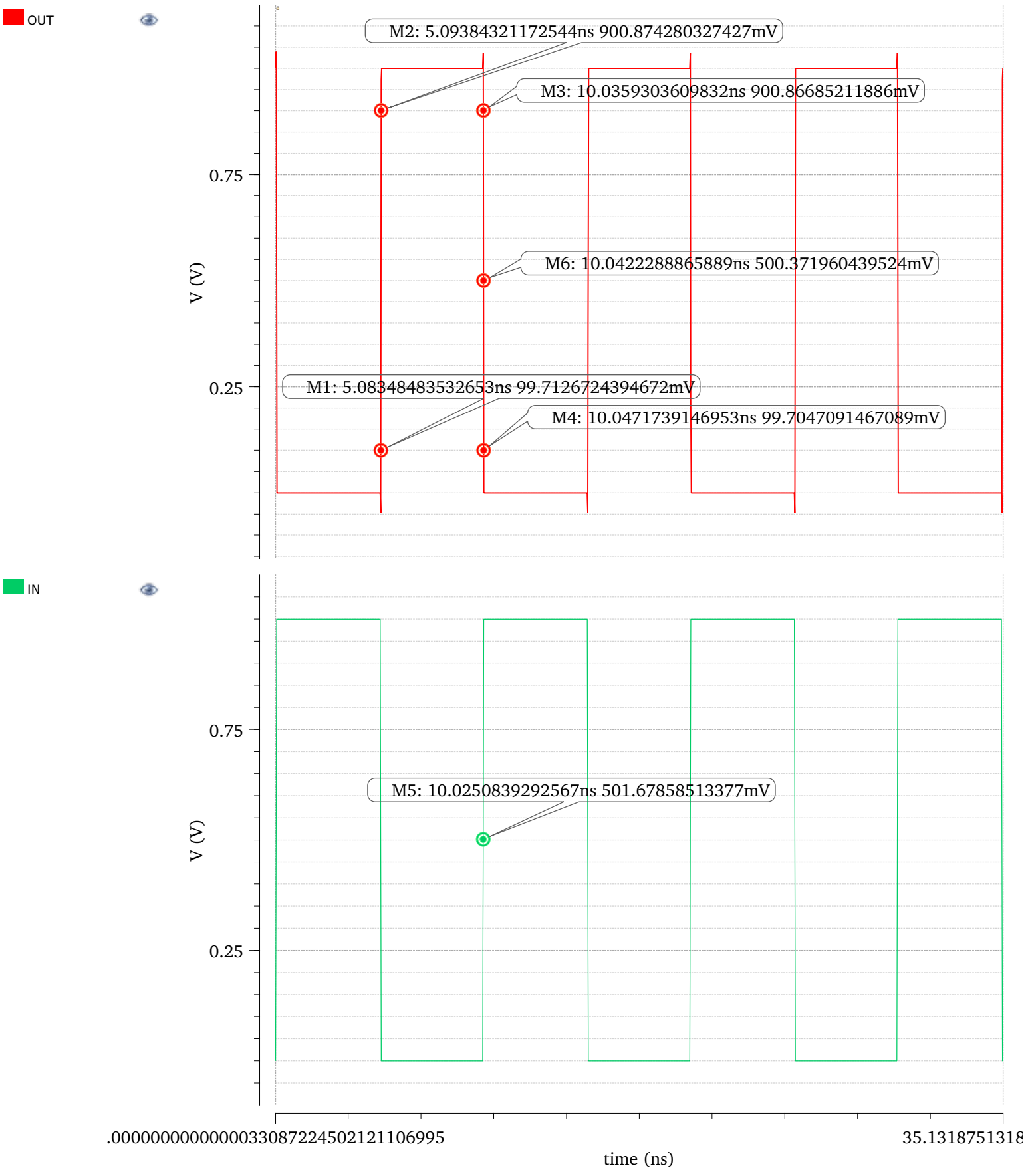
Circuit level
[INVERTER]



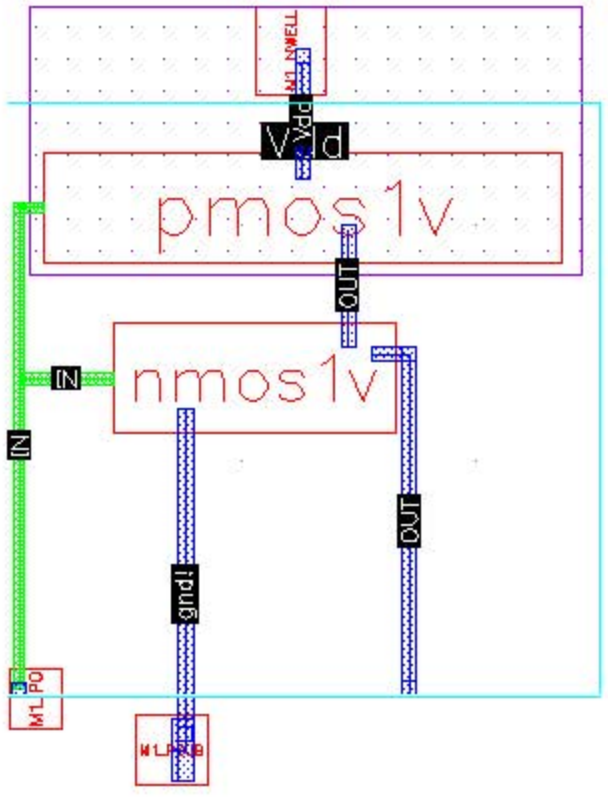
Schematic
[INVERTER]



Transient Response **Wed Oct 12 23:16:10 2022**



Layout [INVERTER]



```
Host is
cmd  is /opt/cadence/ASSURA41/tools.lnx86/assura/bin/assura /home/student/nehagour/library/Inverter.rsf -cdslib /home/student/nehagour/library/cds.lib -restart -gui
Starting the Assura DRC Run: IPC Id ipc:10: pid 20488.
Checking out license for "Assura_UI"
Checking out license for "Phys_Ver_Sys_Results_Mgr"
*WARNING* No DRC errors found.

Loading tech rule set file : /opt/pdk/gpdk045_v_6_0/assura/techRuleSets

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display full path...

Loading tech rule set file : /opt/pdk/gpdk045_v_6_0/assura/techRuleSets
Assura LVS: State loaded "Last"
*INFO*: Checking whether schematic is up to date.
*INFO*: Schematic integrity check is completed.
Assura LVS: State saved "Last"
Host is
cmd  is /opt/cadence/ASSURA41/tools.lnx86/assura/bin/assura /home/student/nehagour/library/Inverter.rsf -cdslib /home/student/nehagour/library/cds.lib -gui
Starting the Assura LVS Run: IPC Id ipc:11: pid 22149.
STATUS: Schematic and Layout Match
```

2. Design, Simulate and Layout of 2-input NAND gate Use: (W/L)n = 2.0/0.045 and (W/L)p = 2.0/0.045

Nand gate: It is a combination of two basic logic gates the AND gate and the NOT gate connected in series.

Equation:

(IN1.IN2)' = OUT

where, IN1, IN2 : 2 inputs of nand gate
OUT: Output of nand gate.

In this schematic, input IN1,IN2 are the inputs and OUT is the output using positive logic.

Truth table:

IN1	IN2	OUT
0	0	1
0	1	1
1	0	1
1	1	0

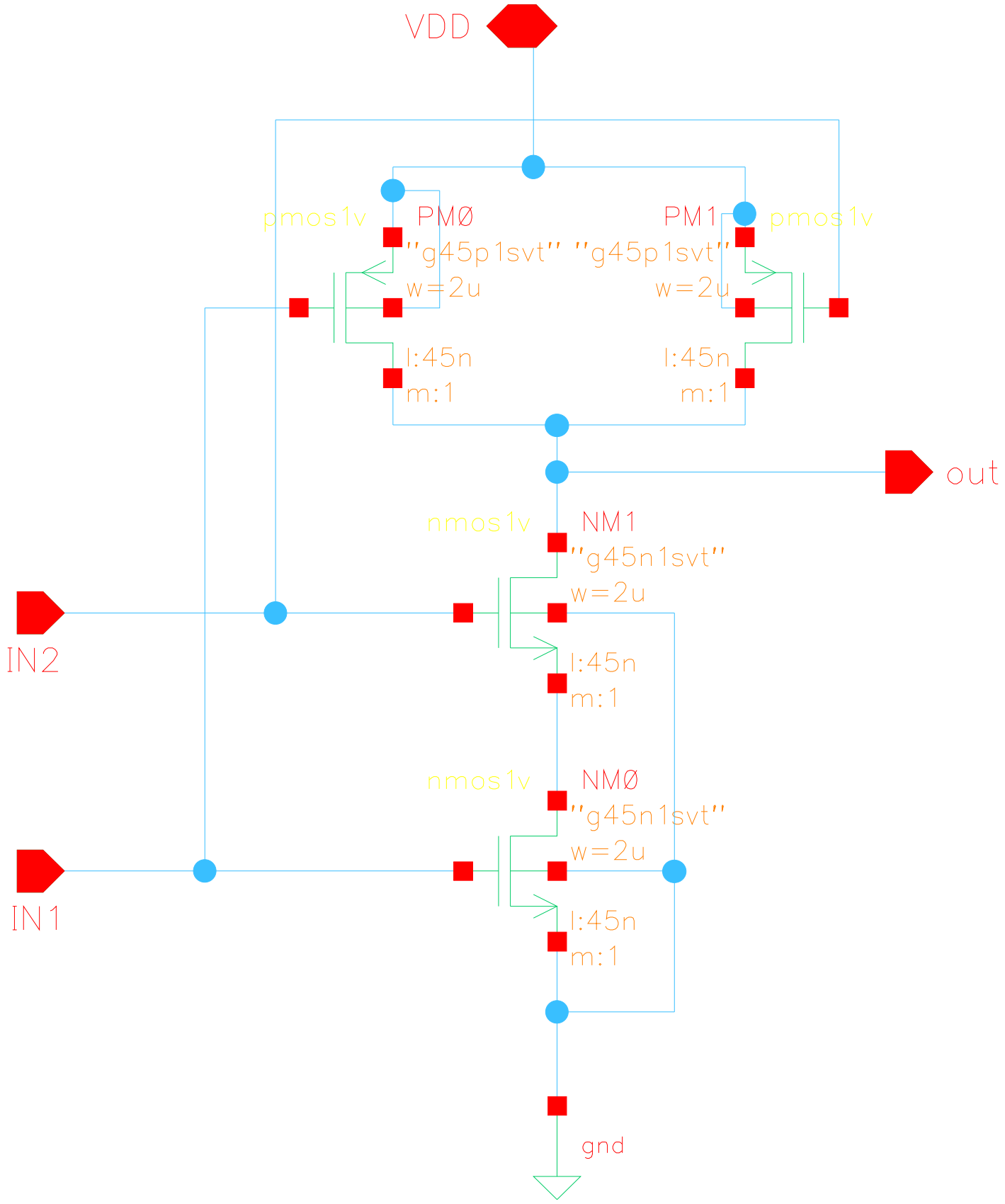
"if both IN1 and IN2 are true, then OUT is NOT true"

Results obtained from circuit:

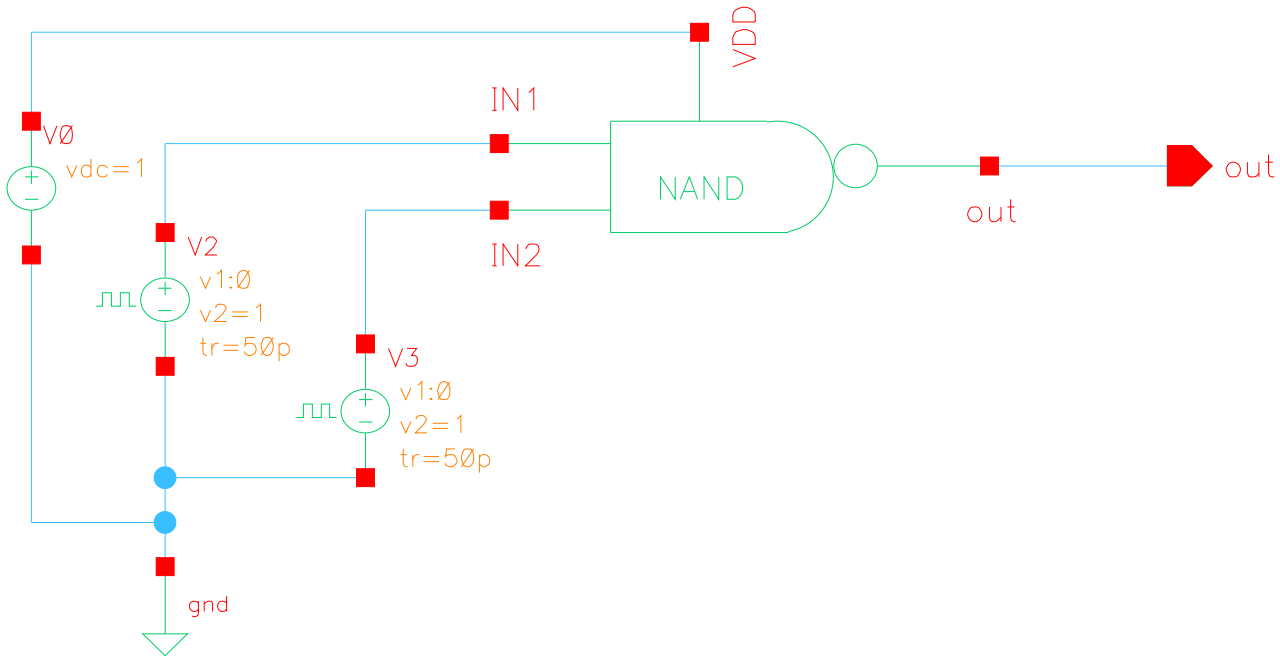
Risetime:=10.10ps
Falltime:=14.30ps
Input-output delay time = 25.11ps

Circuit level

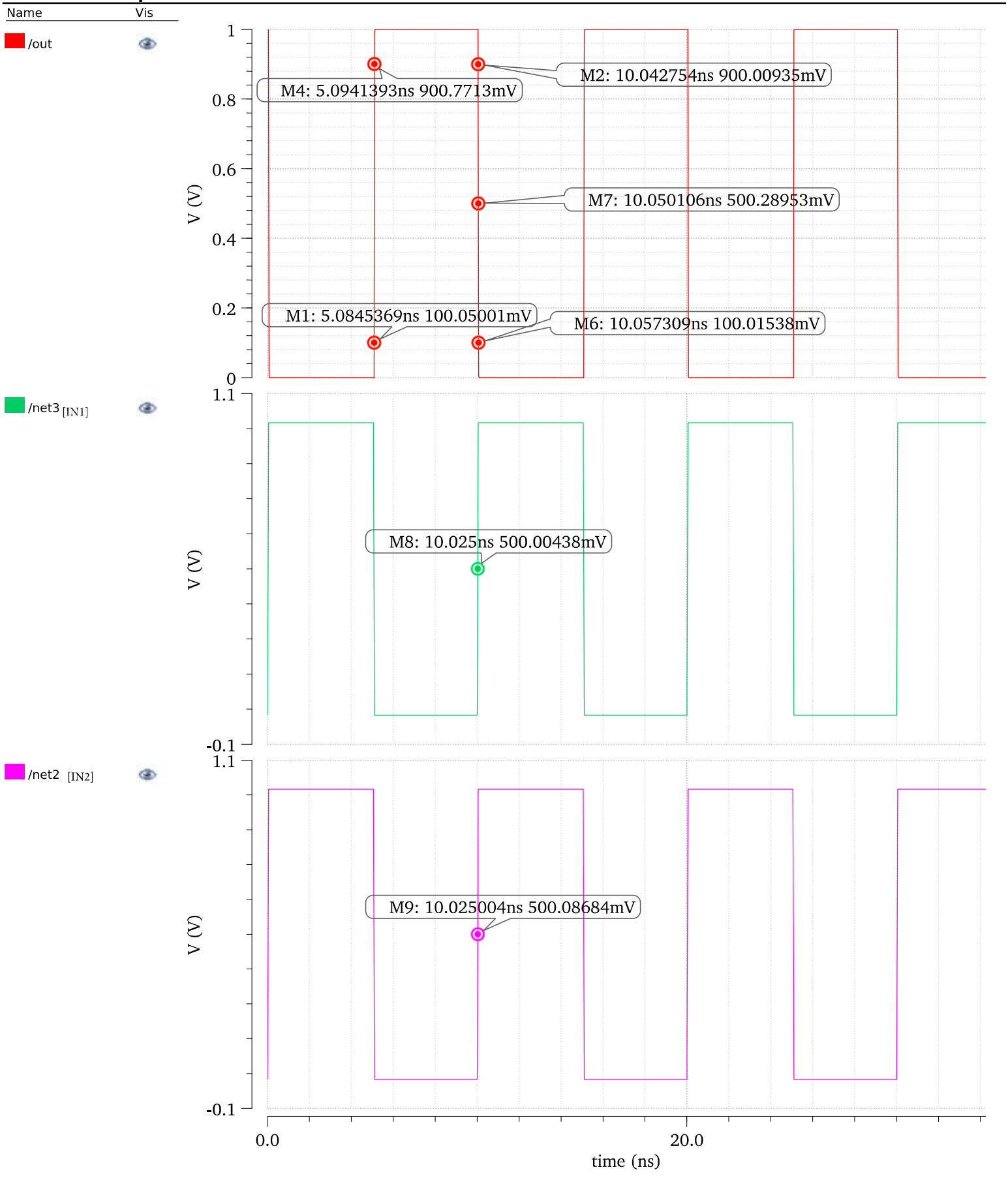
[2-input NAND gate]



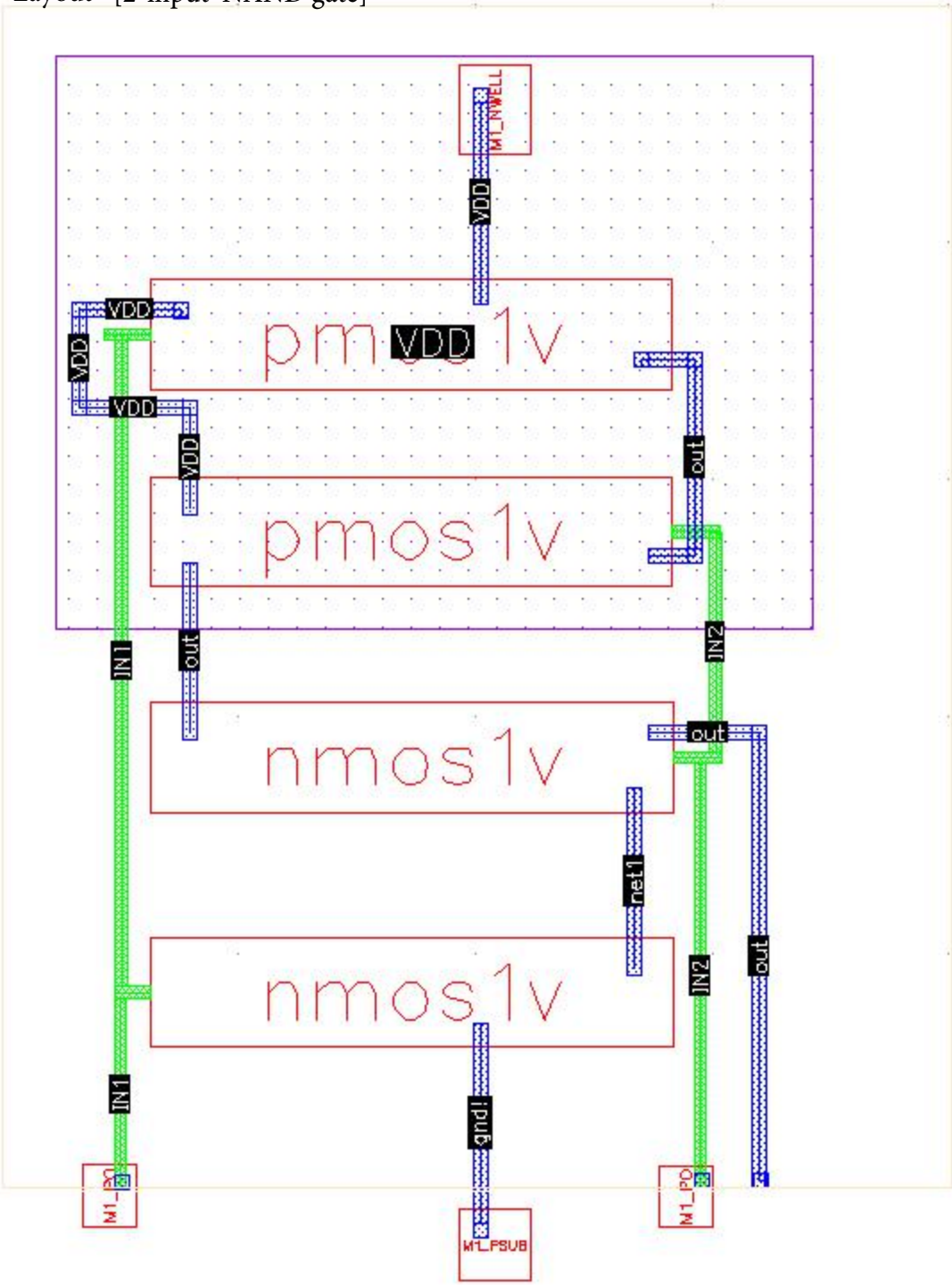
Schematic [2-input NAND gate]



Transient Response **Thu Oct 13 00:25:21 2022**



Layout [2-input NAND gate]



```
Host is
cmd  is /opt/cadence/ASSURA41/tools.lnx86/assura/bin/assura /home/student/nehagour/library/NAND_gate.rsf -cdslib /home/student/nehagour/library/cds.lib -restart -gui
Starting the Assura DRC Run: IPC Id ipc:15: pid 16245.
Checking out license for "Assura_UI"
Checking out license for "Phys_Ver_Sys_Results_Mgr"
*WARNING* No DRC errors found.

Loading tech rule set file : /opt/pdk/gpdk045_v_6_0/assura/techRuleSets

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Loading tech rule set file : /opt/pdk/gpdk045_v_6_0/assura/techRuleSets
display full path...

Loading tech rule set file : /opt/pdk/gpdk045_v_6_0/assura/techRuleSets
Assura LVS: State loaded "Last"
*INFO*: Checking whether schematic is up to date.
*INFO*: Schematic integrity check is completed.
Assura LVS: State saved "Last"
Host is
cmd  is /opt/cadence/ASSURA41/tools.lnx86/assura/bin/assura /home/student/nehagour/library/NAND_gate.rsf -cdslib /home/student/nehagour/library/cds.lib -gui
Starting the Assura LVS Run: IPC Id ipc:16: pid 17192.
STATUS: Schematic and Layout Match
```

3. Design, Simulate and Layout of 2-input NOR gate Use: (W/L)n = 1.0/0.045 and (W/L)p = 4.0/0.045

Nor gate: It is a combination of OR gate and the NOT gate connected in parallel.

Equation:

(IN1 + IN2)' = OUT

where, IN1, IN2 : 2 inputs of NOR gate
OUT: Output of NOR gate.

In this schematic, input IN1, IN2 are the inputs and OUT is the output using positive logic.

Truth table:

IN1	IN2	OUT
0	0	1
0	1	0
1	0	0
1	1	0

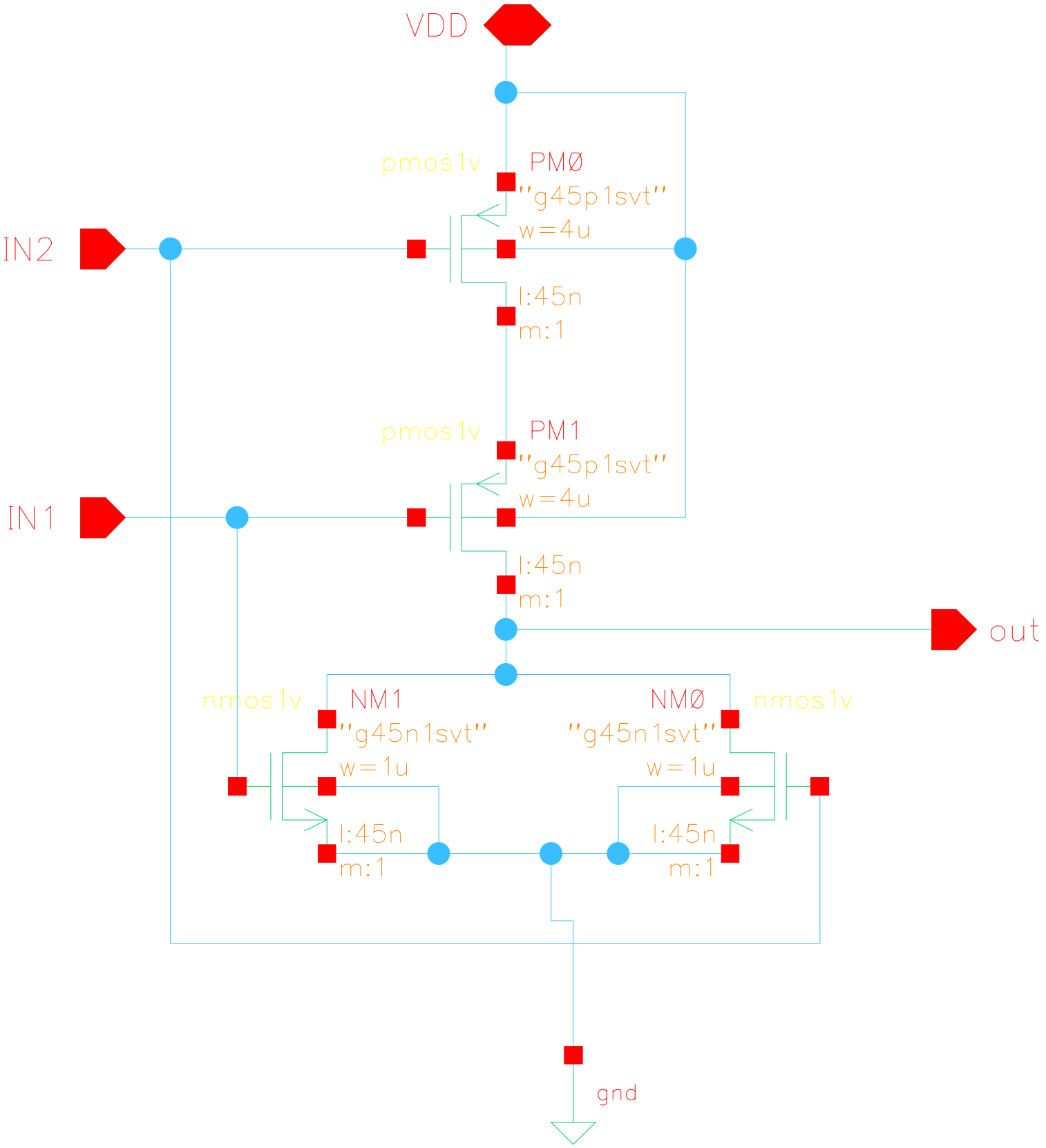
"if both IN1 and IN2 are NOT true, then OUT is true"

Results obtained from circuit:

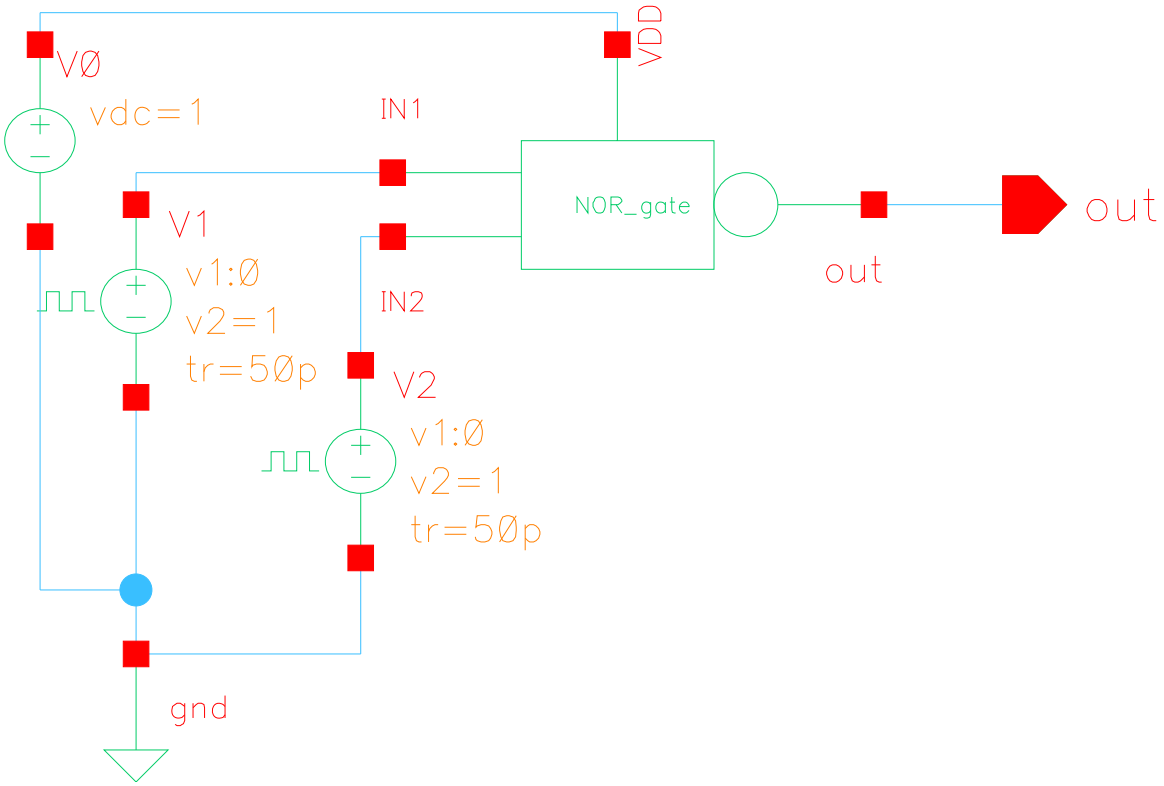
Rise time: t_{rise} = 15.81ps
Fall time t_{fall} = 10.08ps
Input-output delay time = 17.87ps

Circuit level

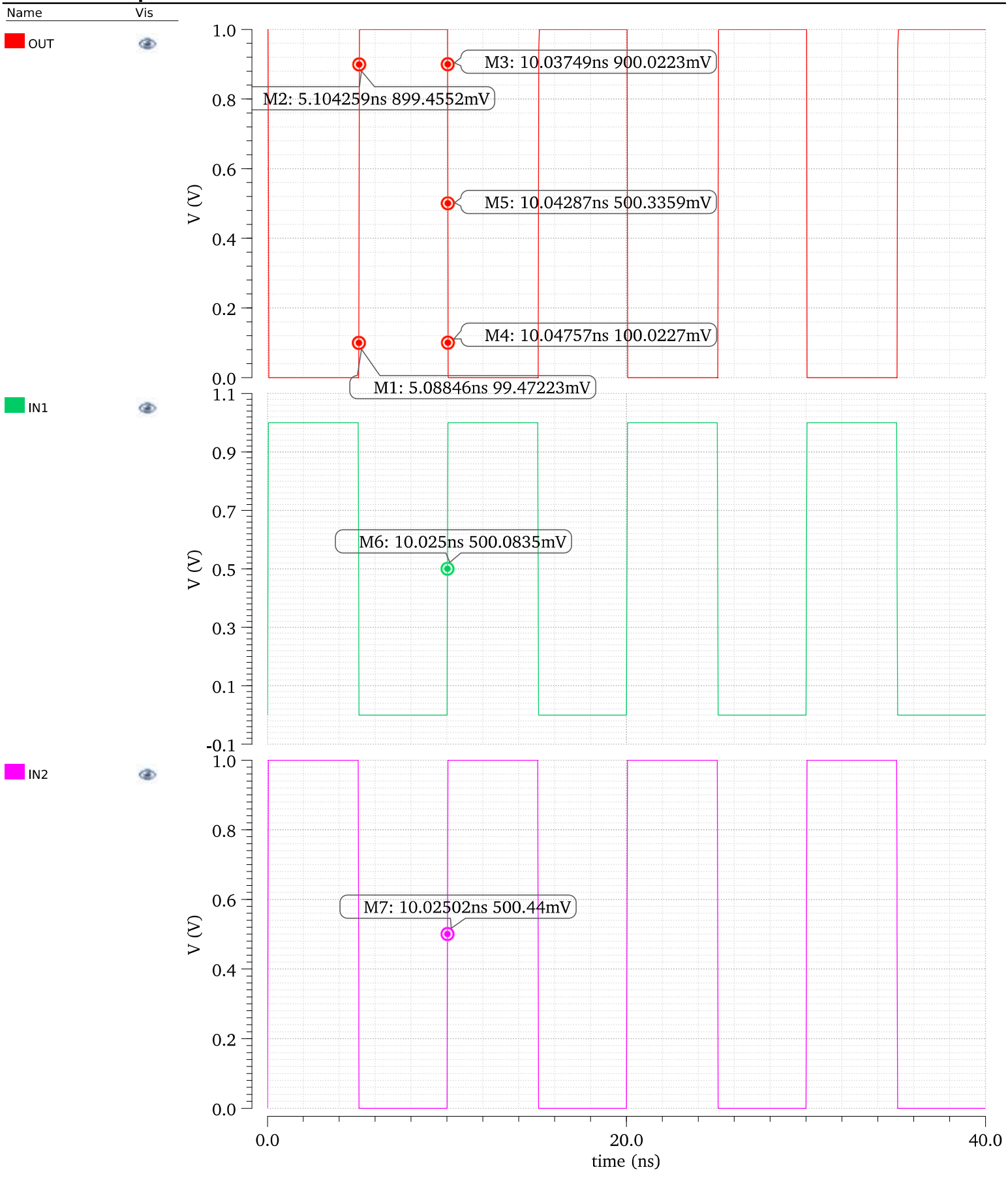
[2-input NOR gate]



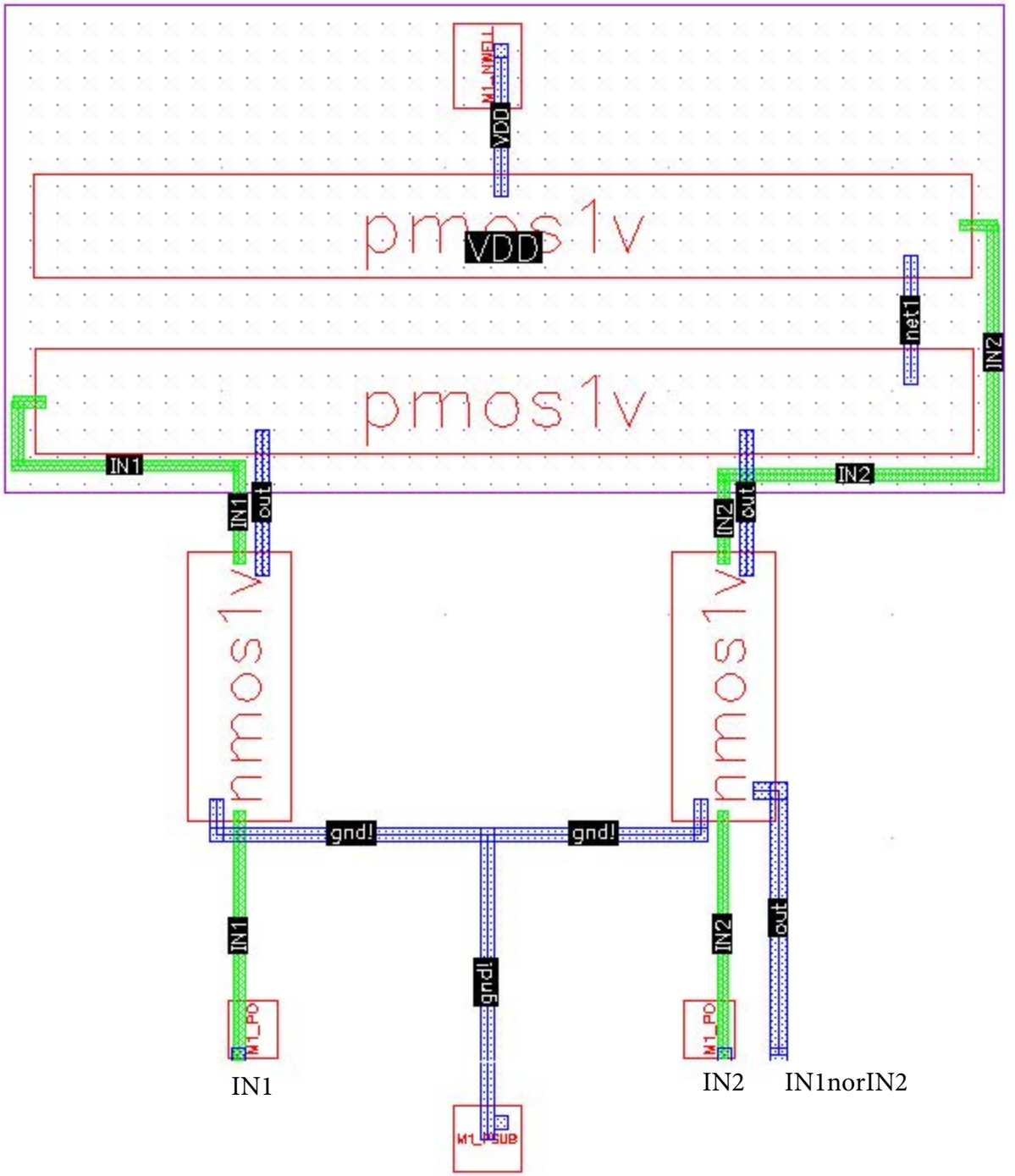
Schematic
[2-input NOR gate]



Transient Response **Thu Oct 13 01:42:33 2022**



Layout [2-input NOR gate]



```
Host is
cmd  is /opt/cadence/ASSURA41/tools.lnx86/assura/bin/assura /home/student/nehagour/library/NOR_gate.rsf -cdslib /home/student/nehagour/library/cds.lib -restart -gui
Starting the Assura DRC Run: IPC Id ipc:53: pid 28371.
Checking out license for "Assura_UI"
Checking out license for "Phys_Ver_Sys_Results_Mgr"
*WARNING* No DRC errors found.
```

Run: "NOR_gate"@ecs-pa-hawking.ecs.csus.edu

Run: "NOR_gate" from
/home/student/nehagour/library/

Schematic and Layout Match.
You currently have an open run (project).

Do you want to close current project and view the results of new run?

Summary of LVS Issues

Extraction Information:

---------- ----------

0 cells have 0 mal-formed device problems
0 cells have 0 label short problems
0 cells have 0 label open problems

Comparison Information:

---------- ----------

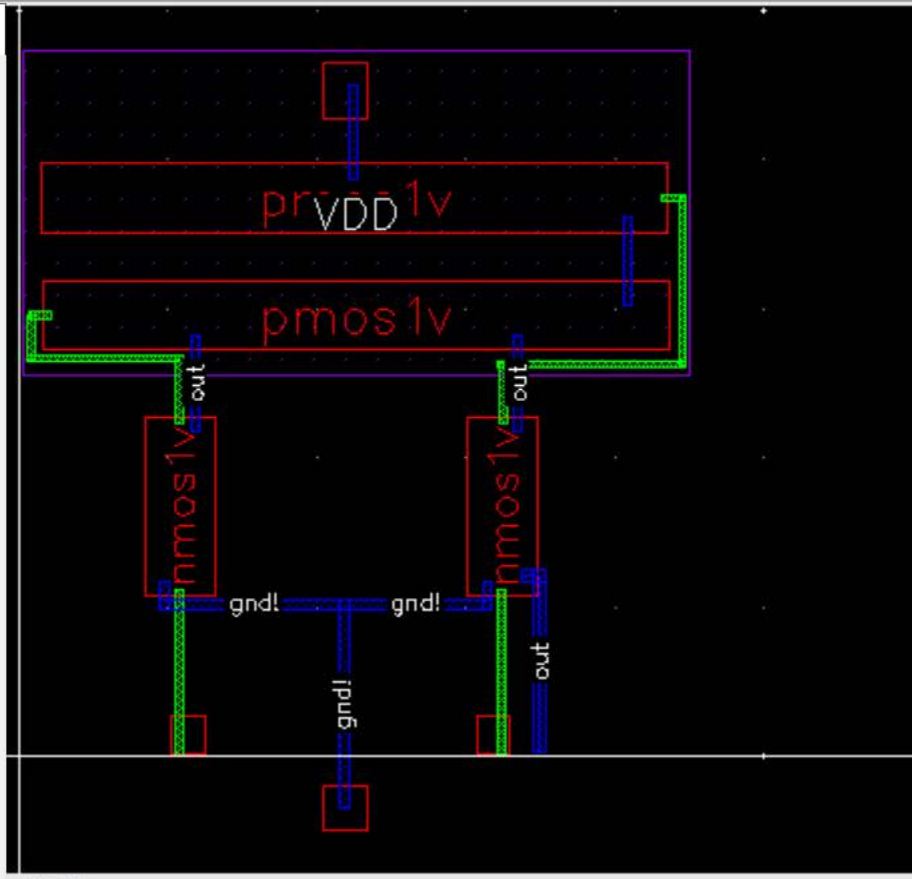
0 cells have 0 Net mismatches
0 cells have 0 Device mismatches
0 cells have 0 Pin mismatches
0 cells have 0 Parameter mismatches

ELW Information:

---------- ----------

Total DRC violations: 0

Yes No Help



```
Loading tech rule set file : /opt/pdk/gpdk045_v_6_0/assura/techRuleSets

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Loading tech rule set file : /opt/pdk/gpdk045_v_6_0/assura/techRuleSets

Loading tech rule set file : /opt/pdk/gpdk045_v_6_0/assura/techRuleSets

Loading tech rule set file : /opt/pdk/gpdk045_v_6_0/assura/techRuleSets
Assura LVS: State loaded "Last"
*INFO*: Checking whether schematic is up to date.
*INFO*: Schematic integrity check is completed.
Assura LVS: State saved "Last"
Host is
cmd  is /opt/cadence/ASSURA41/tools.lnx86/assura/bin/assura /home/student/nehagour/library/NOR_gate.rsf -cdslib /home/student/nehagour/library/cds.lib -gui
Starting the Assura LVS Run: IPC Id ipc:58: pid 3673.
Checking in license for "Phys_Ver_Sys_Results_Mgr"
Checking out license for "Assura_UI"
Checking out license for "Phys_Ver_Sys_Results_Mgr"
Schematic cell -  NOR_gate schematic 234_Project_1_NOR_gate
Schematic cell -  NOR_gate schematic 234_Project_1_NOR_gate
```

4. Design, Simulate and Layout of 2 input XOR gate' Use: (W/L)n = 2.0/0.045 and (W/L)p = 4.0/0.045

Equation of Exclusive-OR:

OUT = A'B+ AB'

Where, A, B are the inputs,

A' B' are the inverted inputs of A & B.
OUT is the output of XOR gate.

Here we are following positive logic.

Use Inverter**: (W/L)n = 1.0/0.045 and (W/L)p = 2.0/0.045**

Inverter truth table:

A	B	A'	B'
0	0	1	1
1	1	0	0

EX-OR truth table:

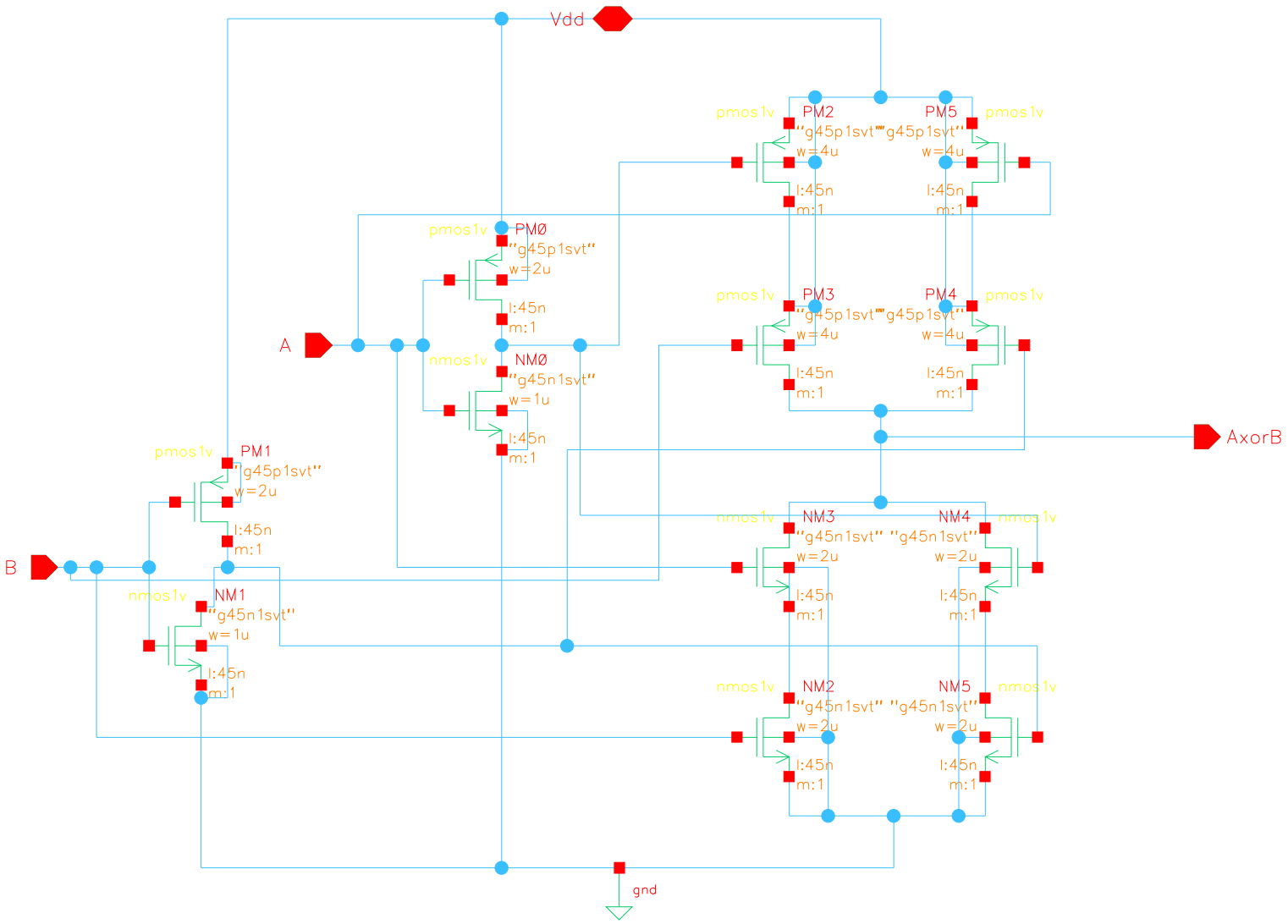
A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	0

Results obtained from circuit:

Rise time: t_{rise} = 50.05ps
Fall time t_{fall} =29.52ps
Input-output delay time = 45.97ps

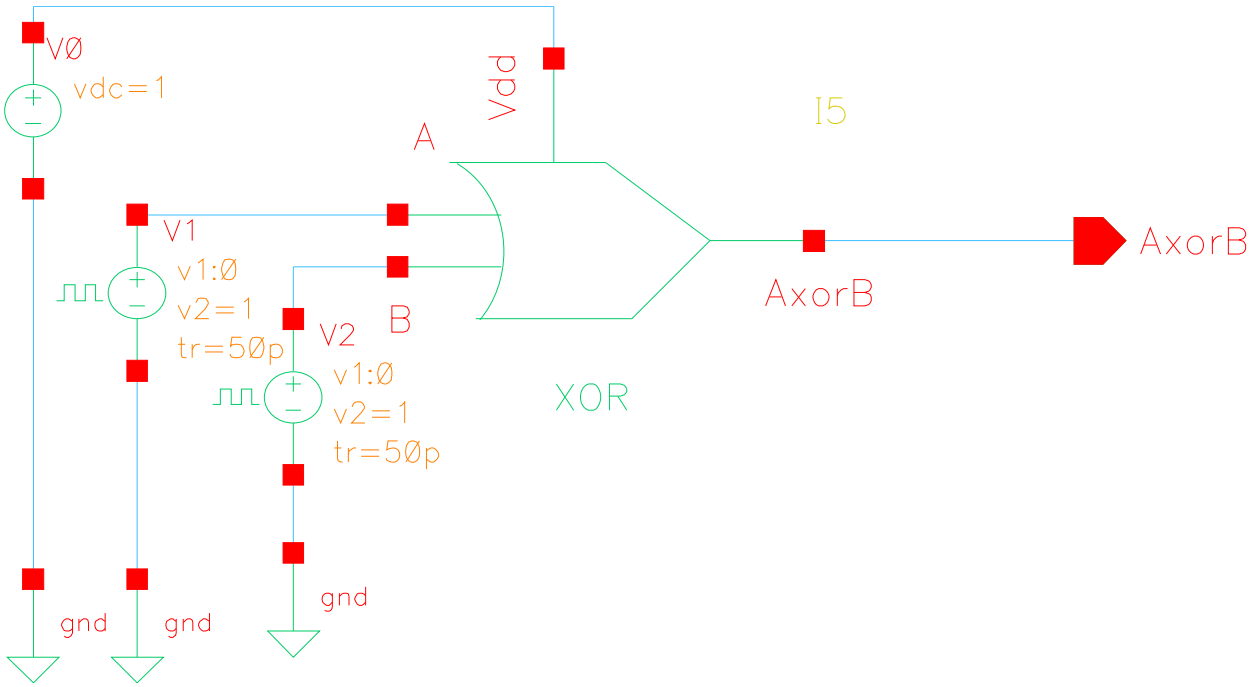
Circuit level

[2-input XOR gate]

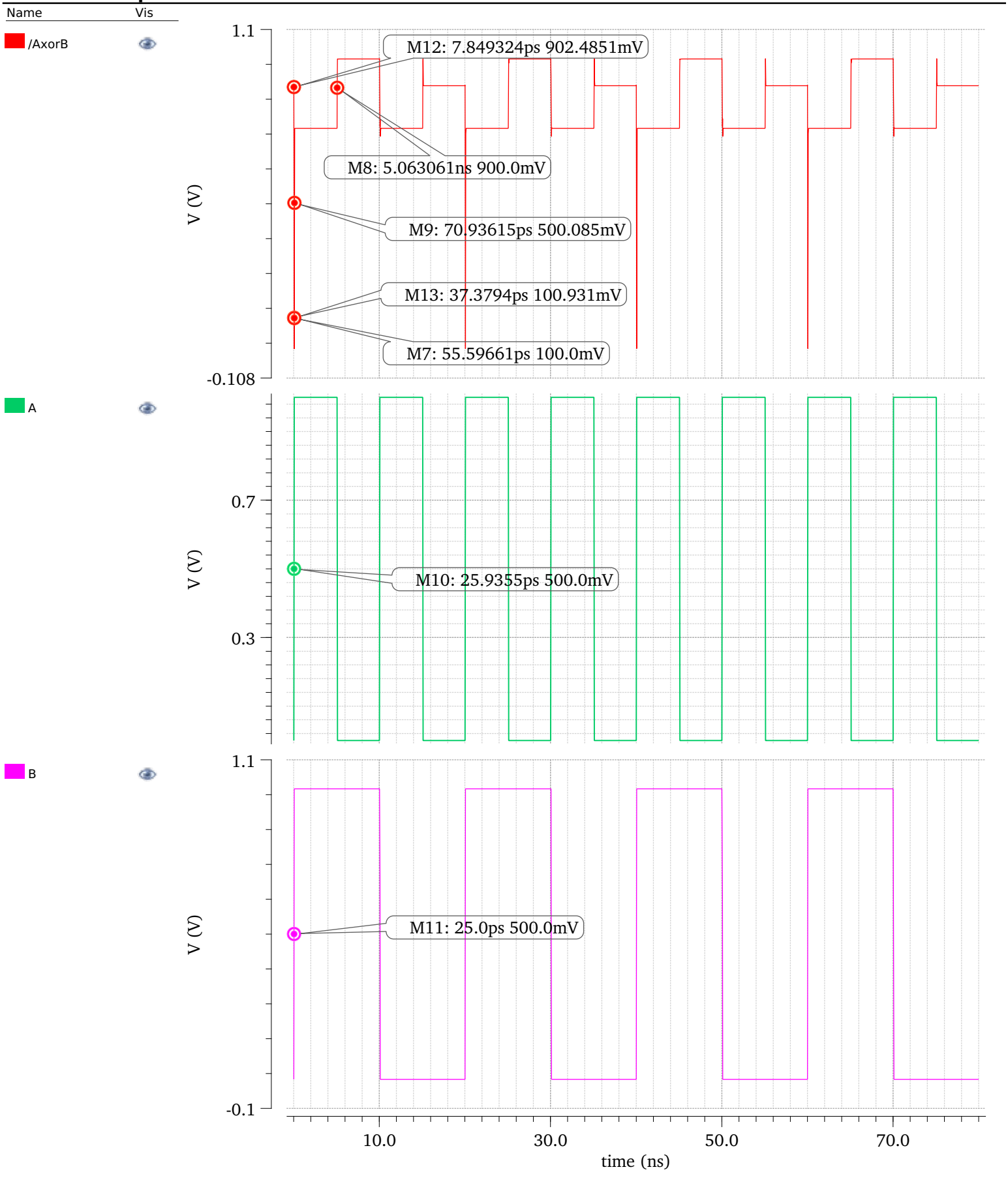


Schematic

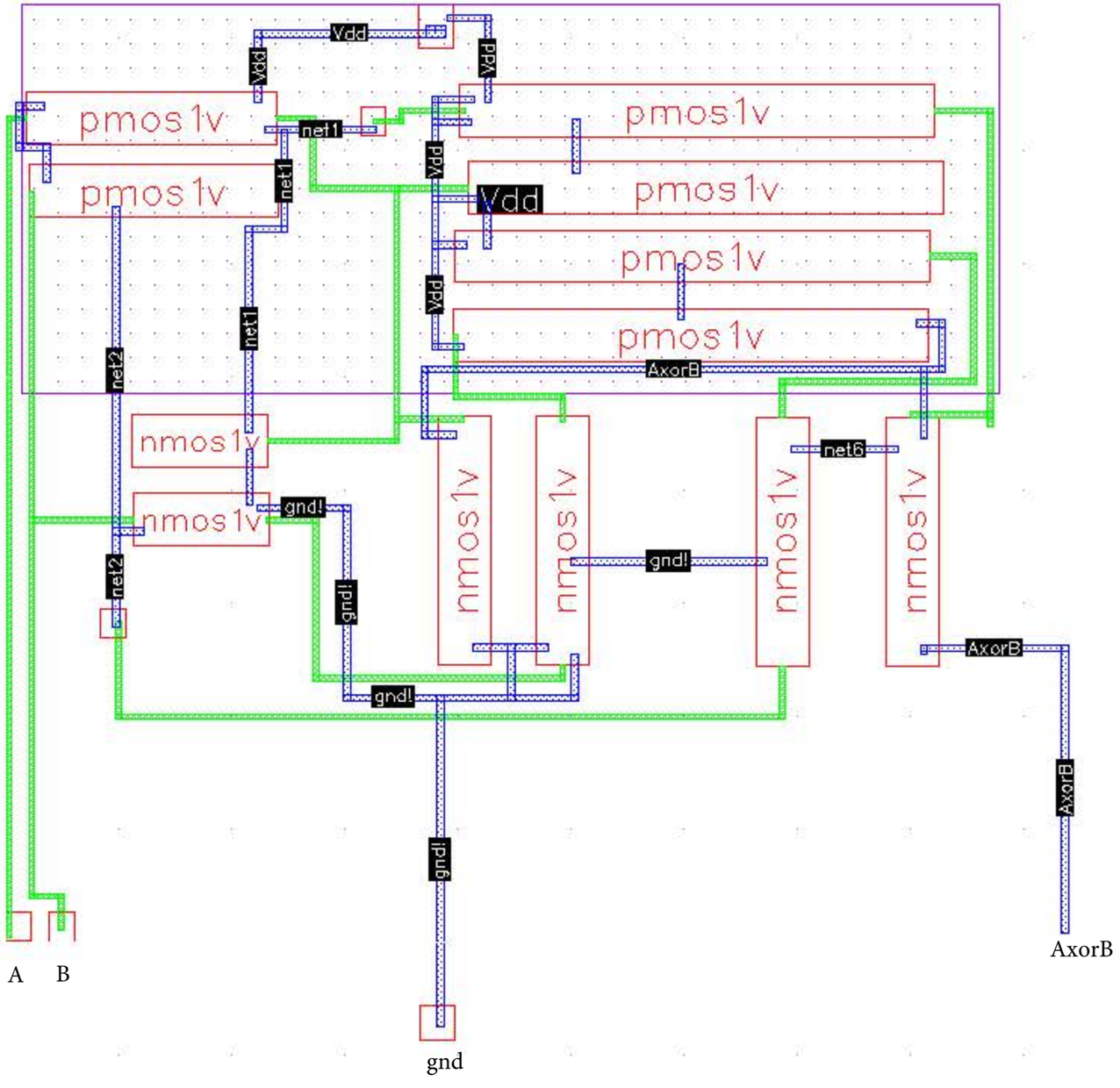
[2-input XOR gate]



Transient Response **Sat Oct 15 18:43:56 2022**



Layout [2-input XOR gate]



```
Host is
cmd  is /opt/cadence/ASSURA41/tools.lnx86/assura/bin/assura /home/student/nehagour/library/XOR.rsf -cdslib /home/student/nehagour/library/cds.lib -restart -gui
Starting the Assura DRC Run: IPC Id ipc:39: pid 26645.
Checking out license for "Assura_UI"
Checking out license for "Phys_Ver_Sys_Results_Mgr"
*WARNING* No DRC errors found.

Loading tech rule set file : /opt/pdk/gpdk045_v_6_0/assura/techRuleSets

Loading tech rule set file : /opt/pdk/gpdk045_v_6_0/assura/techRuleSets

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Loading tech rule set file : /opt/pdk/gpdk045_v_6_0/assura/techRuleSets

Loading tech rule set file : /opt/pdk/gpdk045_v_6_0/assura/techRuleSets
Assura LVS: State loaded "Last"
*INFO*: Checking whether schematic is up to date.
*INFO*: Schematic integrity check is completed.
Assura LVS: State saved "Last"
Host is
cmd  is /opt/cadence/ASSURA41/tools.lnx86/assura/bin/assura /home/student/nehagour/library/XOR.rsf -cdslib /home/student/nehagour/library/cds.lib -gui
Starting the Assura LVS Run: IPC Id ipc:40: pid 27565.
Checking in license for "Phys_Ver_Sys_Results_Mgr"
Checking out license for "Assura_UI"
Checking out license for "Phys_Ver_Sys_Results_Mgr"
Schematic cell -  XOR schematic 234_Project_1_XOR_gate
Schematic cell -  XOR schematic 234_Project_1_XOR_gate
INFO (LX-1947): Editing '234_Project_1_XOR_gate/XOR/layout' in Layout XL without a connectivity reference can introduce Layout XL compliance issues.
Specify the source schematic using the 'Connectivity - Update - Connectivity Reference' menu command.
INFO (BND-1003): Binder initialized for layout cellview '234_Project_1_XOR_gate/XOR/layout' and source cellview '234_Project_1_XOR_gate/XOR/schematic':

                  bound
  terminals           4
  nets                8
  instances          12

INFO (BND-1004): Layout instances and terminals match source.
```

5. Design, Simulate and Layout of a complex gate F = ((A+B)•(C+D))' Use: (W/L)n = 2.0/0.045 and (W/L)p = 4.0/0.045

This AOI contains 4 input A,B,C,D and output will be F

In this schematic, input IN_A, IN_B,IN_C,IN_D are the inputs and F is the output using positive logic.

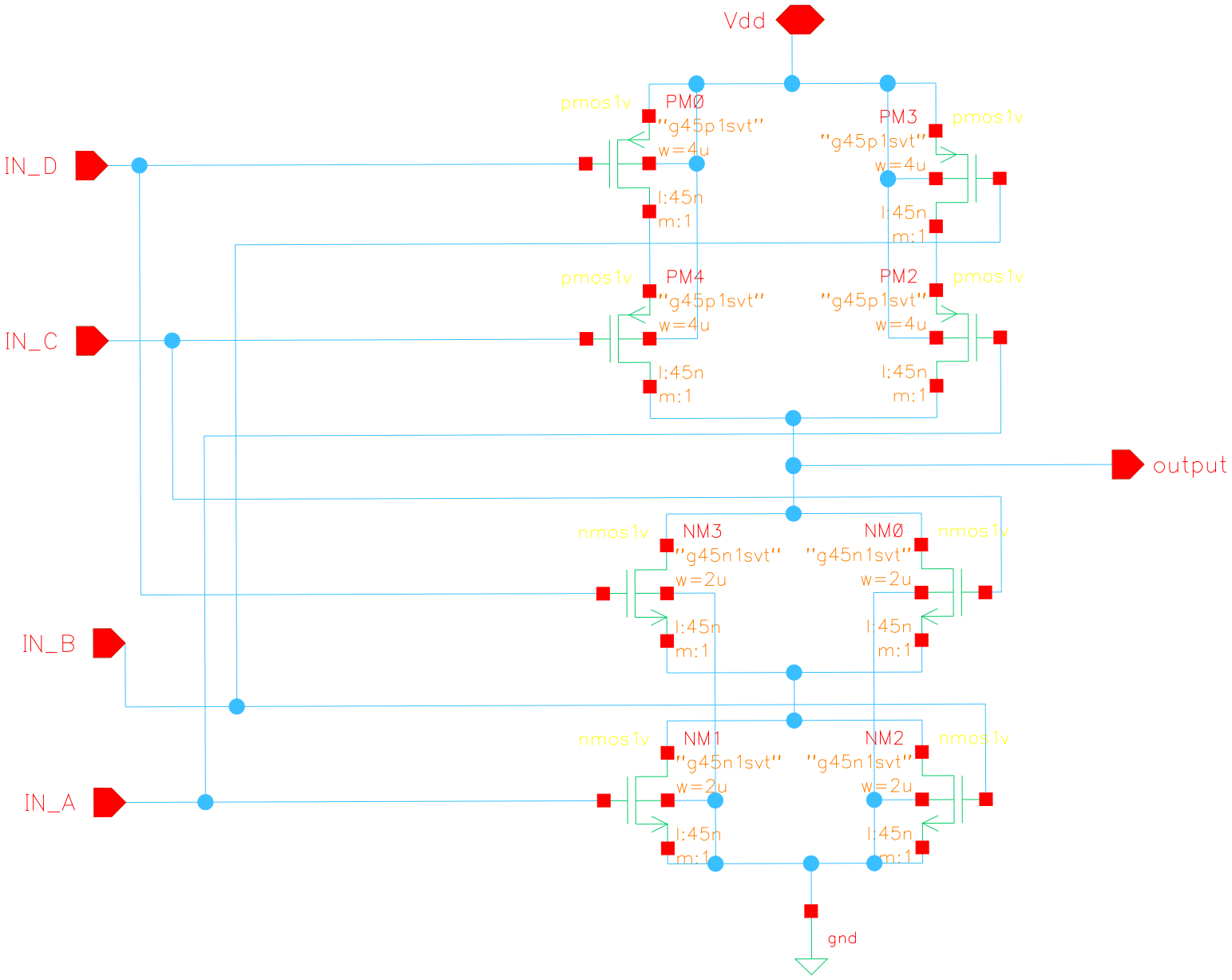
Below are the possible combinations of complex function.

IN_A	IN_B	IN_C	IN_D	OUT
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Results obtained from circuit:

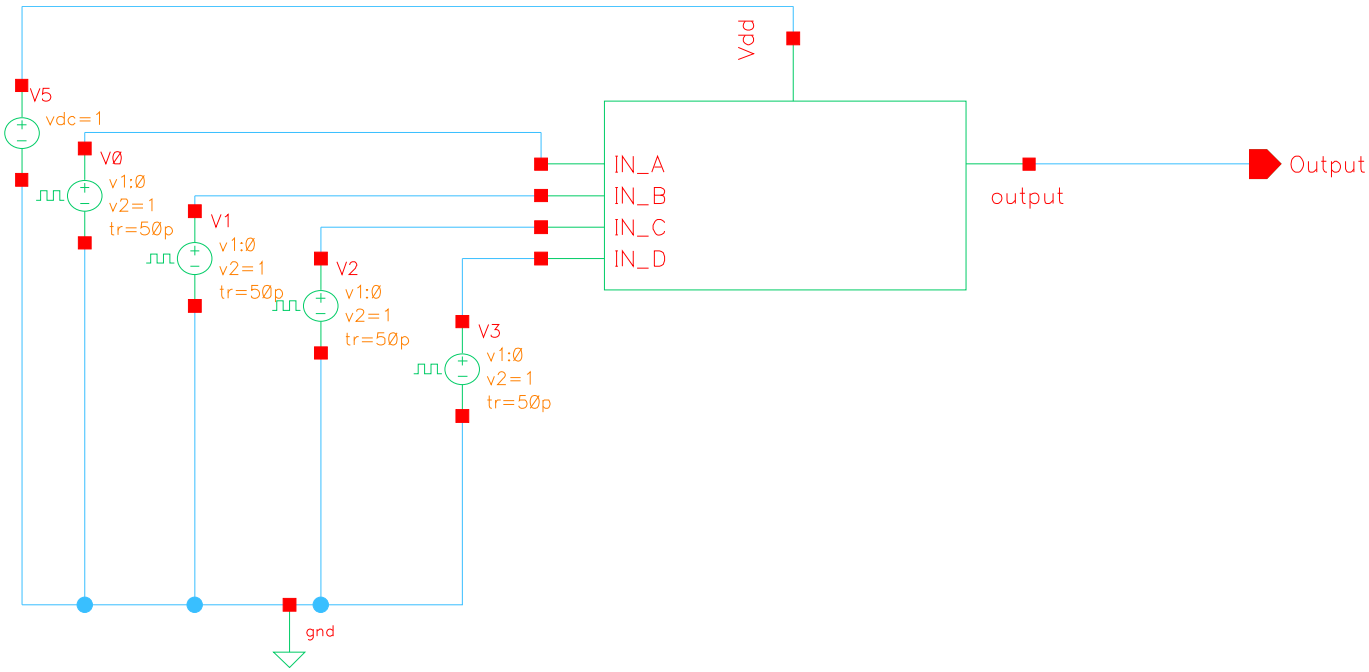
Rise time: t_{rise} = 9.7 ps
Fall time t_{fall} = 5.6ps
Input-output delay time = 23.66ps

Circuit level
AOI

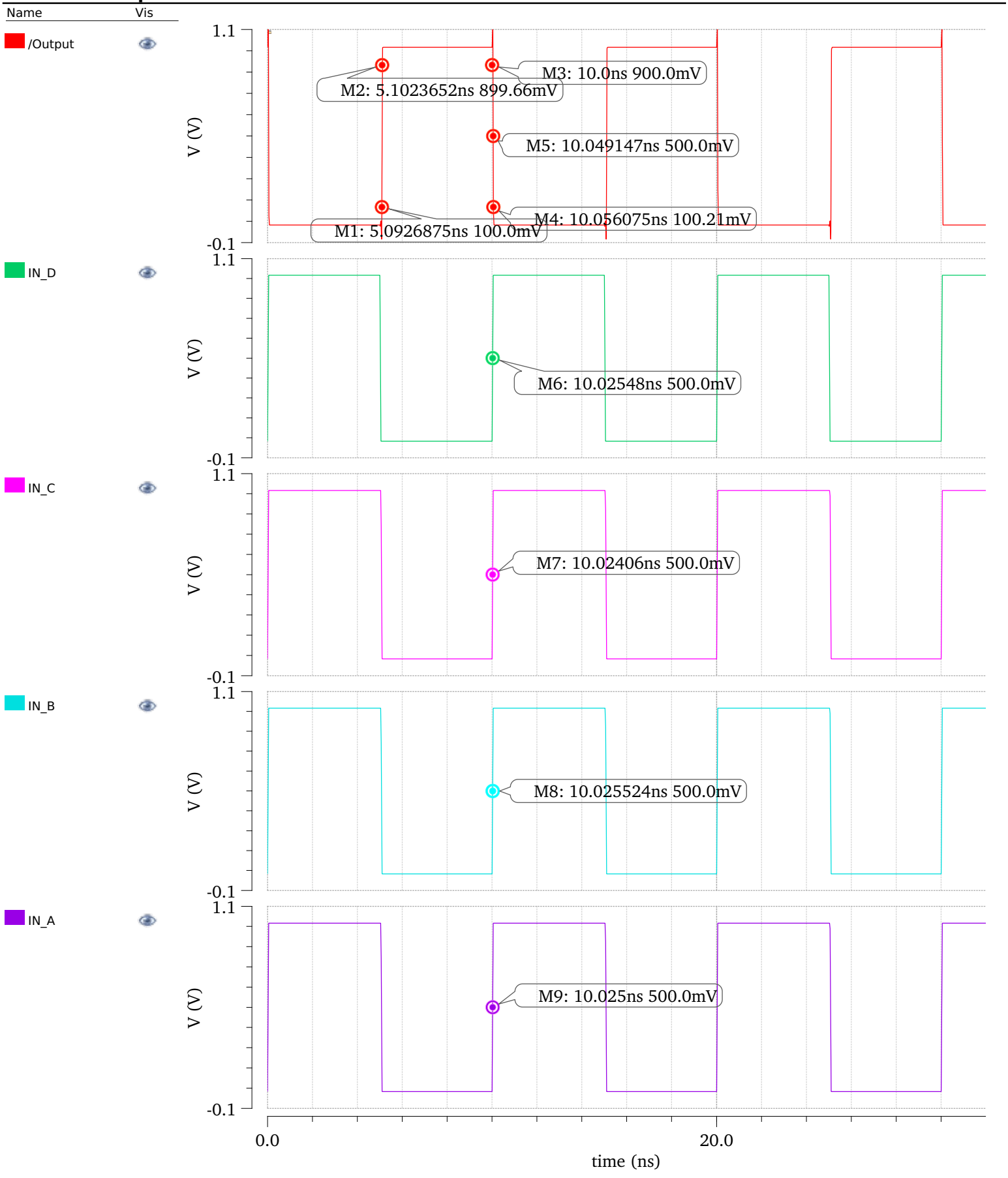


Schematic

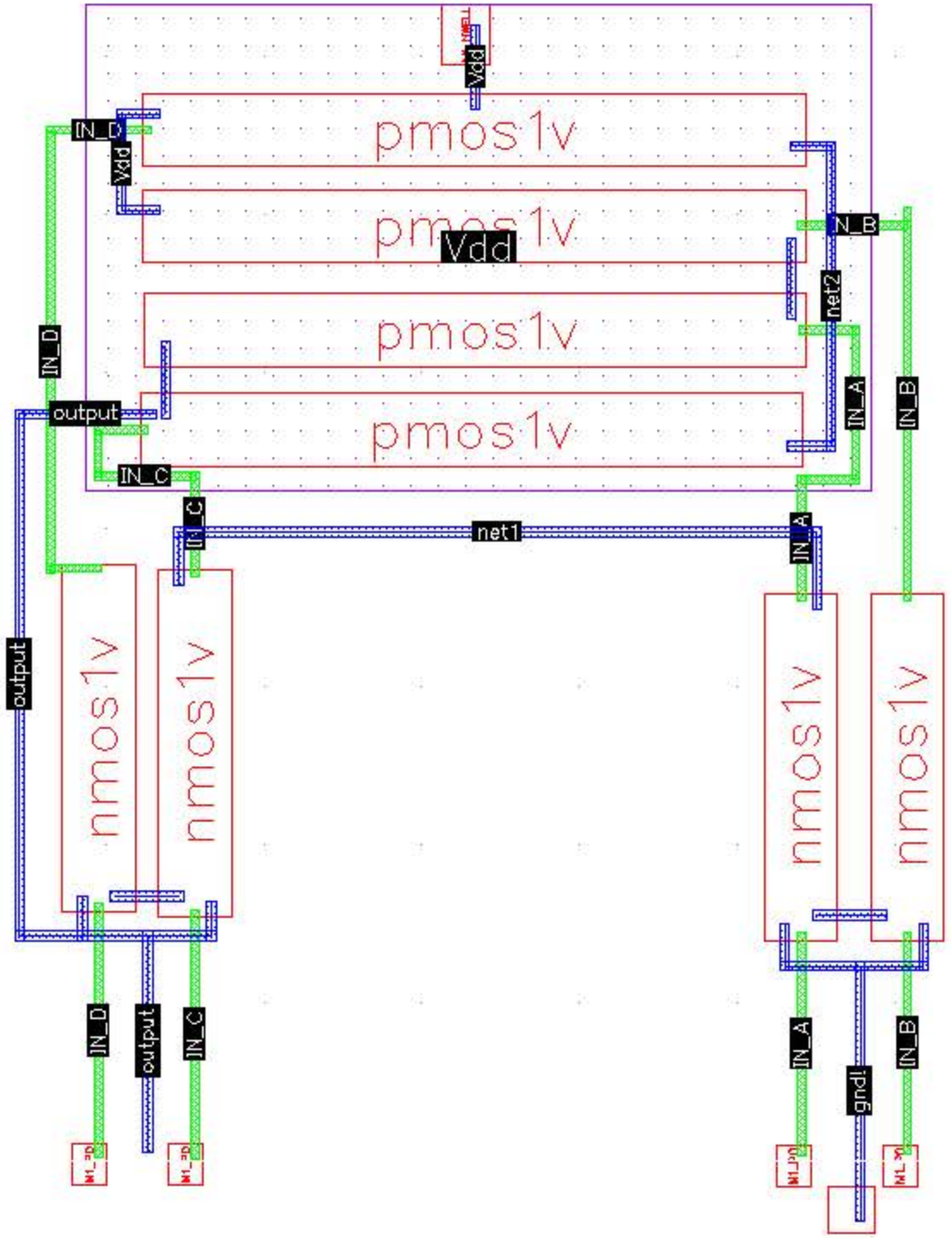
AOI



Transient Response **Fri Oct 14 23:35:09 2022**



Layout AOI


Vdd
IN_D
Vdd
pmos1v
pmos1v
Vdd
pmos1v
pmos1v
IN_B
net2
IN_D
output
IN_A
IN_B
IN_C
IN_C
net1
IN_A
output
nmos1v
nmos1v
nmos1v
nmos1v
IN_D
output
IN_C
IN_A
gnd!
IN_B

```
Host is
cmd  is /opt/cadence/ASSURA41/tools.lnx86/assura/bin/assura /home/student/nehagour/library/Function.rsf -cdslib /home/student/nehagour/library/cds.lib -restart -gui
Starting the Assura DRC Run: IPC Id ipc:34: pid 27481.
Checking out license for "Assura_UI"
Checking out license for "Phys_Ver_Sys_Results_Mgr"
*WARNING* No DRC errors found.
```

```
Loading tech rule set file : /opt/pdk/gpdk045_v_6_0/assura/techRuleSets

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Loading tech rule set file : /opt/pdk/gpdk045_v_6_0/assura/techRuleSets

Loading tech rule set file : /opt/pdk/gpdk045_v_6_0/assura/techRuleSets
Assura LVS: State loaded "Last"
*INFO*: Checking whether schematic is up to date.
*INFO*: Schematic integrity check is completed.
Assura LVS: State saved "Last"
Host is
cmd  is /opt/cadence/ASSURA41/tools.lnx86/assura/bin/assura /home/student/nehagour/library/Function.rsf -cdslib /home/student/nehagour/library/cds.lib -gui
Starting the Assura LVS Run: IPC Id ipc:35: pid 30706.
Checking in license for "Phys_Ver_Sys_Results_Mgr"
Checking out license for "Assura_UI"
Checking out license for "Phys_Ver_Sys_Results_Mgr"
Schematic cell -  Function schematic function
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INFO (LX-1947): Editing 'function/Function/layout' in Layout XL without a connectivity reference can introduce Layout XL compliance issues.
Specify the source schematic using the 'Connectivity - Update - Connectivity Reference' menu command.
INFO (BND-1003): Binder initialized for layout cellview 'function/Function/layout' and source cellview 'function/Function/schematic':

                 bound
  terminals          6
  nets              10
  instances          8

INFO (BND-1004): Layout instances and terminals match source.
```

Results:

We build transistor level designs of basic gates and AOI on Cadence virtuoso, then simulate it & generate DRC & LVS error free layout. With the help of Testbench we are able to find out input-output delay time, & rise and fall times (10%-90%).

Sr.no.	Description	Rise time	Fall time	Delay Time
1	Inverter	10.34ps	11.22ps	14.11ps
2	2-input NAND gate	10.10ps	14.30ps	25.11ps
3	2-input NOR gate	15.81ps	10.08ps	17.87ps
4	2-input XOR gate	50.05ps	29.52ps	45.97ps
5	Complex Function F = ((A+B). (C+D))’	9.7ps	5.6ps	23.66ps