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----------------------------------------------------------------------------------
-- Engineer:
--
-- Create Date: 26.07.2017 09:58:59
-- Design Name:
-- Module Name: adder - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity adder is
    Port ( X : in STD_LOGIC_VECTOR (7 downto 0);
           Y : in STD_LOGIC_VECTOR (7 downto 0);
           Z : out STD_LOGIC_VECTOR (7 downto 0);
           ce1 : in STD_LOGIC;
          clk1 : in STD_LOGIC);
end adder;

architecture Behavioral of adder is
component design_1_adder is
port (X : in STD_LOGIC_VECTOR (7 downto 0);
           Y : in STD_LOGIC_VECTOR (7 downto 0);
           Z : out STD_LOGIC_VECTOR (7 downto 0);
           ce1 : in STD_LOGIC;
           clk1 : in STD_LOGIC );
           end component design_1_adder;
  ------------------------------------------------
      signal A: std_logic_vector(7 downto 0) ;
      signal B: std_logic_vector(7 downto 0) ;
```

```
_vector(7 downto 0) ;
C;
LOGIC;
-------------------------------------------------------
begin
  A(7 downto 0) <= X(7 downto 0);
  B(7 downto 0) <= Y(7 downto 0);
 S(7 downto 0) <= Z(7 downto 0);
  CE1 <= ce1;
  CLK1 <= clk1;

-----------------------------------------------------------------
 design_1_adder_1 : component design_1_adder
  port map(X(7 downto 0) => A(7 downto 0);
           Y(7 downto 0) => B(7 downto 0);
           Z(7 downto 0) => S(7 downto 0);
               ce1  => CE ;
               clk1 => CLK);

end Behavioral;
```