Reducing computational complexity of mathematical functions Using FPGA

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Abstract: Computationally intensive applications such as weather forecasting, computational biology, Big Data etc. require lot of time to execute a task, because usually the task is sequentially simulated. The objective of this project is to explore the computational complexity of mathematical functions using the concept of concurrency. Existing algorithms do not attempt to minimize the execution time. Although matrix multiplication has found a lot of interest in scientific research due to its efficiency and quick execution, it becomes a computational intensive problem, especially in design and implementation on Field Programmable Gate Array (FPGA), where resources are limited. The main goal of our work is to achieve high speed by using the optimization techniques such as loop unrolling and loop pipelining. High Level Synthesis (HLS) is used to apply and verify these different optimization techniques. HLS is an automated generation of hardware circuit of digital system from its behavioural description. Our initial simulation results demonstrate the utility of these optimization techniques in reducing the total execution time of parallel matrix multiplication in comparison to the existing algorithms. In addition, loop unrolling and loop pipelining also results in the increase of hardware.