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## File generated by Vivado(TM) HLS - High-Level Synthesis from C, C++ and SystemC

## Version: 2017.2

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\*\*\*\*\*\* Vivado v2017.2 (64-bit)

\*\*\*\* SW Build 1909853 on Thu Jun 15 18:39:10 MDT 2017

\*\*\*\* IP Build 1909766 on Thu Jun 15 19:58:00 MDT 2017

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source run\_vivadosyn.tcl -notrace

[Fri Mar 16 10:01:01 2018] Launched synth\_1...

Run output will be captured here: /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/project.runs/synth\_1/runme.log

[Fri Mar 16 10:01:01 2018] Waiting for synth\_1 to finish...

\*\*\* Running vivado

with args -log matrixmul.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source matrixmul.tcl

\*\*\*\*\*\* Vivado v2017.2 (64-bit)

\*\*\*\* SW Build 1909853 on Thu Jun 15 18:39:10 MDT 2017

\*\*\*\* IP Build 1909766 on Thu Jun 15 19:58:00 MDT 2017

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source matrixmul.tcl -notrace

Command: synth\_design -top matrixmul -part xc7a35tcpg236-3 -no\_iobuf -mode out\_of\_context

Starting synth\_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a35t-cpg236'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t-cpg236'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 19017

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Starting RTL Elaboration : Time (s): cpu = 00:00:03 ; elapsed = 00:00:03 . Memory (MB): peak = 1155.531 ; gain = 51.992 ; free physical = 350 ; free virtual = 5188

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INFO: [Synth 8-638] synthesizing module 'matrixmul' [/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/matrixmul.vhd:34]

INFO: [Synth 8-5534] Detected attribute (\* fsm\_encoding = "none" \*) [/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/matrixmul.vhd:62]

INFO: [Synth 8-5534] Detected attribute (\* fsm\_encoding = "none" \*) [/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/matrixmul.vhd:65]

INFO: [Synth 8-5534] Detected attribute (\* fsm\_encoding = "none" \*) [/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/matrixmul.vhd:69]

INFO: [Synth 8-5534] Detected attribute (\* fsm\_encoding = "none" \*) [/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/matrixmul.vhd:84]

INFO: [Synth 8-5534] Detected attribute (\* fsm\_encoding = "none" \*) [/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/matrixmul.vhd:93]

INFO: [Synth 8-5534] Detected attribute (\* fsm\_encoding = "none" \*) [/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/matrixmul.vhd:99]

Parameter ID bound to: 1 - type: integer

Parameter NUM\_STAGE bound to: 1 - type: integer

Parameter din0\_WIDTH bound to: 8 - type: integer

Parameter din1\_WIDTH bound to: 8 - type: integer

Parameter din2\_WIDTH bound to: 16 - type: integer

Parameter dout\_WIDTH bound to: 16 - type: integer

INFO: [Synth 8-3491] module 'matrixmul\_mac\_mulbkb' declared at '/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/matrixmul\_mac\_mulbkb.vhd:45' bound to instance 'matrixmul\_mac\_mulbkb\_U1' of component 'matrixmul\_mac\_mulbkb' [/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/matrixmul.vhd:149]

INFO: [Synth 8-638] synthesizing module 'matrixmul\_mac\_mulbkb' [/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/matrixmul\_mac\_mulbkb.vhd:60]

Parameter ID bound to: 1 - type: integer

Parameter NUM\_STAGE bound to: 1 - type: integer

Parameter din0\_WIDTH bound to: 8 - type: integer

Parameter din1\_WIDTH bound to: 8 - type: integer

Parameter din2\_WIDTH bound to: 16 - type: integer

Parameter dout\_WIDTH bound to: 16 - type: integer

INFO: [Synth 8-3491] module 'matrixmul\_mac\_mulbkb\_DSP48\_0' declared at '/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/matrixmul\_mac\_mulbkb.vhd:12' bound to instance 'matrixmul\_mac\_mulbkb\_DSP48\_0\_U' of component 'matrixmul\_mac\_mulbkb\_DSP48\_0' [/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/matrixmul\_mac\_mulbkb.vhd:72]

INFO: [Synth 8-638] synthesizing module 'matrixmul\_mac\_mulbkb\_DSP48\_0' [/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/matrixmul\_mac\_mulbkb.vhd:24]

WARNING: [Synth 8-5974] attribute "use\_dsp48" has been deprecated, please use "use\_dsp" instead

INFO: [Synth 8-256] done synthesizing module 'matrixmul\_mac\_mulbkb\_DSP48\_0' (1#1) [/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/matrixmul\_mac\_mulbkb.vhd:24]

INFO: [Synth 8-256] done synthesizing module 'matrixmul\_mac\_mulbkb' (2#1) [/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/matrixmul\_mac\_mulbkb.vhd:60]

WARNING: [Synth 8-6014] Unused sequential element ap\_idle\_pp0\_reg was removed. [/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/matrixmul.vhd:383]

WARNING: [Synth 8-6014] Unused sequential element ap\_ready\_reg was removed. [/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/matrixmul.vhd:408]

WARNING: [Synth 8-6014] Unused sequential element b\_ce0\_reg was removed. [/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/matrixmul.vhd:419]

INFO: [Synth 8-256] done synthesizing module 'matrixmul' (3#1) [/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/matrixmul.vhd:34]

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Finished RTL Elaboration : Time (s): cpu = 00:00:04 ; elapsed = 00:00:04 . Memory (MB): peak = 1197.039 ; gain = 93.500 ; free physical = 360 ; free virtual = 5199

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Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:04 ; elapsed = 00:00:04 . Memory (MB): peak = 1197.039 ; gain = 93.500 ; free physical = 360 ; free virtual = 5199

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INFO: [Device 21-403] Loading part xc7a35tcpg236-3

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/matrixmul.xdc]

Finished Parsing XDC File [/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/matrixmul.xdc]

Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.02 . Memory (MB): peak = 1536.055 ; gain = 0.004 ; free physical = 128 ; free virtual = 4966

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Finished Constraint Validation : Time (s): cpu = 00:00:12 ; elapsed = 00:00:13 . Memory (MB): peak = 1536.055 ; gain = 432.516 ; free physical = 203 ; free virtual = 5042

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Start Loading Part and Timing Information

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Loading part: xc7a35tcpg236-3

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Finished Loading Part and Timing Information : Time (s): cpu = 00:00:12 ; elapsed = 00:00:13 . Memory (MB): peak = 1536.055 ; gain = 432.516 ; free physical = 203 ; free virtual = 5042

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Start Applying 'set\_property' XDC Constraints

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Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:12 ; elapsed = 00:00:13 . Memory (MB): peak = 1536.055 ; gain = 432.516 ; free physical = 205 ; free virtual = 5043

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INFO: [Synth 8-4490] FSM extraction disabled for register 'ap\_CS\_fsm\_reg' through user attribute

INFO: [Synth 8-5544] ROM "exitcond\_flatten\_fu\_137\_p2" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "exitcond1\_fu\_155\_p2" won't be mapped to Block RAM because address size (2) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "exitcond\_fu\_214\_p2" won't be mapped to Block RAM because address size (2) smaller than threshold (5)

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Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:13 ; elapsed = 00:00:13 . Memory (MB): peak = 1536.055 ; gain = 432.516 ; free physical = 197 ; free virtual = 5035

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start RTL Component Statistics

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Detailed RTL Component Info :

+---Adders :

3 Input 5 Bit Adders := 1

2 Input 5 Bit Adders := 1

4 Input 5 Bit Adders := 2

2 Input 4 Bit Adders := 1

2 Input 2 Bit Adders := 3

+---Registers :

8 Bit Registers := 2

5 Bit Registers := 3

4 Bit Registers := 3

2 Bit Registers := 6

1 Bit Registers := 3

+---Muxes :

2 Input 16 Bit Muxes := 1

3 Input 5 Bit Muxes := 1

2 Input 4 Bit Muxes := 1

2 Input 3 Bit Muxes := 1

2 Input 2 Bit Muxes := 2

2 Input 1 Bit Muxes := 6

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Finished RTL Component Statistics

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Start RTL Hierarchical Component Statistics

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Hierarchical RTL Component report

Module matrixmul

Detailed RTL Component Info :

+---Adders :

3 Input 5 Bit Adders := 1

2 Input 5 Bit Adders := 1

4 Input 5 Bit Adders := 2

2 Input 4 Bit Adders := 1

2 Input 2 Bit Adders := 3

+---Registers :

8 Bit Registers := 2

5 Bit Registers := 3

4 Bit Registers := 3

2 Bit Registers := 6

1 Bit Registers := 3

+---Muxes :

2 Input 16 Bit Muxes := 1

3 Input 5 Bit Muxes := 1

2 Input 4 Bit Muxes := 1

2 Input 3 Bit Muxes := 1

2 Input 2 Bit Muxes := 2

2 Input 1 Bit Muxes := 6

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Finished RTL Hierarchical Component Statistics

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Start Part Resource Summary

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Part Resources:

DSPs: 90 (col length:60)

BRAMs: 100 (col length: RAMB18 60 RAMB36 30)

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Finished Part Resource Summary

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Start Cross Boundary and Area Optimization

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DSP Report: Generating DSP p, operation Mode is: C+A\*B.

DSP Report: operator p is absorbed into DSP p.

DSP Report: operator m is absorbed into DSP p.

WARNING: [Synth 8-3936] Found unconnected internal register 'tmp\_1\_reg\_307\_reg' and it is trimmed from '5' to '4' bits. [/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/matrixmul.vhd:287]

INFO: [Synth 8-3886] merging instance 'j\_mid2\_reg\_297\_reg[1]' (FDE) to 'tmp\_2\_cast\_reg\_312\_reg[1]'

INFO: [Synth 8-3886] merging instance 'j\_mid2\_reg\_297\_reg[0]' (FDE) to 'tmp\_2\_cast\_reg\_312\_reg[0]'

INFO: [Synth 8-3886] merging instance 'tmp\_mid2\_v\_reg\_302\_reg[0]' (FDE) to 'tmp\_1\_reg\_307\_reg[0]'

---------------------------------------------------------------------------------

Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:13 ; elapsed = 00:00:13 . Memory (MB): peak = 1536.059 ; gain = 432.520 ; free physical = 186 ; free virtual = 5025

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Start ROM, RAM, DSP and Shift Register Reporting

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DSP: Preliminary Mapping Report (see note below)

+-----------------------------+-------------+--------+--------+--------+--------+--------+------+------+------+------+-------+------+------+

|Module Name | DSP Mapping | A Size | B Size | C Size | D Size | P Size | AREG | BREG | CREG | DREG | ADREG | MREG | PREG |

+-----------------------------+-------------+--------+--------+--------+--------+--------+------+------+------+------+-------+------+------+

|matrixmul\_mac\_mulbkb\_DSP48\_0 | C+A\*B | 8 | 8 | 16 | - | 16 | 0 | 0 | 0 | - | - | 0 | 0 |

+-----------------------------+-------------+--------+--------+--------+--------+--------+------+------+------+------+-------+------+------+

Note: The table above is a preliminary report that shows the DSPs inferred at the current stage of the synthesis flow. Some DSP may be reimplemented as non DSP primitives later in the synthesis flow. Multiple instantiated DSPs are reported only once.

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Finished ROM, RAM, DSP and Shift Register Reporting

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

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Start Applying XDC Timing Constraints

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Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:21 ; elapsed = 00:00:22 . Memory (MB): peak = 1537.051 ; gain = 433.512 ; free physical = 142 ; free virtual = 4878

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Start Timing Optimization

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Finished Timing Optimization : Time (s): cpu = 00:00:21 ; elapsed = 00:00:22 . Memory (MB): peak = 1550.066 ; gain = 446.527 ; free physical = 156 ; free virtual = 4876

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

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Start Technology Mapping

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Finished Technology Mapping : Time (s): cpu = 00:00:22 ; elapsed = 00:00:22 . Memory (MB): peak = 1560.082 ; gain = 456.543 ; free physical = 152 ; free virtual = 4872

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start IO Insertion

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Start Flattening Before IO Insertion

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Finished Flattening Before IO Insertion

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Start Final Netlist Cleanup

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Finished Final Netlist Cleanup

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Finished IO Insertion : Time (s): cpu = 00:00:22 ; elapsed = 00:00:23 . Memory (MB): peak = 1560.082 ; gain = 456.543 ; free physical = 152 ; free virtual = 4872

---------------------------------------------------------------------------------

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Renaming Generated Instances

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Finished Renaming Generated Instances : Time (s): cpu = 00:00:22 ; elapsed = 00:00:23 . Memory (MB): peak = 1560.082 ; gain = 456.543 ; free physical = 152 ; free virtual = 4872

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Rebuilding User Hierarchy

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Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:22 ; elapsed = 00:00:23 . Memory (MB): peak = 1560.082 ; gain = 456.543 ; free physical = 151 ; free virtual = 4872

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Start Renaming Generated Ports

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Finished Renaming Generated Ports : Time (s): cpu = 00:00:22 ; elapsed = 00:00:23 . Memory (MB): peak = 1560.082 ; gain = 456.543 ; free physical = 151 ; free virtual = 4872

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:22 ; elapsed = 00:00:23 . Memory (MB): peak = 1560.082 ; gain = 456.543 ; free physical = 151 ; free virtual = 4872

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Start Renaming Generated Nets

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Finished Renaming Generated Nets : Time (s): cpu = 00:00:22 ; elapsed = 00:00:23 . Memory (MB): peak = 1560.082 ; gain = 456.543 ; free physical = 151 ; free virtual = 4872

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Start Writing Synthesis Report

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Report BlackBoxes:

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| |BlackBox name |Instances |

+-+--------------+----------+

+-+--------------+----------+

Report Cell Usage:

+------+----------+------+

| |Cell |Count |

+------+----------+------+

|1 |DSP48E1\_1 | 1|

|2 |LUT1 | 2|

|3 |LUT2 | 10|

|4 |LUT3 | 24|

|5 |LUT4 | 14|

|6 |LUT5 | 8|

|7 |LUT6 | 13|

|8 |FDRE | 34|

|9 |FDSE | 1|

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Report Instance Areas:

+------+-----------------------------------+-----------------------------+------+

| |Instance |Module |Cells |

+------+-----------------------------------+-----------------------------+------+

|1 |top | | 107|

|2 | matrixmul\_mac\_mulbkb\_U1 |matrixmul\_mac\_mulbkb | 18|

|3 | matrixmul\_mac\_mulbkb\_DSP48\_0\_U |matrixmul\_mac\_mulbkb\_DSP48\_0 | 18|

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Finished Writing Synthesis Report : Time (s): cpu = 00:00:22 ; elapsed = 00:00:23 . Memory (MB): peak = 1560.082 ; gain = 456.543 ; free physical = 151 ; free virtual = 4871

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Synthesis finished with 0 errors, 0 critical warnings and 1 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:18 ; elapsed = 00:00:18 . Memory (MB): peak = 1560.082 ; gain = 117.527 ; free physical = 216 ; free virtual = 4937

Synthesis Optimization Complete : Time (s): cpu = 00:00:22 ; elapsed = 00:00:23 . Memory (MB): peak = 1560.090 ; gain = 456.543 ; free physical = 216 ; free virtual = 4937

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 1 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

31 Infos, 5 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth\_design completed successfully

synth\_design: Time (s): cpu = 00:00:24 ; elapsed = 00:00:24 . Memory (MB): peak = 1560.090 ; gain = 469.137 ; free physical = 190 ; free virtual = 4912

INFO: [Common 17-1381] The checkpoint '/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/project.runs/synth\_1/matrixmul.dcp' has been generated.

report\_utilization: Time (s): cpu = 00:00:00.08 ; elapsed = 00:00:00.27 . Memory (MB): peak = 1584.098 ; gain = 0.000 ; free physical = 192 ; free virtual = 4915

INFO: [Common 17-206] Exiting Vivado at Fri Mar 16 10:01:34 2018...

[Fri Mar 16 10:01:38 2018] synth\_1 finished

wait\_on\_run: Time (s): cpu = 00:00:00.10 ; elapsed = 00:00:37 . Memory (MB): peak = 1131.289 ; gain = 0.000 ; free physical = 695 ; free virtual = 5418

Design is defaulting to impl run constrset: constrs\_1

Design is defaulting to synth run part: xc7a35tcpg236-3

INFO: [Netlist 29-17] Analyzing 1 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2017.2

INFO: [Device 21-403] Loading part xc7a35tcpg236-3

INFO: [Project 1-570] Preparing netlist for logic optimization

Parsing XDC File [/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/matrixmul.xdc]

INFO: [Vivado 12-4761] HD.CLK\_SRC property is set on port ap\_clk. The net connecting to the port drives either clock PIN or hierarchical black box. Use the create\_clock constraint to create a clock on this port prior to setting HD.CLK\_SRC. [/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/matrixmul.xdc:2]

Finished Parsing XDC File [/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1/solution1/impl/vhdl/matrixmul.xdc]

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

report\_utilization: Time (s): cpu = 00:00:00.09 ; elapsed = 00:00:00.12 . Memory (MB): peak = 1377.488 ; gain = 0.000 ; free physical = 453 ; free virtual = 5177

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -3, Delay Type: max.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 4 CPUs

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [Timing 38-78] ReportTimingParams: -max\_paths 1 -nworst 1 -delay\_type max -sort\_by slack.

report\_timing: Time (s): cpu = 00:00:08 ; elapsed = 00:00:09 . Memory (MB): peak = 1803.934 ; gain = 426.445 ; free physical = 150 ; free virtual = 4801

Implementation tool: Xilinx Vivado v.2017.2

Project: MATRIX\_MULTIPLICATION\_16\_PIPELINE\_1

Solution: solution1

Device target: xc7a35tcpg236-3

Report date: Fri Mar 16 10:01:52 IST 2018

#=== Post-Synthesis Resource usage ===

SLICE: 0

LUT: 52

FF: 35

DSP: 1

BRAM: 0

SRL: 0

#=== Final timing ===

CP required: 10.000

CP achieved post-synthesis: 2.084

Timing met

INFO: [Common 17-206] Exiting Vivado at Fri Mar 16 10:01:52 2018...