INFO: [HLS 200-0] Workspace /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1 opened at Fri Mar 16 11:40:07 IST 2018

INFO: [HLS 200-100] Execute config\_clock -quiet -name default -period 10 -default=false

INFO: [SYN 201-201] Setting up clock 'default' with a period of 10ns.

INFO: [HLS 200-100] Command config\_clock returned 0; 0 sec.

INFO: [HLS 200-100] Execute open\_platform DefaultPlatform

INFO: [HLS 200-100] Command open\_platform returned 0; 0 sec.

INFO: [HLS 200-100] Execute import\_lib /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/artix7/artix7

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/xilinx.lib

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/xilinx\_interface.lib

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/plb46.lib

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/fsl.lib

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/axi4.lib

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/maxi.lib

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/saxilite.lib

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/dsp48.lib

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/ip/xfft.lib

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/ip/dds\_compiler.lib

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/ip/xfir.lib

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0.01 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/xilinx\_old.lib

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/xilinx\_vivado.lib

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/xilinx.hlp

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/target\_info.tcl

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/xilinx\_interface.hlp

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/maxi.hlp

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/saxilite.hlp

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/dsp48.hlp

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/artix7/dsp48e1.hlp

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute get\_default\_platform

INFO: [HLS 200-100] Command get\_default\_platform returned 0; 0 sec.

INFO: [HLS 200-100] Execute config\_chip\_info -quiet -resource {SLICE 15850} {LUT 63400} {FF 126800} {DSP48E 240} {BRAM 270}

INFO: [HLS 200-100] Command config\_chip\_info returned 0; 0 sec.

INFO: [HLS 200-100] Execute config\_chip\_info -quiet -speed medium

INFO: [HLS 200-100] Command config\_chip\_info returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/xilinx.hlp

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/target\_info.tcl

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/xilinx\_interface.hlp

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/maxi.hlp

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/saxilite.hlp

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/dsp48.hlp

INFO: [HLS 200-100] Command ap\_source returned 0; 0.01 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0.01 sec.

INFO: [HLS 200-100] Command import\_lib returned 0; 0.02 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/artix7/artix7.gen

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/virtex.gen

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/xilinx.gen

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/plb46.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/fsl.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/axi4.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/nativeAXI4.gen

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/saxilite.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/maxi.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0.01 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0.01 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/scripts/xilinxcoregen.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/XilEDKCoreGen.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/ip/dds\_compiler.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/ip/xfft.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0.08 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/ip/xfir.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0.01 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/ip/util.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0.11 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/dsp48.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0.11 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0.11 sec.

INFO: [HLS 200-100] Execute set\_part xc7a35tcpg236-3

INFO: [HLS 200-100] Execute add\_library xilinx/artix7/artix7:xc7a35t:cpg236:-3

INFO: [HLS 200-100] Execute get\_default\_platform

INFO: [HLS 200-100] Command get\_default\_platform returned 0; 0 sec.

INFO: [HLS 200-100] Execute license\_isbetapart xc7a35t

INFO: [HLS 200-100] Command license\_isbetapart returned 1; 0.01 sec.

INFO: [HLS 200-100] Execute get\_default\_platform

INFO: [HLS 200-100] Command get\_default\_platform returned 0; 0 sec.

INFO: [HLS 200-100] Execute config\_chip\_info -quiet -resource {SLICE 5200} {LUT 20800} {FF 41600} {DSP48E 90} {BRAM 100}

INFO: [HLS 200-100] Command config\_chip\_info returned 0; 0 sec.

INFO: [HLS 200-100] Execute config\_chip\_info -quiet -speed fast

INFO: [HLS 200-100] Command config\_chip\_info returned 0; 0 sec.

INFO: [HLS 200-100] Command add\_library returned 0; 0.01 sec.

INFO: [HLS 200-100] Execute add\_library xilinx/artix7/artix7\_fpv6

INFO: [HLS 200-100] Execute get\_default\_platform

INFO: [HLS 200-100] Command get\_default\_platform returned 0; 0 sec.

INFO: [HLS 200-100] Execute open\_platform DefaultPlatform

INFO: [HLS 200-100] Command open\_platform returned 0; 0 sec.

INFO: [HLS 200-100] Execute import\_lib /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/artix7/artix7\_fpv6

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/xilinx\_fpv7.lib

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/xilinx\_hp.lib

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0.01 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/xilinx\_fpv.hlp

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/xilinx.hlp

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/target\_info.tcl

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/xilinx\_interface.hlp

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/maxi.hlp

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/saxilite.hlp

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/dsp48.hlp

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/artix7/artix7\_hp.hlp

INFO: [HLS 200-100] Command ap\_source returned 0; 0.01 sec.

INFO: [HLS 200-100] Command import\_lib returned 0; 0.02 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/artix7/artix7\_fpv6.gen

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/xilinx\_fpv6.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Command add\_library returned 0; 0.02 sec.

INFO: [HLS 200-10] Setting target device to 'xc7a35tcpg236-3'

INFO: [HLS 200-100] Execute get\_default\_platform

INFO: [HLS 200-100] Command get\_default\_platform returned 0; 0 sec.

INFO: [HLS 200-100] Command set\_part returned 0; 0.08 sec.

INFO: [HLS 200-100] Execute get\_default\_platform

INFO: [HLS 200-100] Command get\_default\_platform returned 0; 0 sec.

INFO: [HLS 200-100] Execute config\_chip\_info -quiet -resource {SLICE 5200} {LUT 20800} {FF 41600} {DSP48E 90} {BRAM 100}

INFO: [HLS 200-100] Command config\_chip\_info returned 0; 0 sec.

INFO: [HLS 200-100] Execute config\_chip\_info -quiet -speed fast

INFO: [HLS 200-100] Command config\_chip\_info returned 0; 0 sec.

INFO: [HLS 200-100] Command open\_solution returned 0; 0.22 sec.

INFO: [HLS 200-100] Execute set\_part xc7a35tcpg236-3

INFO: [HLS 200-100] Execute add\_library xilinx/artix7/artix7:xc7a35t:cpg236:-3

INFO: [HLS 200-100] Execute get\_default\_platform

INFO: [HLS 200-100] Command get\_default\_platform returned 0; 0 sec.

INFO: [HLS 200-100] Execute license\_isbetapart xc7a35t

INFO: [HLS 200-100] Command license\_isbetapart returned 1; 0 sec.

INFO: [HLS 200-100] Execute get\_default\_platform

INFO: [HLS 200-100] Command get\_default\_platform returned 0; 0 sec.

INFO: [HLS 200-100] Execute config\_chip\_info -quiet -resource {SLICE 5200} {LUT 20800} {FF 41600} {DSP48E 90} {BRAM 100}

INFO: [HLS 200-100] Command config\_chip\_info returned 0; 0 sec.

INFO: [HLS 200-100] Execute config\_chip\_info -quiet -speed fast

INFO: [HLS 200-100] Command config\_chip\_info returned 0; 0 sec.

INFO: [HLS 200-100] Command add\_library returned 0; 0 sec.

INFO: [HLS 200-100] Execute add\_library xilinx/artix7/artix7\_fpv6

INFO: [HLS 200-100] Execute get\_default\_platform

INFO: [HLS 200-100] Command get\_default\_platform returned 0; 0 sec.

INFO: [HLS 200-100] Execute open\_platform DefaultPlatform

INFO: [HLS 200-100] Command open\_platform returned 0; 0 sec.

INFO: [HLS 200-100] Execute import\_lib /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/artix7/artix7\_fpv6

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/xilinx\_fpv7.lib

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/xilinx\_hp.lib

INFO: [HLS 200-100] Command ap\_source returned 0; 0.01 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0.01 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/xilinx\_fpv.hlp

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/xilinx.hlp

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/target\_info.tcl

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/xilinx\_interface.hlp

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/maxi.hlp

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/saxilite.hlp

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/dsp48.hlp

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/artix7/artix7\_hp.hlp

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Command import\_lib returned 0; 0.02 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/artix7/artix7\_fpv6.gen

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/xilinx\_fpv6.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Command add\_library returned 0; 0.02 sec.

INFO: [HLS 200-100] Execute get\_default\_platform

INFO: [HLS 200-100] Command get\_default\_platform returned 0; 0 sec.

INFO: [HLS 200-100] Command set\_part returned 0; 0.07 sec.

INFO: [HLS 200-100] Execute create\_clock -period 10 -name default

INFO: [HLS 200-100] Execute config\_clock -quiet -name default -period 10 -default=false

INFO: [SYN 201-201] Setting up clock 'default' with a period of 10ns.

INFO: [HLS 200-100] Command config\_clock returned 0; 0 sec.

INFO: [HLS 200-100] Command create\_clock returned 0; 0 sec.

INFO: [HLS 200-100] Execute source ./MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/directives.tcl

INFO: [HLS 200-100] Execute set\_directive\_array\_partition -type complete -dim 2 matrixmul a,b

INFO: [HLS 200-0] Setting directive 'ARRAY\_PARTITION' partition=positionBooleanCmd variable=positionBooleanTextRequireda,b complete=positionBoolean0type dim=2

INFO: [HLS 200-100] Command set\_directive\_array\_partition returned 0; 0 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute csynth\_design

INFO: [HLS 200-100] Execute elaborate -effort=medium -skip\_syncheck=0 -keep\_printf=0 -lm=0 -skip\_cdt=0 -skip\_transform=0 -ng=0 -g=0 -opt\_fp=0

INFO: [HLS 200-10] Analyzing design file '../../../../../../home/drsatya/Desktop/lab1/mat\_pipline\_3.cpp' ...

INFO: [HLS 200-0] Compiling one TU...

INFO: [HLS 200-100] Execute is\_m\_axi\_addr64

INFO: [HLS 200-100] Command is\_m\_axi\_addr64 returned 0; 0 sec.

INFO: [HLS 200-0] Handling ../../../../../../home/drsatya/Desktop/lab1/mat\_pipline\_3.cpp as C++

INFO: [HLS 200-0] Syntax Checking before pre-processing...

INFO: [HLS 200-100] Execute clang -fno-limit-debug-info -gcc-toolchain "/opt/Xilinx/Vivado\_HLS/2017.2/lnx64/tools/gcc" -hls -fno-math-errno -c -emit-llvm -O0 -mllvm -disable-llvm-optzns -fno-threadsafe-statics -fno-use-cxa-atexit -fno-threadsafe-statics -fno-use-cxa-atexit -D\_\_CLANG\_3\_1\_\_ -I "/opt/Xilinx/Vivado\_HLS/2017.2/lnx64/tools/systemc/include" -I "/opt/Xilinx/Vivado\_HLS/2017.2/include" -I "/opt/Xilinx/Vivado\_HLS/2017.2/include/ap\_sysc" -fexceptions -I "/opt/Xilinx/Vivado\_HLS/2017.2/common/technology/autopilot" -include etc/autopilot\_ssdm\_op.h "../../../../../../home/drsatya/Desktop/lab1/mat\_pipline\_3.cpp" -o "/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/mat\_pipline\_3.pp.00.o"

INFO: [HLS 200-0] exec clang -fno-limit-debug-info -gcc-toolchain /opt/Xilinx/Vivado\_HLS/2017.2/lnx64/tools/gcc -hls -fno-math-errno -c -emit-llvm -O0 -mllvm -disable-llvm-optzns -fno-threadsafe-statics -fno-use-cxa-atexit -fno-threadsafe-statics -fno-use-cxa-atexit -D\_\_CLANG\_3\_1\_\_ -I /opt/Xilinx/Vivado\_HLS/2017.2/lnx64/tools/systemc/include -I /opt/Xilinx/Vivado\_HLS/2017.2/include -I /opt/Xilinx/Vivado\_HLS/2017.2/include/ap\_sysc -fexceptions -I /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/autopilot -include etc/autopilot\_ssdm\_op.h ../../../../../../home/drsatya/Desktop/lab1/mat\_pipline\_3.cpp -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/mat\_pipline\_3.pp.00.o

INFO: [HLS 200-100] Command clang returned 0; 0.06 sec.

INFO: [HLS 200-100] Execute is\_encrypted /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/mat\_pipline\_3.pp.00.o

INFO: [HLS 200-100] Command is\_encrypted returned 0; 0 sec.

INFO: [HLS 200-0] Source preprocessing

INFO: [HLS 200-100] Execute clang -fno-limit-debug-info -gcc-toolchain "/opt/Xilinx/Vivado\_HLS/2017.2/lnx64/tools/gcc" -hls -fno-exceptions -D\_\_llvm\_\_ -CC -E "../../../../../../home/drsatya/Desktop/lab1/mat\_pipline\_3.cpp" -fno-math-errno -c -emit-llvm -O0 -mllvm -disable-llvm-optzns -fno-threadsafe-statics -fno-use-cxa-atexit -fno-threadsafe-statics -fno-use-cxa-atexit -D\_\_CLANG\_3\_1\_\_ -DAESL\_SYN -D\_\_SYNTHESIS\_\_ -D\_\_HLS\_SYN\_\_ -I "/opt/Xilinx/Vivado\_HLS/2017.2/common/technology/autopilot" -I "/opt/Xilinx/Vivado\_HLS/2017.2/common/technology/autopilot/ap\_sysc" -include etc/autopilot\_ssdm\_op.h -o "/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/mat\_pipline\_3.pp.0.cpp"

INFO: [HLS 200-0] exec clang -fno-limit-debug-info -gcc-toolchain /opt/Xilinx/Vivado\_HLS/2017.2/lnx64/tools/gcc -hls -fno-exceptions -D\_\_llvm\_\_ -CC -E ../../../../../../home/drsatya/Desktop/lab1/mat\_pipline\_3.cpp -fno-math-errno -c -emit-llvm -O0 -mllvm -disable-llvm-optzns -fno-threadsafe-statics -fno-use-cxa-atexit -fno-threadsafe-statics -fno-use-cxa-atexit -D\_\_CLANG\_3\_1\_\_ -DAESL\_SYN -D\_\_SYNTHESIS\_\_ -D\_\_HLS\_SYN\_\_ -I /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/autopilot -I /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/autopilot/ap\_sysc -include etc/autopilot\_ssdm\_op.h -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/mat\_pipline\_3.pp.0.cpp

INFO: [HLS 200-100] Command clang returned 0; 0.05 sec.

INFO: [HLS 200-0] GCC PP time: 0 seconds per iteration

INFO: [HLS 200-0] Setting directive 'ARRAY\_PARTITION' partition=positionBooleanCmd variable=positionBooleanTextRequireda,b complete=positionBoolean0type dim=2

INFO: [HLS 200-100] Execute list\_core -type functional\_unit

INFO: [HLS 200-100] Command list\_core returned 0; 0 sec.

INFO: [HLS 200-0] CDT Preprocessing...

INFO: [HLS 200-0] Marker-Pragma convertor: /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/mat\_pipline\_3.pp.0.cpp /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/mat\_pipline\_3.pp.0.cpp.ap-line.cpp /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/mat\_pipline\_3.pp.0.cpp.ap-line.cpp.CXX 1

INFO: [HLS 200-0] Converting Markers to Pragmas...

INFO: [HLS 200-100] Execute cdt "/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/mat\_pipline\_3.pp.0.cpp.ap-line.cpp" -m "matrixmul" -o "/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/mat\_pipline\_3.pp.0.cpp.ap-cdt.cpp" --pp --directive /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/solution1.directive --source /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/../../../../../../home/drsatya/Desktop/lab1/mat\_pipline\_3.cpp --error /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db --funcunit "AddSub AddSub\_DSP AddSubnS DAddSub\_fulldsp DAddSub\_nodsp DDiv DExp\_fulldsp DExp\_meddsp DExp\_nodsp DLog\_fulldsp DLog\_meddsp DLog\_nodsp DMul\_fulldsp DMul\_maxdsp DMul\_meddsp DMul\_nodsp DRSqrt DRecip DSqrt DivnS FAddSub\_fulldsp FAddSub\_nodsp FDiv FExp\_fulldsp FExp\_meddsp FExp\_nodsp FLog\_fulldsp FLog\_meddsp FLog\_nodsp FMul\_fulldsp FMul\_maxdsp FMul\_meddsp FMul\_nodsp FRSqrt\_fulldsp FRSqrt\_nodsp FRecip\_fulldsp FRecip\_nodsp FSqrt HAddSub\_fulldsp HAddSub\_meddsp HAddSub\_nodsp HDiv HMul\_fulldsp HMul\_maxdsp HMul\_nodsp HSqrt Mul Mul2S Mul3S Mul4S Mul5S Mul6S Mul\_LUT MulnS MuxnS" --ve --vetcl /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db --ca --es --gf --pd --p2d /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db --sd --scff /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/.systemc\_flag --ad

INFO: [HLS 200-100] Command cdt returned 0; 1.06 sec.

INFO: [HLS 200-0] Marker-Pragma convertor: /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/mat\_pipline\_3.pp.0.cpp.ap-cdt.cpp /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/mat\_pipline\_3.pragma.0.cpp /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/mat\_pipline\_3.pragma.0.cpp.ap-line.CXX 0

INFO: [HLS 200-0] Converting Pragmas to Markers...

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/pragma.status.tcl

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-0] Pragma Handling...

INFO: [HLS 200-0] Source preprocessing

INFO: [HLS 200-100] Execute clang -fno-limit-debug-info -gcc-toolchain "/opt/Xilinx/Vivado\_HLS/2017.2/lnx64/tools/gcc" -hls -fno-exceptions -D\_\_llvm\_\_ -CC -E "/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/mat\_pipline\_3.pragma.1.cpp" -fno-math-errno -c -emit-llvm -O0 -mllvm -disable-llvm-optzns -fno-threadsafe-statics -fno-use-cxa-atexit -fno-threadsafe-statics -fno-use-cxa-atexit -D\_\_CLANG\_3\_1\_\_ -DAESL\_SYN -D\_\_SYNTHESIS\_\_ -D\_\_HLS\_SYN\_\_ -I "/opt/Xilinx/Vivado\_HLS/2017.2/common/technology/autopilot" -I "/opt/Xilinx/Vivado\_HLS/2017.2/common/technology/autopilot/ap\_sysc" -include etc/autopilot\_ssdm\_op.h -o "/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/mat\_pipline\_3.pragma.2.cpp"

INFO: [HLS 200-0] exec clang -fno-limit-debug-info -gcc-toolchain /opt/Xilinx/Vivado\_HLS/2017.2/lnx64/tools/gcc -hls -fno-exceptions -D\_\_llvm\_\_ -CC -E /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/mat\_pipline\_3.pragma.1.cpp -fno-math-errno -c -emit-llvm -O0 -mllvm -disable-llvm-optzns -fno-threadsafe-statics -fno-use-cxa-atexit -fno-threadsafe-statics -fno-use-cxa-atexit -D\_\_CLANG\_3\_1\_\_ -DAESL\_SYN -D\_\_SYNTHESIS\_\_ -D\_\_HLS\_SYN\_\_ -I /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/autopilot -I /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/autopilot/ap\_sysc -include etc/autopilot\_ssdm\_op.h -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/mat\_pipline\_3.pragma.2.cpp

INFO: [HLS 200-100] Command clang returned 0; 0.05 sec.

INFO: [HLS 200-0] Processing labels

INFO: [HLS 200-100] Execute clang -fno-limit-debug-info -gcc-toolchain /opt/Xilinx/Vivado\_HLS/2017.2/lnx64/tools/gcc -hls -hls-analyze-label -hls-analyze-pragma -fno-exceptions -D\_\_llvm\_\_ -w "/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/mat\_pipline\_3.pragma.2.cpp" -fno-math-errno -c -emit-llvm -O0 -mllvm -disable-llvm-optzns -fno-threadsafe-statics -fno-use-cxa-atexit -DAESL\_SYN -D\_\_SYNTHESIS\_\_ -D\_\_HLS\_SYN\_\_ -I "/opt/Xilinx/Vivado\_HLS/2017.2/common/technology/autopilot" -I "/opt/Xilinx/Vivado\_HLS/2017.2/common/technology/autopilot/ap\_sysc" -include etc/autopilot\_ssdm\_op.h -g -o "/opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/mat\_pipline\_3.g.bc"

INFO: [HLS 200-0] exec clang -fno-limit-debug-info -gcc-toolchain /opt/Xilinx/Vivado\_HLS/2017.2/lnx64/tools/gcc -hls -hls-analyze-label -hls-analyze-pragma -fno-exceptions -D\_\_llvm\_\_ -w /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/mat\_pipline\_3.pragma.2.cpp -fno-math-errno -c -emit-llvm -O0 -mllvm -disable-llvm-optzns -fno-threadsafe-statics -fno-use-cxa-atexit -DAESL\_SYN -D\_\_SYNTHESIS\_\_ -D\_\_HLS\_SYN\_\_ -I /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/autopilot -I /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/autopilot/ap\_sysc -include etc/autopilot\_ssdm\_op.h -g -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/mat\_pipline\_3.g.bc

INFO: [HLS 200-100] Command clang returned 0; 0.06 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/ve\_warning.tcl

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-10] Validating synthesis directives ...

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/pragma.status.tcl

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-111] Finished Checking Pragmas Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 352.020 ; gain = 12.590 ; free physical = 686 ; free virtual = 5518

INFO: [HLS 200-0] Linking Release ...

INFO: [HLS 200-100] Execute llvm-ld /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/mat\_pipline\_3.bc -disable-opt -L/opt/Xilinx/Vivado\_HLS/2017.2/lnx64/lib -lm\_basic -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.o

INFO: [HLS 200-100] Command llvm-ld returned 0; 0.02 sec.

INFO: [HLS 200-100] Execute disassemble /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.o

INFO: [HLS 200-100] Execute is\_encrypted /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.o.bc

INFO: [HLS 200-100] Command is\_encrypted returned 0; 0 sec.

INFO: [HLS 200-100] Command disassemble returned 0; 0.02 sec.

INFO: [HLS 200-0] Disassemble time: 0 seconds per iteration

INFO: [HLS 200-0] Linking Debug ...

INFO: [HLS 200-100] Execute llvm-ld /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/mat\_pipline\_3.g.bc -disable-opt -L/opt/Xilinx/Vivado\_HLS/2017.2/lnx64/lib -lm\_basic -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.g

INFO: [HLS 200-100] Command llvm-ld returned 0; 0.03 sec.

INFO: [HLS 200-100] Execute disassemble /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.g /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.g

INFO: [HLS 200-100] Execute is\_encrypted /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.g.bc

INFO: [HLS 200-100] Command is\_encrypted returned 0; 0 sec.

INFO: [HLS 200-100] Command disassemble returned 0; 0.02 sec.

INFO: [HLS 200-0] Disassemble time: 0 seconds per iteration

INFO: [HLS 200-111] Finished Linking Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 352.020 ; gain = 12.590 ; free physical = 685 ; free virtual = 5518

INFO: [HLS 200-100] Execute opt\_and\_import\_c a -opt\_level=2 -skip\_syncheck=0 -ng=0 -keep\_printf=0

INFO: [HLS 200-100] Execute cleanup\_all\_models

INFO: [HLS 200-100] Command cleanup\_all\_models returned 0; 0 sec.

INFO: [HLS 200-10] Starting code transformations ...

INFO: [HLS 200-100] Execute transform -promote-dbg-pointer /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.pp.bc -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.pp.0.bc -f

INFO: [HLS 200-100] Command transform returned 0; 0.01 sec.

INFO: [HLS 200-100] Execute llvm-ld /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.pp.0.bc -disable-opt -L/opt/Xilinx/Vivado\_HLS/2017.2/lnx64/lib -lfloatconversion -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.g.0

INFO: [HLS 200-100] Command llvm-ld returned 0; 0.03 sec.

INFO: [HLS 200-0] Running Standard Transforms...

INFO: [HLS 200-100] Execute transform -hls -share-std-xform -demangle-name -inline-byval-memcpy -always-inline -promote-dbg-pointer -interface-preproc -scalarrepl -mem2reg -keep-read-access -instcombine -dce -promote-dbg-pointer -bitop-raise -loop-simplify -indvarspre -indvars -loop-simplify -xunroll -constprop -instcombine -simplifycfg -indvars -simplifycfg -dce -globaldce -basicaa -simplifycfg -mem2reg -globalopt -global-constprop -deadargelim -instcombine -simplifycfg -prune-eh -simplifycfg -scalarrepl -instcombine -reassociate -licm -simplifycfg -loop-simplify -indvars -instcombine -simplifycfg -mem2reg -loop-simplify -indvars -instcombine -gvn -gvn -instcombine -adce -break-crit-edges -simplifycfg -loop-delete -global-array-opt -dce -dse -adce -find-syn-modules -top matrixmul -deadargelim -mem2reg -instcombine -dce -presyn-prepare -auto-rom-infer -interface-preproc -syn-check -check-rec-only -find-region -simplifycfg -func-extr -function-inline -globaldce -mem2reg -instcombine -dce -gvn -globaldce -adce -adse -constprop -instcombine -bit-constprop -instcombine -dce -simplifycfg -bitop-raise -simplifycfg -dce -loop-delete -reassociate -globalopt -global-privatize -mem2reg -dce -global-constprop -pointer-simplify -constprop -dce -func-inst -deadargelim -auto-shift-reg-idiom -promote-dbg-pointer -norm-name /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.g.0.bc -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.g.1.bc -f -phase std-opt

INFO: [HLS 200-100] Command transform returned 0; 0.01 sec.

INFO: [HLS 200-100] Execute disassemble /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.g.1 /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.g.1

INFO: [HLS 200-100] Execute is\_encrypted /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.g.1.bc

INFO: [HLS 200-100] Command is\_encrypted returned 0; 0 sec.

INFO: [HLS 200-100] Command disassemble returned 0; 0.02 sec.

INFO: [HLS 200-111] Finished Standard Transforms Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 352.020 ; gain = 12.590 ; free physical = 685 ; free virtual = 5518

INFO: [HLS 200-10] Checking synthesizability ...

INFO: [HLS 200-0] Checking Synthesizability 1/2..

INFO: [HLS 200-100] Execute transform -hls -syn-check -check-rec-only -disaggr -scalarrepl -norm-name -dce -mem2reg -instcombine -function-uniquify -directive-preproc -mem2reg -dse -dce -auto-rom-infer -dce -array-normalize -instcombine -dce -warn-fifo-pointer -array-seg-normalize -instcombine -dce -array-flatten -instcombine -dce -array-burst -dce -deadargelim -promote-global-argument -simplifycfg -mem2reg -globaldce -resolve-double-ptr -dce -deadargelim -dce -instcombine -function-inline -globaldce -dce -doublePtrSimplify -doublePtrElim -dce -doublePtrSimplify -promote-dbg-pointer -dce -scalarrepl -dse -adse -instcombine -ptrLegalization -simplifycfg -dce -instcombine -pointer-simplify -ptrArgReplace -dce -instcombine -disaggr -scalarrepl -norm-name -dce -mem2reg -instcombine -ptrLegalization -simplifycfg -deadargelim -instcombine -dce -inst-simplify -function-uniquify -directive-preproc -mem2reg -dse -dce -globaldce /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.g.1.bc -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.g.2.prechk.bc -f

INFO: [HLS 200-100] Command transform returned 0; 0.01 sec.

INFO: [HLS 200-0] Checking Synthesizability 2/2..

INFO: [HLS 200-100] Execute transform -syn-check /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.g.2.prechk.bc -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.g.2.bc -f -phase syn-check

INFO: [HLS 200-100] Command transform returned 0; 0.01 sec.

INFO: [HLS 200-111] Finished Checking Synthesizability Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 352.020 ; gain = 12.590 ; free physical = 685 ; free virtual = 5518

INFO: [HLS 200-0] Compiler optimizing ...

INFO: [HLS 200-0] Share syncheck's 1.bc for syn flow: copy /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.g.1.bc to /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.o.1.bc

INFO: [HLS 200-0] Presyn 1...

INFO: [HLS 200-100] Execute transform -hls -tmp /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db -interface-port-rename -type-info -function-uniquify -directive-preproc -mem2reg -dse -dce -disaggr -scalarrepl -norm-name -deadargelim -mem2reg -instcombine -dce -auto-rom-infer -dce -function-uniquify -resource-proc -simplifycfg -mem2reg -globaldce -resolve-double-ptr -dce -deadargelim -dce -instcombine -clib-intrinsic-prepare -dce -func-buffer -dce -array-normalize -func-legal -instcombine -gvn -constprop -dce -ptrArgReplace -mem2reg -instcombine -dce -array-seg-normalize -deadargelim -instcombine -dce -pointer-simplify -dce -port-alignment -dce -interface-preproc -data-pack -instcombine -dce -basicaa -aggr-aa -aggrmodref-aa -aggr-aa -gvn -gvn -basicaa -aggr-aa -aggrmodref-aa -aggr-aa -dse -adse -adce -loop-simplify -indvars -instcombine -gvn -loop-simplify -mem2reg -dce -simplifycfg -find-region -instcombine -auto-loop-pipeline -inst-simplify -interface-preproc -cfgopt -instcombine -indvars -auto-loop-unroll -loop-simplify -loop-bound -xunroll -constprop -instcombine -simplifycfg -indvars -simplifycfg -dce -globaldce -clean-region -attach-range -gvn -inst-simplify -constprop -simplifycfg -dce -pointer-simplify -dce -globalopt -constprop -dce -array-promote -constprop -instcombine -dce -ptrArgReplace -mem2reg -instcombine -simplifycfg -dce -auto-par -instcombine -dce -array-transform-check -array-reshape -instcombine -simplifycfg -dce -ptrArgReplace -deadargelim -mem2reg -instcombine -simplifycfg -dce -indvars -loop-simplify -loop-bound -xunroll -constprop -instcombine -simplifycfg -indvars -simplifycfg -dce -globaldce -duplicate-dataflow-processes -globaldce -instcombine -array-partition -instcombine -simplifycfg -dce -ptrArgReplace -global-constprop -deadargelim -mem2reg -func-legal -instcombine -dce -global-constprop -deadargelim -mem2reg -instcombine -simplifycfg -dce -globalopt -constprop -dce -array-promote -constprop -instcombine -dce -ptrArgReplace -mem2reg -instcombine -simplifycfg -dce -mem-intrinsic-preproc -dce -global-privatize -mem2reg -globaldce -promote-global-argument -ptrArgReplace -mem2reg -instcombine -dce -globalopt -mergereturn -simplify-global-access -mem2reg -dce -pointer-simplify -dce -functionattrs -basicaa -aggr-aa -aggrmodref-aa -aggr-aa -gvn -gvn -basicaa -aggr-aa -aggrmodref-aa -aggr-aa -dse -adse -adce -inst-simplify -dce -norm-name -function-inline -globaldce -func-inst -constprop -instcombine -simplifycfg -dce -func-legal -dce -loop-bound -arraycheck -bitwidthmin -on-by-dataflow -loop-delete -instcombine -simplifycfg -globaldce -dce -gvn -deadargelim -dce -loop-simplify -clean-region -simplifycfg -propagate-stable-arguments -loop-stream -instcombine -simplifycfg -dce -globaldce -stream-intrinsic-preproc -dce -check-ap-stream -loop-simplify -eliminate-keepreads -extract-dataflow-in-loop -loop-simplify -dce -gvn -deadargelim -dse -check-dataflow-syntax -legalize-stream-variable -legalize-global -extract-subproc -dce -dead-channel-elimination -canonicalize-gep -globaldce -dce -gvn -deadargelim -annotate-dataflow-channels -scalar-propagation -deadargelim -globaldce -mem2reg -check-dataflow-channels -function-stream -dce -globaldce -prop-fifo-spec -internal-stream-gen -canonicalize-gep -globaldce -dce -gvn -deadargelim -mergereturn -indvars -loop-simplify -instcombine -array-stream -array-seg-normalize -array-partition -func-legal -instcombine -simplifycfg -dce -bundle-memfifo-ops -deadargelim -function-uniquify -directive-preproc -mem2reg -dse -dce -group-axi-access -licm -simplifycfg -dce -loop-delete -norm-name /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.o.1.bc -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.o.1.tmp.bc -f

INFO: [XFORM 203-502] Unrolling all sub-loops inside loop 'Col' (../../../../../../home/drsatya/Desktop/lab1/mat\_pipline\_3.cpp:14) in function 'matrixmul' for pipelining.

INFO: [XFORM 203-501] Unrolling loop 'Product' (../../../../../../home/drsatya/Desktop/lab1/mat\_pipline\_3.cpp:18) in function 'matrixmul' completely.

INFO: [XFORM 203-101] Partitioning array 'a' (../../../../../../home/drsatya/Desktop/lab1/mat\_pipline\_3.cpp:5) in dimension 2 completely.

INFO: [XFORM 203-101] Partitioning array 'b' (../../../../../../home/drsatya/Desktop/lab1/mat\_pipline\_3.cpp:6) in dimension 2 completely.

INFO: [HLS 200-100] Command transform returned 0; 0.04 sec.

INFO: [HLS 200-0] Presyn 2...

INFO: [HLS 200-100] Execute transform -hls -keep-callgraph -scalarrepl -mem2reg -port-alignment -attach-range -dce -pipe-mux-gen -indvars -loop-bound -inst-simplify -instcombine -dce -merge-array-access -mem2reg -dce -clean-region -mergereturn -if-conv -instcombine -dce -constprop -basicaa -aggr-aa -aggrmodref-aa -aggr-aa -gvn -gvn -basicaa -aggr-aa -aggrmodref-aa -aggr-aa -dse -adse -adce -scalarrepl -mem2reg -global-constprop -deadargelim -deadargelim -instcombine -dce -simplifycfg -ptrArgReplace -mem2reg -function-inline -globaldce -mem2reg -instcombine -dce -expr-balance -instcombine -dce -bitwidthmin -interface-preproc -directive-preproc -inst-rectify -instcombine -dce -functionattrs -constprop -instcombine -bit-constprop -simplify-global-access -globalopt -globaldce -inst-simplify -instcombine -elimdeaddata -dce -loop-delete -simplifycfg -loop-simplify -auto-burst -norm-name /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.o.1.tmp.bc -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.o.2.bc -f -phase presyn

INFO: [HLS 200-100] Command transform returned 0; 0.04 sec.

INFO: [HLS 200-100] Execute disassemble /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.o.2 /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.o.2

INFO: [HLS 200-100] Execute is\_encrypted /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.o.2.bc

INFO: [HLS 200-100] Command is\_encrypted returned 0; 0 sec.

INFO: [HLS 200-100] Command disassemble returned 0; 0.02 sec.

INFO: [HLS 200-111] Finished Pre-synthesis Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 480.016 ; gain = 140.586 ; free physical = 665 ; free virtual = 5498

INFO: [HLS 200-0] Building ssdm...

INFO: [HLS 200-100] Execute transform -hls -function-uniquify -auto-function-inline -globaldce -ptrArgReplace -mem2reg -instcombine -dce -reset-lda -loop-simplify -indvars -licm -loop-dep -loop-bound -licm -loop-simplify -flattenloopnest -array-flatten -gvn -instcombine -dce -array-map -dce -func-legal -gvn -adce -instcombine -cfgopt -simplifycfg -loop-simplify -array-burst -promote-global-argument -dce -axi4-lower -array-seg-normalize -basicaa -aggrmodref-aa -globalsmodref-aa -aggr-aa -gvn -gvn -basicaa -aggrmodref-aa -globalsmodref-aa -aggr-aa -dse -adse -adce -licm -inst-simplify -dce -globaldce -instcombine -array-stream -eliminate-keepreads -instcombine -dce -deadargelim -doublePtrSimplify -doublePtrElim -dce -doublePtrSimplify -promote-dbg-pointer -dce -scalarrepl -mem2reg -disaggr -norm-name -mem2reg -instcombine -dse -adse -adce -ptrLegalization -dce -auto-rom-infer -array-flatten -dce -instcombine -check-doubleptr -loop-rot -constprop -cfgopt -simplifycfg -loop-simplify -indvars -pointer-simplify -dce -loop-bound -loop-simplify -loop-preproc -constprop -global-constprop -gvn -mem2reg -instcombine -dce -loop-bound -loop-merge -dce -bitwidthmin -deadargelim -dce -canonicalize-dataflow -dce -scalar-propagation -deadargelim -globaldce -mem2reg -interface-preproc -interface-gen -deadargelim -directive-preproc -inst-simplify -dce -gvn -mem2reg -instcombine -dce -adse -loop-bound -instcombine -cfgopt -simplifycfg -loop-simplify -clean-region -io-protocol -find-region -mem2reg -bitop-raise -inst-simplify -inst-rectify -instcombine -adce -deadargelim -loop-simplify -phi-opt -bitop-raise -cfgopt -simplifycfg -strip-dead-prototypes -interface-lower -bitop-lower -intrinsic-lower -auto-function-inline -basicaa -aggrmodref-aa -globalsmodref-aa -aggr-aa -inst-simplify -simplifycfg -loop-simplify -mergereturn -inst-simplify -inst-rectify -dce -bitop-lower -loop-rewind -pointer-simplify -dce -cfgopt -read-loop-dep -dce -bitwidth -loop-dep -norm-name -legalize -validate-dataflow -cdfg-build /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.o.2.bc -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.o.3.bc -f -phase build-ssdm

INFO: [XFORM 203-541] Flattening a loop nest 'Row' (../../../../../../home/drsatya/Desktop/lab1/mat\_pipline\_3.cpp:11:36) in function 'matrixmul'.

INFO: [HLS 200-100] Command transform returned 0; 0.06 sec.

INFO: [HLS 200-100] Execute disassemble /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.o.3 /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.o.3

INFO: [HLS 200-100] Execute is\_encrypted /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.o.3.bc

INFO: [HLS 200-100] Command is\_encrypted returned 0; 0 sec.

INFO: [HLS 200-100] Command disassemble returned 0; 0.02 sec.

INFO: [HLS 200-111] Finished Architecture Synthesis Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 480.016 ; gain = 140.586 ; free physical = 674 ; free virtual = 5507

INFO: [HLS 200-0] Finish building internal data model.

INFO: [HLS 200-100] Command opt\_and\_import\_c returned 0; 0.28 sec.

INFO: [HLS 200-100] Command elaborate returned 0; 1.87 sec.

INFO: [HLS 200-100] Execute autosyn

INFO: [HLS 200-10] Starting hardware synthesis ...

INFO: [HLS 200-0] Synthesizing C/C++ design ...

INFO: [HLS 200-10] Synthesizing 'matrixmul' ...

INFO: [HLS 200-100] Execute ap\_set\_top\_model matrixmul

INFO: [HLS 200-100] Command ap\_set\_top\_model returned 0; 0 sec.

INFO: [HLS 200-100] Execute get\_model\_list matrixmul -filter all-wo-channel -topdown

INFO: [HLS 200-100] Command get\_model\_list returned 0; 0 sec.

INFO: [HLS 200-100] Execute preproc\_iomode -model matrixmul

INFO: [HLS 200-100] Command preproc\_iomode returned 0; 0 sec.

INFO: [HLS 200-100] Execute get\_model\_list matrixmul -filter all-wo-channel

INFO: [HLS 200-100] Command get\_model\_list returned 0; 0 sec.

INFO: [HLS 200-0] Model list for configure: matrixmul

INFO: [HLS 200-0] Configuring Module : matrixmul ...

INFO: [HLS 200-100] Execute set\_default\_model matrixmul

INFO: [HLS 200-100] Command set\_default\_model returned 0; 0 sec.

INFO: [HLS 200-100] Execute apply\_spec\_resource\_limit matrixmul

INFO: [HLS 200-100] Command apply\_spec\_resource\_limit returned 0; 0 sec.

INFO: [HLS 200-0] Model list for preprocess: matrixmul

INFO: [HLS 200-0] Preprocessing Module: matrixmul ...

INFO: [HLS 200-100] Execute set\_default\_model matrixmul

INFO: [HLS 200-100] Command set\_default\_model returned 0; 0 sec.

INFO: [HLS 200-100] Execute cdfg\_preprocess -model matrixmul

INFO: [HLS 200-100] Command cdfg\_preprocess returned 0; 0 sec.

INFO: [HLS 200-100] Execute rtl\_gen\_preprocess matrixmul

INFO: [HLS 200-100] Command rtl\_gen\_preprocess returned 0; 0.01 sec.

INFO: [HLS 200-0] Model list for synthesis: matrixmul

INFO: [HLS 200-10] ----------------------------------------------------------------

INFO: [HLS 200-10] -- Implementing module 'matrixmul'

INFO: [HLS 200-10] ----------------------------------------------------------------

INFO: [HLS 200-100] Execute set\_default\_model matrixmul

INFO: [HLS 200-100] Command set\_default\_model returned 0; 0 sec.

INFO: [HLS 200-100] Execute schedule -model matrixmul

INFO: [SCHED 204-11] Starting scheduling ...

INFO: [SCHED 204-61] Pipelining loop 'Row\_Col'.

WARNING: [SCHED 204-69] Unable to schedule 'load' operation ('b\_0\_load\_1') on array 'b\_0' due to limited memory ports.

INFO: [SCHED 204-61] Pipelining result: Target II: 1, Final II: 2, Depth: 4.

INFO: [SCHED 204-11] Finished scheduling.

INFO: [HLS 200-100] Command schedule returned 0; 0.05 sec.

INFO: [HLS 200-111] Elapsed time: 2.45 seconds; current allocated memory: 0.318 MB.

INFO: [HLS 200-100] Execute report -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/matrixmul.verbose.sched.rpt -verbose -f

INFO: [HLS 200-100] Command report returned 0; 0 sec.

INFO: [HLS 200-100] Execute db\_write -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/matrixmul.sched.adb -f

INFO: [HLS 200-100] Command db\_write returned 0; 0.01 sec.

INFO: [HLS 200-0] Finish scheduling matrixmul.

INFO: [HLS 200-100] Execute set\_default\_model matrixmul

INFO: [HLS 200-100] Command set\_default\_model returned 0; 0 sec.

INFO: [HLS 200-100] Execute bind -model matrixmul

INFO: [BIND 205-110] clear=

INFO: [BIND 205-110] debug=

INFO: [BIND 205-110] drf=

INFO: [BIND 205-110] effort=

INFO: [BIND 205-110] fast\_refine=

INFO: [BIND 205-110] fu\_weight=[ 0.0 -- 1.0 ]

INFO: [BIND 205-110] global\_opt=

INFO: [BIND 205-110] gsearch=

INFO: [BIND 205-110] help=

INFO: [BIND 205-110] help-hidden=

INFO: [BIND 205-110] min\_mem\_port=

INFO: [BIND 205-110] min\_op=

INFO: [BIND 205-110] minreg=

INFO: [BIND 205-110] ml=

INFO: [BIND 205-110] model=matrixmul

INFO: [BIND 205-110] no\_false\_path=

INFO: [BIND 205-110] no\_min\_op=

INFO: [BIND 205-110] normalize=

INFO: [BIND 205-110] quiet=

INFO: [BIND 205-110] refine=

INFO: [BIND 205-110] reg\_weight=[ 0.0 -- 1.0 ]

INFO: [BIND 205-110] search=

INFO: [BIND 205-110] tight\_delay=

INFO: [BIND 205-110] verbose=

INFO: [BIND 205-110] wFF=

INFO: [BIND 205-110] wFU=

INFO: [BIND 205-110] wMUX=

INFO: [BIND 205-110] wNET=

INFO: [BIND 205-100] Starting micro-architecture generation ...

INFO: [BIND 205-101] Performing variable lifetime analysis.

INFO: [BIND 205-101] Exploring resource sharing.

INFO: [BIND 205-101] Binding ...

INFO: [BIND 205-100] Finished micro-architecture generation.

INFO: [HLS 200-100] Command bind returned 0; 0.01 sec.

INFO: [HLS 200-111] Elapsed time: 0.02 seconds; current allocated memory: 0.318 MB.

INFO: [HLS 200-100] Execute report -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/matrixmul.verbose.bind.rpt -verbose -f

INFO: [HLS 200-100] Command report returned 0; 0.03 sec.

INFO: [HLS 200-100] Execute db\_write -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/matrixmul.bind.adb -f

INFO: [HLS 200-100] Command db\_write returned 0; 0 sec.

INFO: [HLS 200-0] Finish binding matrixmul.

INFO: [HLS 200-100] Execute get\_model\_list matrixmul -filter all-wo-channel

INFO: [HLS 200-100] Command get\_model\_list returned 0; 0 sec.

INFO: [HLS 200-0] Preprocessing for RTLGen ...

INFO: [HLS 200-100] Execute rtl\_gen\_preprocess matrixmul

INFO: [HLS 200-100] Command rtl\_gen\_preprocess returned 0; 0 sec.

INFO: [HLS 200-0] Model list for RTL generation: matrixmul

INFO: [HLS 200-10] ----------------------------------------------------------------

INFO: [HLS 200-10] -- Generating RTL for module 'matrixmul'

INFO: [HLS 200-10] ----------------------------------------------------------------

INFO: [HLS 200-100] Execute create\_rtl\_model matrixmul -vendor xilinx -mg\_file /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/matrixmul.compgen.tcl

INFO: [RTGEN 206-500] Setting interface mode on port 'matrixmul/a\_0' to 'ap\_memory'.

INFO: [RTGEN 206-500] Setting interface mode on port 'matrixmul/a\_1' to 'ap\_memory'.

INFO: [RTGEN 206-500] Setting interface mode on port 'matrixmul/a\_2' to 'ap\_memory'.

INFO: [RTGEN 206-500] Setting interface mode on port 'matrixmul/b\_0' to 'ap\_memory'.

INFO: [RTGEN 206-500] Setting interface mode on port 'matrixmul/b\_1' to 'ap\_memory'.

INFO: [RTGEN 206-500] Setting interface mode on port 'matrixmul/b\_2' to 'ap\_memory'.

INFO: [RTGEN 206-500] Setting interface mode on port 'matrixmul/res' to 'ap\_memory'.

INFO: [RTGEN 206-500] Setting interface mode on function 'matrixmul' to 'ap\_ctrl\_hs'.

INFO: [SYN 201-210] Renamed object name 'matrixmul\_mux\_32\_8\_1' to 'matrixmul\_mux\_32\_bkb' due to the length limit 20

INFO: [SYN 201-210] Renamed object name 'matrixmul\_mac\_muladd\_8s\_8s\_16ns\_16\_1' to 'matrixmul\_mac\_mulcud' due to the length limit 20

INFO: [SYN 201-210] Renamed object name 'matrixmul\_mac\_muladd\_8s\_8s\_16s\_16\_1' to 'matrixmul\_mac\_muldEe' due to the length limit 20

INFO: [RTGEN 206-100] Generating core module 'matrixmul\_mac\_mulcud': 1 instance(s).

INFO: [RTGEN 206-100] Generating core module 'matrixmul\_mac\_muldEe': 1 instance(s).

INFO: [RTGEN 206-100] Generating core module 'matrixmul\_mux\_32\_bkb': 2 instance(s).

INFO: [RTGEN 206-100] Finished creating RTL model for 'matrixmul'.

INFO: [HLS 200-100] Command create\_rtl\_model returned 0; 0.01 sec.

INFO: [HLS 200-111] Elapsed time: 0.05 seconds; current allocated memory: 0.318 MB.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/matrixmul.rtl\_wrap.cfg.tcl

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute gen\_rtl matrixmul -istop -style xilinx -tracefl mytrace -tracefmt vcd -traceopt all -f -lang sc -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/syn/systemc/matrixmul -synmodules matrixmul

INFO: [HLS 200-100] Command gen\_rtl returned 0; 0 sec.

INFO: [HLS 200-100] Execute gen\_rtl matrixmul -istop -style xilinx -f -lang vhdl -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/syn/vhdl/matrixmul

INFO: [HLS 200-100] Command gen\_rtl returned 0; 0.02 sec.

INFO: [HLS 200-100] Execute gen\_rtl matrixmul -istop -style xilinx -f -lang vlog -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/syn/verilog/matrixmul

INFO: [HLS 200-100] Command gen\_rtl returned 0; 0.01 sec.

INFO: [HLS 200-100] Execute export\_constraint\_db -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/matrixmul.constraint.tcl -f -tool general

INFO: [HLS 200-100] Command export\_constraint\_db returned 0; 0 sec.

INFO: [HLS 200-100] Execute report -model matrixmul -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/matrixmul.design.xml -verbose -f -dv

INFO: [HLS 200-100] Command report returned 0; 0.02 sec.

INFO: [HLS 200-100] Execute report -model matrixmul -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/matrixmul.sdaccel.xml -verbose -f -sdaccel

INFO: [HLS 200-100] Command report returned 0; 0.03 sec.

INFO: [HLS 200-100] Execute gen\_tb\_info matrixmul -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/matrixmul -p /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db

INFO: [HLS 200-100] Command gen\_tb\_info returned 0; 0 sec.

INFO: [HLS 200-100] Execute report -model matrixmul -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/syn/report/matrixmul\_csynth.rpt -f

INFO: [HLS 200-100] Command report returned 0; 0.01 sec.

INFO: [HLS 200-100] Execute report -model matrixmul -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/syn/report/matrixmul\_csynth.xml -f -x

INFO: [HLS 200-100] Command report returned 0; 0.02 sec.

INFO: [HLS 200-100] Execute report -model matrixmul -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/matrixmul.verbose.rpt -verbose -f

INFO: [HLS 200-100] Command report returned 0; 0.03 sec.

INFO: [HLS 200-100] Execute db\_write -model matrixmul -o /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/matrixmul.adb -f

INFO: [HLS 200-100] Command db\_write returned 0; 0.01 sec.

INFO: [HLS 200-100] Execute sc\_get\_clocks matrixmul

INFO: [HLS 200-100] Command sc\_get\_clocks returned 0; 0 sec.

INFO: [HLS 200-100] Execute sc\_get\_portdomain matrixmul

INFO: [HLS 200-100] Command sc\_get\_portdomain returned 0; 0 sec.

INFO: [HLS 200-0] Model list for RTL component generation: matrixmul

INFO: [HLS 200-0] Handling components in module [matrixmul] ...

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/matrixmul.compgen.tcl

INFO: [HLS 200-0] Found component matrixmul\_mux\_32\_bkb.

INFO: [HLS 200-0] Append model matrixmul\_mux\_32\_bkb

INFO: [HLS 200-0] Found component matrixmul\_mac\_mulcud.

INFO: [HLS 200-0] Append model matrixmul\_mac\_mulcud

INFO: [HLS 200-0] Found component matrixmul\_mac\_muldEe.

INFO: [HLS 200-0] Append model matrixmul\_mac\_muldEe

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-0] Append model matrixmul

INFO: [HLS 200-0] Generating RTL model list ...

INFO: [HLS 200-0] All models in this session: matrixmul\_mux\_32\_bkb matrixmul\_mac\_mulcud matrixmul\_mac\_muldEe matrixmul

INFO: [HLS 200-0] To file: write model matrixmul\_mux\_32\_bkb

INFO: [HLS 200-0] To file: write model matrixmul\_mac\_mulcud

INFO: [HLS 200-0] To file: write model matrixmul\_mac\_muldEe

INFO: [HLS 200-0] To file: write model matrixmul

INFO: [HLS 200-0] Finished generating RTL model list.

INFO: [HLS 200-0] RTL Generation done.

INFO: [HLS 200-0] CAS Generation done.

INFO: [HLS 200-0] CBC Generation done.

INFO: [HLS 200-100] Execute export\_ssdm /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/a.export.ll

INFO: [HLS 200-100] Command export\_ssdm returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/global.setting.tcl

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/generic/autopilot/common.gen

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/generic/autopilot/APCoreGen.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/generic/autopilot/op.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/generic/autopilot/op\_simcore.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/generic/autopilot/interface.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/global.setting.tcl

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/artix7/artix7.gen

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/virtex.gen

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/xilinx.gen

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/plb46.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0.01 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/fsl.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/axi4.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/nativeAXI4.gen

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/saxilite.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/maxi.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0.01 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0.01 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/scripts/xilinxcoregen.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/interface/XilEDKCoreGen.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0.01 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/ip/dds\_compiler.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/ip/xfft.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0.08 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/ip/xfir.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/ip/util.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0.11 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/dsp48.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0.11 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0.11 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/artix7/artix7\_fpv6.gen

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/common/xilinx\_fpv6.gen

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/global.setting.tcl

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/global.setting.tcl

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/global.setting.tcl

INFO: [HLS 200-100] Command ap\_source returned 0; 0 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/global.setting.tcl

INFO: [HLS 200-100] Command ap\_source returned 0; 0.01 sec.

INFO: [HLS 200-100] Execute source /opt/Xilinx/Vivado\_HLS/2017.2/bin/INTEGER\_MATRIX\_MULTIPLICATION/MATRIX\_MULTIPLICATION\_16\_PIPELINE\_3/solution1/.autopilot/db/matrixmul.compgen.tcl

INFO: [HLS 200-100] Command ap\_source returned 0; 0.02 sec.

INFO: [HLS 200-111] Finished generating all RTL models Time (s): cpu = 00:00:04 ; elapsed = 00:00:03 . Memory (MB): peak = 480.020 ; gain = 140.590 ; free physical = 667 ; free virtual = 5501

INFO: [SYSC 207-301] Generating SystemC RTL for matrixmul.

INFO: [VHDL 208-304] Generating VHDL RTL for matrixmul.

INFO: [VLOG 209-307] Generating Verilog RTL for matrixmul.

INFO: [HLS 200-100] Command autosyn returned 0; 0.44 sec.

INFO: [HLS 200-100] Command csynth\_design returned 0; 2.31 sec.

INFO: [HLS 200-100] Command ap\_source returned 0; 2.61 sec.

INFO: [HLS 200-100] Execute cleanup\_all

INFO: [HLS 200-100] Command cleanup\_all returned 0; 0 sec.