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File generated by Vivado(TM) HLS - High-Level Synthesis from C, C++ and SystemC

Version: 2017.2

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INFO: [SYN 201-201] Setting up clock 'default' with a period of 10ns.

INFO: [HLS 200-10] Setting target device to 'xc7a35tcpg236-3'

INFO: [SYN 201-201] Setting up clock 'default' with a period of 10ns.

INFO: [HLS 200-10] Analyzing design file '../../../../../../home/drsatya/Desktop/lab1/mat\_pipline\_3.cpp' ...

INFO: [HLS 200-10] Validating synthesis directives ...

INFO: [HLS 200-111] Finished Checking Pragmas Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 352.020 ; gain = 12.590 ; free physical = 686 ; free virtual = 5518

INFO: [HLS 200-111] Finished Linking Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 352.020 ; gain = 12.590 ; free physical = 685 ; free virtual = 5518

INFO: [HLS 200-10] Starting code transformations ...

INFO: [HLS 200-111] Finished Standard Transforms Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 352.020 ; gain = 12.590 ; free physical = 685 ; free virtual = 5518

INFO: [HLS 200-10] Checking synthesizability ...

INFO: [HLS 200-111] Finished Checking Synthesizability Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 352.020 ; gain = 12.590 ; free physical = 685 ; free virtual = 5518

INFO: [XFORM 203-502] Unrolling all sub-loops inside loop 'Col' (../../../../../../home/drsatya/Desktop/lab1/mat\_pipline\_3.cpp:14) in function 'matrixmul' for pipelining.

INFO: [XFORM 203-501] Unrolling loop 'Product' (../../../../../../home/drsatya/Desktop/lab1/mat\_pipline\_3.cpp:18) in function 'matrixmul' completely.

INFO: [XFORM 203-101] Partitioning array 'a' (../../../../../../home/drsatya/Desktop/lab1/mat\_pipline\_3.cpp:5) in dimension 2 completely.

INFO: [XFORM 203-101] Partitioning array 'b' (../../../../../../home/drsatya/Desktop/lab1/mat\_pipline\_3.cpp:6) in dimension 2 completely.

INFO: [HLS 200-111] Finished Pre-synthesis Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 480.016 ; gain = 140.586 ; free physical = 665 ; free virtual = 5498

INFO: [XFORM 203-541] Flattening a loop nest 'Row' (../../../../../../home/drsatya/Desktop/lab1/mat\_pipline\_3.cpp:11:36) in function 'matrixmul'.

INFO: [HLS 200-111] Finished Architecture Synthesis Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 480.016 ; gain = 140.586 ; free physical = 674 ; free virtual = 5507

INFO: [HLS 200-10] Starting hardware synthesis ...

INFO: [HLS 200-10] Synthesizing 'matrixmul' ...

INFO: [HLS 200-10] ----------------------------------------------------------------

INFO: [HLS 200-10] -- Implementing module 'matrixmul'

INFO: [HLS 200-10] ----------------------------------------------------------------

INFO: [SCHED 204-11] Starting scheduling ...

INFO: [SCHED 204-61] Pipelining loop 'Row\_Col'.

WARNING: [SCHED 204-69] Unable to schedule 'load' operation ('b\_0\_load\_1') on array 'b\_0' due to limited memory ports.

INFO: [SCHED 204-61] Pipelining result: Target II: 1, Final II: 2, Depth: 4.

INFO: [SCHED 204-11] Finished scheduling.

INFO: [HLS 200-111] Elapsed time: 2.45 seconds; current allocated memory: 0.318 MB.

INFO: [BIND 205-100] Starting micro-architecture generation ...

INFO: [BIND 205-101] Performing variable lifetime analysis.

INFO: [BIND 205-101] Exploring resource sharing.

INFO: [BIND 205-101] Binding ...

INFO: [BIND 205-100] Finished micro-architecture generation.

INFO: [HLS 200-111] Elapsed time: 0.02 seconds; current allocated memory: 0.318 MB.

INFO: [HLS 200-10] ----------------------------------------------------------------

INFO: [HLS 200-10] -- Generating RTL for module 'matrixmul'

INFO: [HLS 200-10] ----------------------------------------------------------------

INFO: [RTGEN 206-500] Setting interface mode on port 'matrixmul/a\_0' to 'ap\_memory'.

INFO: [RTGEN 206-500] Setting interface mode on port 'matrixmul/a\_1' to 'ap\_memory'.

INFO: [RTGEN 206-500] Setting interface mode on port 'matrixmul/a\_2' to 'ap\_memory'.

INFO: [RTGEN 206-500] Setting interface mode on port 'matrixmul/b\_0' to 'ap\_memory'.

INFO: [RTGEN 206-500] Setting interface mode on port 'matrixmul/b\_1' to 'ap\_memory'.

INFO: [RTGEN 206-500] Setting interface mode on port 'matrixmul/b\_2' to 'ap\_memory'.

INFO: [RTGEN 206-500] Setting interface mode on port 'matrixmul/res' to 'ap\_memory'.

INFO: [RTGEN 206-500] Setting interface mode on function 'matrixmul' to 'ap\_ctrl\_hs'.

INFO: [SYN 201-210] Renamed object name 'matrixmul\_mux\_32\_8\_1' to 'matrixmul\_mux\_32\_bkb' due to the length limit 20

INFO: [SYN 201-210] Renamed object name 'matrixmul\_mac\_muladd\_8s\_8s\_16ns\_16\_1' to 'matrixmul\_mac\_mulcud' due to the length limit 20

INFO: [SYN 201-210] Renamed object name 'matrixmul\_mac\_muladd\_8s\_8s\_16s\_16\_1' to 'matrixmul\_mac\_muldEe' due to the length limit 20

INFO: [RTGEN 206-100] Generating core module 'matrixmul\_mac\_mulcud': 1 instance(s).

INFO: [RTGEN 206-100] Generating core module 'matrixmul\_mac\_muldEe': 1 instance(s).

INFO: [RTGEN 206-100] Generating core module 'matrixmul\_mux\_32\_bkb': 2 instance(s).

INFO: [RTGEN 206-100] Finished creating RTL model for 'matrixmul'.

INFO: [HLS 200-111] Elapsed time: 0.05 seconds; current allocated memory: 0.318 MB.

INFO: [HLS 200-111] Finished generating all RTL models Time (s): cpu = 00:00:04 ; elapsed = 00:00:03 . Memory (MB): peak = 480.020 ; gain = 140.590 ; free physical = 667 ; free virtual = 5501

INFO: [SYSC 207-301] Generating SystemC RTL for matrixmul.

INFO: [VHDL 208-304] Generating VHDL RTL for matrixmul.

INFO: [VLOG 209-307] Generating Verilog RTL for matrixmul.

INFO: [HLS 200-112] Total elapsed time: 2.83 seconds; peak allocated memory: 0.318 MB.