// ==============================================================

// RTL generated by Vivado(TM) HLS - High-Level Synthesis from C, C++ and SystemC

// Version: 2017.2

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// ===========================================================

#ifndef \_matrixmul\_HH\_

#define \_matrixmul\_HH\_

#include "systemc.h"

#include "AESL\_pkg.h"

#include "matrixmul\_mux\_32\_bkb.h"

#include "matrixmul\_mac\_mulcud.h"

#include "matrixmul\_mac\_muldEe.h"

namespace ap\_rtl {

struct matrixmul : public sc\_module {

// Port declarations 37

sc\_in\_clk ap\_clk;

sc\_in< sc\_logic > ap\_rst;

sc\_in< sc\_logic > ap\_start;

sc\_out< sc\_logic > ap\_done;

sc\_out< sc\_logic > ap\_idle;

sc\_out< sc\_logic > ap\_ready;

sc\_out< sc\_lv<2> > a\_0\_address0;

sc\_out< sc\_logic > a\_0\_ce0;

sc\_in< sc\_lv<8> > a\_0\_q0;

sc\_out< sc\_lv<2> > a\_1\_address0;

sc\_out< sc\_logic > a\_1\_ce0;

sc\_in< sc\_lv<8> > a\_1\_q0;

sc\_out< sc\_lv<2> > a\_2\_address0;

sc\_out< sc\_logic > a\_2\_ce0;

sc\_in< sc\_lv<8> > a\_2\_q0;

sc\_out< sc\_lv<2> > b\_0\_address0;

sc\_out< sc\_logic > b\_0\_ce0;

sc\_in< sc\_lv<8> > b\_0\_q0;

sc\_out< sc\_lv<2> > b\_0\_address1;

sc\_out< sc\_logic > b\_0\_ce1;

sc\_in< sc\_lv<8> > b\_0\_q1;

sc\_out< sc\_lv<2> > b\_1\_address0;

sc\_out< sc\_logic > b\_1\_ce0;

sc\_in< sc\_lv<8> > b\_1\_q0;

sc\_out< sc\_lv<2> > b\_1\_address1;

sc\_out< sc\_logic > b\_1\_ce1;

sc\_in< sc\_lv<8> > b\_1\_q1;

sc\_out< sc\_lv<2> > b\_2\_address0;

sc\_out< sc\_logic > b\_2\_ce0;

sc\_in< sc\_lv<8> > b\_2\_q0;

sc\_out< sc\_lv<2> > b\_2\_address1;

sc\_out< sc\_logic > b\_2\_ce1;

sc\_in< sc\_lv<8> > b\_2\_q1;

sc\_out< sc\_lv<4> > res\_address0;

sc\_out< sc\_logic > res\_ce0;

sc\_out< sc\_logic > res\_we0;

sc\_out< sc\_lv<16> > res\_d0;

// Module declarations

matrixmul(sc\_module\_name name);

SC\_HAS\_PROCESS(matrixmul);

~matrixmul();

sc\_trace\_file\* mVcdFile;

ofstream mHdltvinHandle;

ofstream mHdltvoutHandle;

matrixmul\_mux\_32\_bkb<1,1,8,8,8,2,8>\* matrixmul\_mux\_32\_bkb\_U1;

matrixmul\_mux\_32\_bkb<1,1,8,8,8,2,8>\* matrixmul\_mux\_32\_bkb\_U2;

matrixmul\_mac\_mulcud<1,1,8,8,16,16>\* matrixmul\_mac\_mulcud\_U3;

matrixmul\_mac\_muldEe<1,1,8,8,16,16>\* matrixmul\_mac\_muldEe\_U4;

sc\_signal< sc\_lv<4> > ap\_CS\_fsm;

sc\_signal< sc\_logic > ap\_CS\_fsm\_state1;

sc\_signal< sc\_lv<4> > indvar\_flatten\_reg\_205;

sc\_signal< sc\_lv<2> > i\_reg\_216;

sc\_signal< sc\_lv<2> > j\_reg\_227;

sc\_signal< sc\_lv<8> > grp\_fu\_238\_p5;

sc\_signal< sc\_lv<8> > reg\_249;

sc\_signal< sc\_logic > ap\_CS\_fsm\_pp0\_stage1;

sc\_signal< sc\_logic > ap\_enable\_reg\_pp0\_iter0;

sc\_signal< bool > ap\_block\_state3\_pp0\_stage1\_iter0;

sc\_signal< bool > ap\_block\_state5\_pp0\_stage1\_iter1;

sc\_signal< bool > ap\_block\_pp0\_stage1\_flag00011001;

sc\_signal< sc\_lv<1> > exitcond\_flatten\_reg\_437;

sc\_signal< sc\_logic > ap\_CS\_fsm\_pp0\_stage0;

sc\_signal< sc\_logic > ap\_enable\_reg\_pp0\_iter1;

sc\_signal< bool > ap\_block\_state2\_pp0\_stage0\_iter0;

sc\_signal< bool > ap\_block\_state4\_pp0\_stage0\_iter1;

sc\_signal< bool > ap\_block\_pp0\_stage0\_flag00011001;

sc\_signal< sc\_lv<1> > exitcond\_flatten\_fu\_253\_p2;

sc\_signal< sc\_lv<1> > ap\_reg\_pp0\_iter1\_exitcond\_flatten\_reg\_437;

sc\_signal< sc\_lv<4> > indvar\_flatten\_next\_fu\_259\_p2;

sc\_signal< sc\_lv<4> > indvar\_flatten\_next\_reg\_441;

sc\_signal< sc\_lv<2> > j\_mid2\_fu\_277\_p3;

sc\_signal< sc\_lv<2> > j\_mid2\_reg\_446;

sc\_signal< sc\_lv<2> > ap\_reg\_pp0\_iter1\_j\_mid2\_reg\_446;

sc\_signal< sc\_lv<2> > tmp\_mid2\_v\_fu\_285\_p3;

sc\_signal< sc\_lv<2> > tmp\_mid2\_v\_reg\_454;

sc\_signal< sc\_lv<2> > ap\_reg\_pp0\_iter1\_tmp\_mid2\_v\_reg\_454;

sc\_signal< sc\_lv<8> > a\_0\_load\_reg\_476;

sc\_signal< sc\_lv<8> > a\_1\_load\_reg\_481;

sc\_signal< sc\_lv<8> > a\_2\_load\_reg\_486;

sc\_signal< sc\_lv<8> > tmp\_9\_fu\_300\_p5;

sc\_signal< sc\_lv<8> > tmp\_9\_reg\_491;

sc\_signal< sc\_lv<2> > j\_1\_fu\_311\_p2;

sc\_signal< sc\_lv<2> > j\_1\_reg\_496;

sc\_signal< sc\_lv<16> > grp\_fu\_376\_p3;

sc\_signal< sc\_lv<16> > tmp1\_reg\_501;

sc\_signal< bool > ap\_block\_pp0\_stage0\_flag00011011;

sc\_signal< sc\_logic > ap\_condition\_pp0\_exit\_iter0\_state2;

sc\_signal< bool > ap\_block\_pp0\_stage1\_flag00011011;

sc\_signal< sc\_lv<4> > indvar\_flatten\_phi\_fu\_209\_p4;

sc\_signal< bool > ap\_block\_pp0\_stage0\_flag00000000;

sc\_signal< sc\_lv<2> > i\_phi\_fu\_220\_p4;

sc\_signal< sc\_lv<2> > j\_phi\_fu\_231\_p4;

sc\_signal< sc\_lv<64> > tmp\_mid2\_fu\_293\_p1;

sc\_signal< sc\_lv<64> > tmp\_10\_cast\_fu\_364\_p1;

sc\_signal< bool > ap\_block\_pp0\_stage1\_flag00000000;

sc\_signal< sc\_lv<16> > grp\_fu\_384\_p3;

sc\_signal< sc\_lv<1> > exitcond\_fu\_271\_p2;

sc\_signal< sc\_lv<2> > i\_1\_fu\_265\_p2;

sc\_signal< sc\_lv<8> > tmp\_7\_2\_fu\_329\_p0;

sc\_signal< sc\_lv<8> > tmp\_7\_2\_fu\_329\_p1;

sc\_signal< sc\_lv<4> > tmp\_fu\_338\_p3;

sc\_signal< sc\_lv<5> > p\_shl\_cast\_fu\_345\_p1;

sc\_signal< sc\_lv<5> > tmp\_mid2\_cast\_fu\_335\_p1;

sc\_signal< sc\_lv<5> > tmp\_1\_fu\_349\_p2;

sc\_signal< sc\_lv<5> > tmp\_2\_cast\_fu\_355\_p1;

sc\_signal< sc\_lv<5> > tmp\_s\_fu\_358\_p2;

sc\_signal< sc\_lv<16> > grp\_fu\_376\_p2;

sc\_signal< sc\_logic > ap\_CS\_fsm\_state6;

sc\_signal< sc\_lv<4> > ap\_NS\_fsm;

sc\_signal< sc\_logic > ap\_idle\_pp0;

sc\_signal< sc\_logic > ap\_enable\_pp0;

static const sc\_logic ap\_const\_logic\_1;

static const sc\_logic ap\_const\_logic\_0;

static const sc\_lv<4> ap\_ST\_fsm\_state1;

static const sc\_lv<4> ap\_ST\_fsm\_pp0\_stage0;

static const sc\_lv<4> ap\_ST\_fsm\_pp0\_stage1;

static const sc\_lv<4> ap\_ST\_fsm\_state6;

static const sc\_lv<32> ap\_const\_lv32\_0;

static const bool ap\_const\_boolean\_1;

static const sc\_lv<32> ap\_const\_lv32\_2;

static const bool ap\_const\_boolean\_0;

static const sc\_lv<1> ap\_const\_lv1\_0;

static const sc\_lv<32> ap\_const\_lv32\_1;

static const sc\_lv<1> ap\_const\_lv1\_1;

static const sc\_lv<4> ap\_const\_lv4\_0;

static const sc\_lv<2> ap\_const\_lv2\_0;

static const sc\_lv<64> ap\_const\_lv64\_0;

static const sc\_lv<64> ap\_const\_lv64\_1;

static const sc\_lv<64> ap\_const\_lv64\_2;

static const sc\_lv<4> ap\_const\_lv4\_9;

static const sc\_lv<4> ap\_const\_lv4\_1;

static const sc\_lv<2> ap\_const\_lv2\_1;

static const sc\_lv<2> ap\_const\_lv2\_3;

static const sc\_lv<32> ap\_const\_lv32\_3;

// Thread declarations

void thread\_ap\_clk\_no\_reset\_();

void thread\_a\_0\_address0();

void thread\_a\_0\_ce0();

void thread\_a\_1\_address0();

void thread\_a\_1\_ce0();

void thread\_a\_2\_address0();

void thread\_a\_2\_ce0();

void thread\_ap\_CS\_fsm\_pp0\_stage0();

void thread\_ap\_CS\_fsm\_pp0\_stage1();

void thread\_ap\_CS\_fsm\_state1();

void thread\_ap\_CS\_fsm\_state6();

void thread\_ap\_block\_pp0\_stage0\_flag00000000();

void thread\_ap\_block\_pp0\_stage0\_flag00011001();

void thread\_ap\_block\_pp0\_stage0\_flag00011011();

void thread\_ap\_block\_pp0\_stage1\_flag00000000();

void thread\_ap\_block\_pp0\_stage1\_flag00011001();

void thread\_ap\_block\_pp0\_stage1\_flag00011011();

void thread\_ap\_block\_state2\_pp0\_stage0\_iter0();

void thread\_ap\_block\_state3\_pp0\_stage1\_iter0();

void thread\_ap\_block\_state4\_pp0\_stage0\_iter1();

void thread\_ap\_block\_state5\_pp0\_stage1\_iter1();

void thread\_ap\_condition\_pp0\_exit\_iter0\_state2();

void thread\_ap\_done();

void thread\_ap\_enable\_pp0();

void thread\_ap\_idle();

void thread\_ap\_idle\_pp0();

void thread\_ap\_ready();

void thread\_b\_0\_address0();

void thread\_b\_0\_address1();

void thread\_b\_0\_ce0();

void thread\_b\_0\_ce1();

void thread\_b\_1\_address0();

void thread\_b\_1\_address1();

void thread\_b\_1\_ce0();

void thread\_b\_1\_ce1();

void thread\_b\_2\_address0();

void thread\_b\_2\_address1();

void thread\_b\_2\_ce0();

void thread\_b\_2\_ce1();

void thread\_exitcond\_flatten\_fu\_253\_p2();

void thread\_exitcond\_fu\_271\_p2();

void thread\_grp\_fu\_376\_p2();

void thread\_i\_1\_fu\_265\_p2();

void thread\_i\_phi\_fu\_220\_p4();

void thread\_indvar\_flatten\_next\_fu\_259\_p2();

void thread\_indvar\_flatten\_phi\_fu\_209\_p4();

void thread\_j\_1\_fu\_311\_p2();

void thread\_j\_mid2\_fu\_277\_p3();

void thread\_j\_phi\_fu\_231\_p4();

void thread\_p\_shl\_cast\_fu\_345\_p1();

void thread\_res\_address0();

void thread\_res\_ce0();

void thread\_res\_d0();

void thread\_res\_we0();

void thread\_tmp\_10\_cast\_fu\_364\_p1();

void thread\_tmp\_1\_fu\_349\_p2();

void thread\_tmp\_2\_cast\_fu\_355\_p1();

void thread\_tmp\_7\_2\_fu\_329\_p0();

void thread\_tmp\_7\_2\_fu\_329\_p1();

void thread\_tmp\_fu\_338\_p3();

void thread\_tmp\_mid2\_cast\_fu\_335\_p1();

void thread\_tmp\_mid2\_fu\_293\_p1();

void thread\_tmp\_mid2\_v\_fu\_285\_p3();

void thread\_tmp\_s\_fu\_358\_p2();

void thread\_ap\_NS\_fsm();

void thread\_hdltv\_gen();

};

}

using namespace ap\_rtl;

#endif