\*\*\* Running vivado

with args -log design\_1.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source design\_1.tcl -notrace

\*\*\*\*\*\* Vivado v2017.2 (64-bit)

\*\*\*\* SW Build 1909853 on Thu Jun 15 18:39:10 MDT 2017

\*\*\*\* IP Build 1909766 on Thu Jun 15 19:58:00 MDT 2017

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source design\_1.tcl -notrace

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1700] Loaded user IP repository '/opt/Xilinx/Vivado\_HLS/2017.2/bin/sequence\_floating\_8\_march'.

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/opt/Xilinx/Vivado/2017.2/data/ip'.

Design is defaulting to srcset: sources\_1

Design is defaulting to constrset: constrs\_1

INFO: [Project 1-454] Reading design checkpoint '/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/design\_1/ip/design\_1\_fifo\_generator\_0\_0/design\_1\_fifo\_generator\_0\_0.dcp' for cell 'fifo\_generator\_0'

INFO: [Project 1-454] Reading design checkpoint '/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/design\_1/ip/design\_1\_fifo\_generator\_0\_1/design\_1\_fifo\_generator\_0\_1.dcp' for cell 'fifo\_generator\_1'

INFO: [Project 1-454] Reading design checkpoint '/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/design\_1/ip/design\_1\_simple\_0\_0/design\_1\_simple\_0\_0.dcp' for cell 'simple\_0'

INFO: [Netlist 29-17] Analyzing 108 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2017.2

INFO: [Device 21-403] Loading part xc7a35tcpg236-2

INFO: [Project 1-570] Preparing netlist for logic optimization

Parsing XDC File [/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/design\_1/ip/design\_1\_fifo\_generator\_0\_0/design\_1\_fifo\_generator\_0\_0.xdc] for cell 'fifo\_generator\_0/U0'

Finished Parsing XDC File [/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/design\_1/ip/design\_1\_fifo\_generator\_0\_0/design\_1\_fifo\_generator\_0\_0.xdc] for cell 'fifo\_generator\_0/U0'

Parsing XDC File [/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/design\_1/ip/design\_1\_fifo\_generator\_0\_1/design\_1\_fifo\_generator\_0\_1.xdc] for cell 'fifo\_generator\_1/U0'

Finished Parsing XDC File [/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/design\_1/ip/design\_1\_fifo\_generator\_0\_1/design\_1\_fifo\_generator\_0\_1.xdc] for cell 'fifo\_generator\_1/U0'

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

link\_design: Time (s): cpu = 00:00:05 ; elapsed = 00:00:05 . Memory (MB): peak = 1400.039 ; gain = 309.102 ; free physical = 592 ; free virtual = 5310

INFO: [Vivado\_Tcl 4-424] Cannot write hardware definition file as there are no IPI block design hardware handoff files present

Command: opt\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a35t-cpg236'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35t-cpg236'

Running DRC as a precondition to command opt\_design

Starting DRC Task

Command: report\_drc (run\_mandatory\_drcs) for: opt\_checks

INFO: [DRC 23-27] Running DRC with 4 threads

report\_drc (run\_mandatory\_drcs) completed successfully

INFO: [Project 1-461] DRC finished with 0 Errors

INFO: [Project 1-462] Please refer to the DRC report (report\_drc) for more information.

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.66 . Memory (MB): peak = 1447.047 ; gain = 47.008 ; free physical = 585 ; free virtual = 5304

INFO: [Timing 38-35] Done setting XDC timing constraints.

Starting Logic Optimization Task

Phase 1 Retarget

INFO: [Opt 31-138] Pushed 1 inverter(s) to 17 load pin(s).

INFO: [Opt 31-49] Retargeted 0 cell(s).

Phase 1 Retarget | Checksum: 1995e0cb

Time (s): cpu = 00:00:00.08 ; elapsed = 00:00:00.11 . Memory (MB): peak = 1831.477 ; gain = 0.000 ; free physical = 217 ; free virtual = 4929

INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 1 cells

Phase 2 Constant propagation

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Phase 2 Constant propagation | Checksum: edae84b6

Time (s): cpu = 00:00:00.13 ; elapsed = 00:00:00.22 . Memory (MB): peak = 1831.477 ; gain = 0.000 ; free physical = 216 ; free virtual = 4929

INFO: [Opt 31-389] Phase Constant propagation created 24 cells and removed 26 cells

Phase 3 Sweep

Phase 3 Sweep | Checksum: 8652ef53

Time (s): cpu = 00:00:00.19 ; elapsed = 00:00:00.28 . Memory (MB): peak = 1831.477 ; gain = 0.000 ; free physical = 216 ; free virtual = 4929

INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 9 cells

Phase 4 BUFG optimization

INFO: [Opt 31-194] Inserted BUFG ap\_clk\_IBUF\_BUFG\_inst to drive 282 load(s) on clock net ap\_clk\_IBUF\_BUFG

INFO: [Opt 31-193] Inserted 1 BUFG(s) on clock nets

Phase 4 BUFG optimization | Checksum: 57adc148

Time (s): cpu = 00:00:00.25 ; elapsed = 00:00:00.36 . Memory (MB): peak = 1831.477 ; gain = 0.000 ; free physical = 215 ; free virtual = 4929

INFO: [Opt 31-389] Phase BUFG optimization created 1 cells and removed 0 cells

Phase 5 Shift Register Optimization

Phase 5 Shift Register Optimization | Checksum: 57adc148

Time (s): cpu = 00:00:00.26 ; elapsed = 00:00:00.36 . Memory (MB): peak = 1831.477 ; gain = 0.000 ; free physical = 215 ; free virtual = 4929

INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1831.477 ; gain = 0.000 ; free physical = 215 ; free virtual = 4929

Ending Logic Optimization Task | Checksum: 57adc148

Time (s): cpu = 00:00:00.26 ; elapsed = 00:00:00.37 . Memory (MB): peak = 1831.477 ; gain = 0.000 ; free physical = 215 ; free virtual = 4929

Starting Power Optimization Task

INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.

INFO: [Pwropt 34-9] Applying IDT optimizations ...

INFO: [Pwropt 34-10] Applying ODC optimizations ...

INFO: [Timing 38-35] Done setting XDC timing constraints.

WARNING: [Power 33-232] No user defined clocks were found in the design!

Resolution: Please specify clocks using create\_clock/create\_generated\_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate

Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation

Starting PowerOpt Patch Enables Task

INFO: [Pwropt 34-162] WRITE\_MODE attribute of 2 BRAM(s) out of a total of 2 has been updated to save power. Run report\_power\_opt to get a complete listing of the BRAMs updated.

INFO: [Pwropt 34-201] Structural ODC has moved 0 WE to EN ports

Number of BRAM Ports augmented: 0 newly gated: 0 Total Ports: 4

Ending PowerOpt Patch Enables Task | Checksum: 141479a19

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 183 ; free virtual = 4907

Ending Power Optimization Task | Checksum: 141479a19

Time (s): cpu = 00:00:01 ; elapsed = 00:00:02 . Memory (MB): peak = 1990.578 ; gain = 159.102 ; free physical = 188 ; free virtual = 4911

35 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

opt\_design completed successfully

opt\_design: Time (s): cpu = 00:00:11 ; elapsed = 00:00:11 . Memory (MB): peak = 1990.578 ; gain = 590.539 ; free physical = 188 ; free virtual = 4911

INFO: [Common 17-1381] The checkpoint '/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/project\_1\_sequence\_8\_march\_float\_1.runs/impl\_1/design\_1\_opt.dcp' has been generated.

Command: report\_drc -file design\_1\_drc\_opted.rpt

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Coretcl 2-168] The results of DRC are in file /opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/project\_1\_sequence\_8\_march\_float\_1.runs/impl\_1/design\_1\_drc\_opted.rpt.

report\_drc completed successfully

INFO: [Chipscope 16-241] No debug cores found in the current design.

Before running the implement\_debug\_core command, either use the Set Up Debug wizard (GUI mode)

or use the create\_debug\_core and connect\_debug\_core Tcl commands to insert debug cores into the design.

Command: place\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a35t-cpg236'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35t-cpg236'

Command: report\_drc (run\_mandatory\_drcs) for: incr\_eco\_checks

INFO: [DRC 23-27] Running DRC with 4 threads

report\_drc (run\_mandatory\_drcs) completed successfully

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Running DRC as a precondition to command place\_design

Command: report\_drc (run\_mandatory\_drcs) for: placer\_checks

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [DRC REQP-1725] DSP\_Abus\_sign\_bit\_alert: simple\_0/U0/simple\_fadd\_32ns\_bkb\_U1/simple\_ap\_fadd\_3\_full\_dsp\_32\_u/U0/i\_synth/ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.ALIGN\_ADD/DSP2/DSP: When using the PreAdder and USE\_DPORT is TRUE, the A operand should be restricted to 24 bit two's complement (and sign extended) to avoid over/underflow in the pre-add stage.

report\_drc (run\_mandatory\_drcs) completed successfully

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors, 1 Advisories

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Placer Task

INFO: [Place 30-611] Multithreading enabled for place\_design using a maximum of 4 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting

Netlist sorting complete. Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 178 ; free virtual = 4902

Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 767e1a39

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.05 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 178 ; free virtual = 4902

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 178 ; free virtual = 4902

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device

INFO: [Timing 38-35] Done setting XDC timing constraints.

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: be2a2bd8

Time (s): cpu = 00:00:02 ; elapsed = 00:00:01 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 166 ; free virtual = 4897

Phase 1.3 Build Placer Netlist Model

Phase 1.3 Build Placer Netlist Model | Checksum: 181637f2c

Time (s): cpu = 00:00:02 ; elapsed = 00:00:02 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 164 ; free virtual = 4897

Phase 1.4 Constrain Clocks/Macros

Phase 1.4 Constrain Clocks/Macros | Checksum: 181637f2c

Time (s): cpu = 00:00:02 ; elapsed = 00:00:02 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 164 ; free virtual = 4897

Phase 1 Placer Initialization | Checksum: 181637f2c

Time (s): cpu = 00:00:02 ; elapsed = 00:00:02 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 163 ; free virtual = 4897

Phase 2 Global Placement

WARNING: [Place 46-30] place\_design is not in timing mode. Skip physical synthesis in placer

Phase 2 Global Placement | Checksum: 19d9c23fa

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 161 ; free virtual = 4896

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros

Phase 3.1 Commit Multi Column Macros | Checksum: 19d9c23fa

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 161 ; free virtual = 4896

Phase 3.2 Commit Most Macros & LUTRAMs

Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: ea9d378c

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 161 ; free virtual = 4896

Phase 3.3 Area Swap Optimization

Phase 3.3 Area Swap Optimization | Checksum: 11ba59ecb

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 161 ; free virtual = 4896

Phase 3.4 Pipeline Register Optimization

Phase 3.4 Pipeline Register Optimization | Checksum: 11ba59ecb

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 161 ; free virtual = 4896

Phase 3.5 Small Shape Detail Placement

Phase 3.5 Small Shape Detail Placement | Checksum: 109e12c00

Time (s): cpu = 00:00:03 ; elapsed = 00:00:03 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 159 ; free virtual = 4895

Phase 3.6 Re-assign LUT pins

Phase 3.6 Re-assign LUT pins | Checksum: 109e12c00

Time (s): cpu = 00:00:03 ; elapsed = 00:00:03 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 159 ; free virtual = 4895

Phase 3.7 Pipeline Register Optimization

Phase 3.7 Pipeline Register Optimization | Checksum: 109e12c00

Time (s): cpu = 00:00:03 ; elapsed = 00:00:03 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 159 ; free virtual = 4895

Phase 3 Detail Placement | Checksum: 109e12c00

Time (s): cpu = 00:00:03 ; elapsed = 00:00:03 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 159 ; free virtual = 4895

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization

Phase 4.1 Post Commit Optimization | Checksum: 109e12c00

Time (s): cpu = 00:00:03 ; elapsed = 00:00:03 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 159 ; free virtual = 4895

Phase 4.2 Post Placement Cleanup

Phase 4.2 Post Placement Cleanup | Checksum: 109e12c00

Time (s): cpu = 00:00:03 ; elapsed = 00:00:03 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 159 ; free virtual = 4896

Phase 4.3 Placer Reporting

Phase 4.3 Placer Reporting | Checksum: 109e12c00

Time (s): cpu = 00:00:03 ; elapsed = 00:00:03 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 159 ; free virtual = 4896

Phase 4.4 Final Placement Cleanup

Phase 4.4 Final Placement Cleanup | Checksum: 12c42adf7

Time (s): cpu = 00:00:03 ; elapsed = 00:00:03 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 159 ; free virtual = 4896

Phase 4 Post Placement Optimization and Clean-Up | Checksum: 12c42adf7

Time (s): cpu = 00:00:03 ; elapsed = 00:00:03 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 159 ; free virtual = 4896

Ending Placer Task | Checksum: 1141423c4

Time (s): cpu = 00:00:03 ; elapsed = 00:00:03 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 165 ; free virtual = 4902

51 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.

place\_design completed successfully

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.18 ; elapsed = 00:00:00.07 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 163 ; free virtual = 4902

INFO: [Common 17-1381] The checkpoint '/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/project\_1\_sequence\_8\_march\_float\_1.runs/impl\_1/design\_1\_placed.dcp' has been generated.

report\_io: Time (s): cpu = 00:00:00.16 ; elapsed = 00:00:00.20 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 160 ; free virtual = 4898

report\_utilization: Time (s): cpu = 00:00:00.10 ; elapsed = 00:00:00.14 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 164 ; free virtual = 4902

report\_control\_sets: Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.12 . Memory (MB): peak = 1990.578 ; gain = 0.000 ; free physical = 164 ; free virtual = 4902

Command: route\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a35t-cpg236'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35t-cpg236'

Running DRC as a precondition to command route\_design

Command: report\_drc (run\_mandatory\_drcs) for: router\_checks

INFO: [DRC 23-27] Running DRC with 4 threads

report\_drc (run\_mandatory\_drcs) completed successfully

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Routing Task

INFO: [Route 35-254] Multithreading enabled for route\_design using a maximum of 4 CPUs

Checksum: PlaceDB: 905980a1 ConstDB: 0 ShapeSum: 83baa323 RouteDB: 0

Phase 1 Build RT Design

Phase 1 Build RT Design | Checksum: d922f95e

Time (s): cpu = 00:00:15 ; elapsed = 00:00:13 . Memory (MB): peak = 1999.238 ; gain = 8.660 ; free physical = 139 ; free virtual = 4768

Phase 2 Router Initialization

INFO: [Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.

Phase 2.1 Fix Topology Constraints

Phase 2.1 Fix Topology Constraints | Checksum: d922f95e

Time (s): cpu = 00:00:15 ; elapsed = 00:00:13 . Memory (MB): peak = 2014.238 ; gain = 23.660 ; free physical = 121 ; free virtual = 4753

Phase 2.2 Pre Route Cleanup

Phase 2.2 Pre Route Cleanup | Checksum: d922f95e

Time (s): cpu = 00:00:15 ; elapsed = 00:00:13 . Memory (MB): peak = 2014.238 ; gain = 23.660 ; free physical = 121 ; free virtual = 4753

Number of Nodes with overlaps = 0

Phase 2 Router Initialization | Checksum: 149f71489

Time (s): cpu = 00:00:15 ; elapsed = 00:00:13 . Memory (MB): peak = 2031.238 ; gain = 40.660 ; free physical = 109 ; free virtual = 4741

Phase 3 Initial Routing

Phase 3 Initial Routing | Checksum: 107b8460a

Time (s): cpu = 00:00:15 ; elapsed = 00:00:13 . Memory (MB): peak = 2031.238 ; gain = 40.660 ; free physical = 114 ; free virtual = 4747

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0

Number of Nodes with overlaps = 31

Number of Nodes with overlaps = 0

Phase 4.1 Global Iteration 0 | Checksum: 10bdad5bd

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2031.238 ; gain = 40.660 ; free physical = 114 ; free virtual = 4747

Phase 4 Rip-up And Reroute | Checksum: 10bdad5bd

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2031.238 ; gain = 40.660 ; free physical = 114 ; free virtual = 4747

Phase 5 Delay and Skew Optimization

Phase 5 Delay and Skew Optimization | Checksum: 10bdad5bd

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2031.238 ; gain = 40.660 ; free physical = 114 ; free virtual = 4747

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter

Phase 6.1 Hold Fix Iter | Checksum: 10bdad5bd

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2031.238 ; gain = 40.660 ; free physical = 114 ; free virtual = 4747

Phase 6 Post Hold Fix | Checksum: 10bdad5bd

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2031.238 ; gain = 40.660 ; free physical = 114 ; free virtual = 4747

Phase 7 Route finalize

Router Utilization Summary

Global Vertical Routing Utilization = 0.38085 %

Global Horizontal Routing Utilization = 0.376236 %

Routable Net Status\*

\*Does not include unroutable nets such as driverless and loadless.

Run report\_route\_status for detailed report.

Number of Failed Nets = 0

Number of Unrouted Nets = 0

Number of Partially Routed Nets = 0

Number of Node Overlaps = 0

Congestion Report

North Dir 1x1 Area, Max Cong = 34.2342%, No Congested Regions.

South Dir 1x1 Area, Max Cong = 43.2432%, No Congested Regions.

East Dir 1x1 Area, Max Cong = 33.8235%, No Congested Regions.

West Dir 1x1 Area, Max Cong = 38.2353%, No Congested Regions.

Phase 7 Route finalize | Checksum: 10bdad5bd

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2031.238 ; gain = 40.660 ; free physical = 114 ; free virtual = 4747

Phase 8 Verifying routed nets

Verification completed successfully

Phase 8 Verifying routed nets | Checksum: 10bdad5bd

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2031.238 ; gain = 40.660 ; free physical = 114 ; free virtual = 4747

Phase 9 Depositing Routes

Phase 9 Depositing Routes | Checksum: 186c39212

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2031.238 ; gain = 40.660 ; free physical = 114 ; free virtual = 4747

INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2031.238 ; gain = 40.660 ; free physical = 131 ; free virtual = 4764

Routing Is Done.

59 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.

route\_design completed successfully

route\_design: Time (s): cpu = 00:00:18 ; elapsed = 00:00:14 . Memory (MB): peak = 2031.242 ; gain = 40.664 ; free physical = 130 ; free virtual = 4763

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.18 ; elapsed = 00:00:00.06 . Memory (MB): peak = 2031.242 ; gain = 0.000 ; free physical = 127 ; free virtual = 4763

INFO: [Common 17-1381] The checkpoint '/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/project\_1\_sequence\_8\_march\_float\_1.runs/impl\_1/design\_1\_routed.dcp' has been generated.

Command: report\_drc -file design\_1\_drc\_routed.rpt -pb design\_1\_drc\_routed.pb -rpx design\_1\_drc\_routed.rpx

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Coretcl 2-168] The results of DRC are in file /opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/project\_1\_sequence\_8\_march\_float\_1.runs/impl\_1/design\_1\_drc\_routed.rpt.

report\_drc completed successfully

Command: report\_methodology -file design\_1\_methodology\_drc\_routed.rpt -rpx design\_1\_methodology\_drc\_routed.rpx

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [DRC 23-133] Running Methodology with 4 threads

INFO: [Coretcl 2-1520] The results of Report Methodology are in file /opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/project\_1\_sequence\_8\_march\_float\_1.runs/impl\_1/design\_1\_methodology\_drc\_routed.rpt.

report\_methodology completed successfully

Command: report\_power -file design\_1\_power\_routed.rpt -pb design\_1\_power\_summary\_routed.pb -rpx design\_1\_power\_routed.rpx

WARNING: [Power 33-232] No user defined clocks were found in the design!

Resolution: Please specify clocks using create\_clock/create\_generated\_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate

INFO: [Timing 38-35] Done setting XDC timing constraints.

Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation

66 Infos, 3 Warnings, 0 Critical Warnings and 0 Errors encountered.

report\_power completed successfully

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -2, Delay Type: min\_max.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 4 CPUs

WARNING: [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.

INFO: [Common 17-206] Exiting Vivado at Thu Mar 8 12:44:26 2018...