\*\*\* Running vivado

with args -log design\_1.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source design\_1.tcl

\*\*\*\*\*\* Vivado v2017.2 (64-bit)

\*\*\*\* SW Build 1909853 on Thu Jun 15 18:39:10 MDT 2017

\*\*\*\* IP Build 1909766 on Thu Jun 15 19:58:00 MDT 2017

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source design\_1.tcl -notrace

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1700] Loaded user IP repository '/opt/Xilinx/Vivado\_HLS/2017.2/bin/sequence\_floating\_8\_march'.

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/opt/Xilinx/Vivado/2017.2/data/ip'.

Command: synth\_design -top design\_1 -part xc7a35tcpg236-2

Starting synth\_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a35t-cpg236'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t-cpg236'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 19568

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Starting RTL Elaboration : Time (s): cpu = 00:00:03 ; elapsed = 00:00:04 . Memory (MB): peak = 1168.520 ; gain = 64.992 ; free physical = 772 ; free virtual = 5475

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INFO: [Synth 8-638] synthesizing module 'design\_1' [/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/design\_1/hdl/design\_1.vhd:34]

INFO: [Synth 8-3491] module 'design\_1\_fifo\_generator\_0\_0' declared at '/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/project\_1\_sequence\_8\_march\_float\_1.runs/synth\_1/.Xil/Vivado-19560-drsatya-OptiPlex-990/realtime/design\_1\_fifo\_generator\_0\_0\_stub.vhdl:5' bound to instance 'fifo\_generator\_0' of component 'design\_1\_fifo\_generator\_0\_0' [/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/design\_1/hdl/design\_1.vhd:117]

INFO: [Synth 8-638] synthesizing module 'design\_1\_fifo\_generator\_0\_0' [/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/project\_1\_sequence\_8\_march\_float\_1.runs/synth\_1/.Xil/Vivado-19560-drsatya-OptiPlex-990/realtime/design\_1\_fifo\_generator\_0\_0\_stub.vhdl:19]

INFO: [Synth 8-3491] module 'design\_1\_fifo\_generator\_0\_1' declared at '/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/project\_1\_sequence\_8\_march\_float\_1.runs/synth\_1/.Xil/Vivado-19560-drsatya-OptiPlex-990/realtime/design\_1\_fifo\_generator\_0\_1\_stub.vhdl:5' bound to instance 'fifo\_generator\_1' of component 'design\_1\_fifo\_generator\_0\_1' [/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/design\_1/hdl/design\_1.vhd:128]

INFO: [Synth 8-638] synthesizing module 'design\_1\_fifo\_generator\_0\_1' [/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/project\_1\_sequence\_8\_march\_float\_1.runs/synth\_1/.Xil/Vivado-19560-drsatya-OptiPlex-990/realtime/design\_1\_fifo\_generator\_0\_1\_stub.vhdl:19]

INFO: [Synth 8-3491] module 'design\_1\_simple\_0\_0' declared at '/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/project\_1\_sequence\_8\_march\_float\_1.runs/synth\_1/.Xil/Vivado-19560-drsatya-OptiPlex-990/realtime/design\_1\_simple\_0\_0\_stub.vhdl:5' bound to instance 'simple\_0' of component 'design\_1\_simple\_0\_0' [/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/design\_1/hdl/design\_1.vhd:139]

INFO: [Synth 8-638] synthesizing module 'design\_1\_simple\_0\_0' [/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/project\_1\_sequence\_8\_march\_float\_1.runs/synth\_1/.Xil/Vivado-19560-drsatya-OptiPlex-990/realtime/design\_1\_simple\_0\_0\_stub.vhdl:28]

INFO: [Synth 8-256] done synthesizing module 'design\_1' (1#1) [/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/design\_1/hdl/design\_1.vhd:34]

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Finished RTL Elaboration : Time (s): cpu = 00:00:04 ; elapsed = 00:00:04 . Memory (MB): peak = 1210.027 ; gain = 106.500 ; free physical = 782 ; free virtual = 5485

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Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:04 ; elapsed = 00:00:04 . Memory (MB): peak = 1210.027 ; gain = 106.500 ; free physical = 782 ; free virtual = 5486

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INFO: [Device 21-403] Loading part xc7a35tcpg236-2

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/project\_1\_sequence\_8\_march\_float\_1.runs/synth\_1/.Xil/Vivado-19560-drsatya-OptiPlex-990/dcp7/design\_1\_simple\_0\_0\_in\_context.xdc] for cell 'simple\_0'

Finished Parsing XDC File [/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/project\_1\_sequence\_8\_march\_float\_1.runs/synth\_1/.Xil/Vivado-19560-drsatya-OptiPlex-990/dcp7/design\_1\_simple\_0\_0\_in\_context.xdc] for cell 'simple\_0'

Parsing XDC File [/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/project\_1\_sequence\_8\_march\_float\_1.runs/synth\_1/.Xil/Vivado-19560-drsatya-OptiPlex-990/dcp9/design\_1\_fifo\_generator\_0\_0\_in\_context.xdc] for cell 'fifo\_generator\_0'

Finished Parsing XDC File [/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/project\_1\_sequence\_8\_march\_float\_1.runs/synth\_1/.Xil/Vivado-19560-drsatya-OptiPlex-990/dcp9/design\_1\_fifo\_generator\_0\_0\_in\_context.xdc] for cell 'fifo\_generator\_0'

Parsing XDC File [/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/project\_1\_sequence\_8\_march\_float\_1.runs/synth\_1/.Xil/Vivado-19560-drsatya-OptiPlex-990/dcp11/design\_1\_fifo\_generator\_0\_1\_in\_context.xdc] for cell 'fifo\_generator\_1'

Finished Parsing XDC File [/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/project\_1\_sequence\_8\_march\_float\_1.runs/synth\_1/.Xil/Vivado-19560-drsatya-OptiPlex-990/dcp11/design\_1\_fifo\_generator\_0\_1\_in\_context.xdc] for cell 'fifo\_generator\_1'

Parsing XDC File [/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/project\_1\_sequence\_8\_march\_float\_1.runs/synth\_1/dont\_touch.xdc]

Finished Parsing XDC File [/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/project\_1\_sequence\_8\_march\_float\_1.runs/synth\_1/dont\_touch.xdc]

Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1469.035 ; gain = 0.000 ; free physical = 559 ; free virtual = 5261

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Finished Constraint Validation : Time (s): cpu = 00:00:12 ; elapsed = 00:00:12 . Memory (MB): peak = 1469.035 ; gain = 365.508 ; free physical = 606 ; free virtual = 5309

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Start Loading Part and Timing Information

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Loading part: xc7a35tcpg236-2

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Finished Loading Part and Timing Information : Time (s): cpu = 00:00:12 ; elapsed = 00:00:12 . Memory (MB): peak = 1469.035 ; gain = 365.508 ; free physical = 606 ; free virtual = 5309

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Start Applying 'set\_property' XDC Constraints

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Applied set\_property DONT\_TOUCH = true for fifo\_generator\_0. (constraint file auto generated constraint, line ).

Applied set\_property DONT\_TOUCH = true for fifo\_generator\_1. (constraint file auto generated constraint, line ).

Applied set\_property DONT\_TOUCH = true for simple\_0. (constraint file auto generated constraint, line ).

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Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:12 ; elapsed = 00:00:12 . Memory (MB): peak = 1469.035 ; gain = 365.508 ; free physical = 608 ; free virtual = 5311

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Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:12 ; elapsed = 00:00:12 . Memory (MB): peak = 1469.035 ; gain = 365.508 ; free physical = 608 ; free virtual = 5311

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

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+-+--------------+------------+----------+

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Start RTL Component Statistics

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Detailed RTL Component Info :

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Finished RTL Component Statistics

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---------------------------------------------------------------------------------

Start RTL Hierarchical Component Statistics

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Hierarchical RTL Component report

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Finished RTL Hierarchical Component Statistics

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Start Part Resource Summary

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Part Resources:

DSPs: 90 (col length:60)

BRAMs: 100 (col length: RAMB18 60 RAMB36 30)

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Finished Part Resource Summary

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Start Cross Boundary and Area Optimization

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Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:12 ; elapsed = 00:00:13 . Memory (MB): peak = 1469.035 ; gain = 365.508 ; free physical = 609 ; free virtual = 5312

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Applying XDC Timing Constraints

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Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:19 ; elapsed = 00:00:19 . Memory (MB): peak = 1499.035 ; gain = 395.508 ; free physical = 514 ; free virtual = 5208

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Start Timing Optimization

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Finished Timing Optimization : Time (s): cpu = 00:00:19 ; elapsed = 00:00:19 . Memory (MB): peak = 1499.035 ; gain = 395.508 ; free physical = 514 ; free virtual = 5208

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Technology Mapping

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Finished Technology Mapping : Time (s): cpu = 00:00:19 ; elapsed = 00:00:19 . Memory (MB): peak = 1509.047 ; gain = 405.520 ; free physical = 513 ; free virtual = 5207

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start IO Insertion

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Start Flattening Before IO Insertion

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Finished Flattening Before IO Insertion

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Start Final Netlist Cleanup

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Finished Final Netlist Cleanup

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Finished IO Insertion : Time (s): cpu = 00:00:19 ; elapsed = 00:00:19 . Memory (MB): peak = 1509.047 ; gain = 405.520 ; free physical = 513 ; free virtual = 5207

---------------------------------------------------------------------------------

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Renaming Generated Instances

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Finished Renaming Generated Instances : Time (s): cpu = 00:00:19 ; elapsed = 00:00:19 . Memory (MB): peak = 1509.047 ; gain = 405.520 ; free physical = 513 ; free virtual = 5207

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

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+-+--------------+------------+----------+

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Start Rebuilding User Hierarchy

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Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:19 ; elapsed = 00:00:19 . Memory (MB): peak = 1509.047 ; gain = 405.520 ; free physical = 513 ; free virtual = 5207

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Start Renaming Generated Ports

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Finished Renaming Generated Ports : Time (s): cpu = 00:00:19 ; elapsed = 00:00:19 . Memory (MB): peak = 1509.047 ; gain = 405.520 ; free physical = 513 ; free virtual = 5207

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:19 ; elapsed = 00:00:19 . Memory (MB): peak = 1509.047 ; gain = 405.520 ; free physical = 513 ; free virtual = 5207

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Start Renaming Generated Nets

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Finished Renaming Generated Nets : Time (s): cpu = 00:00:19 ; elapsed = 00:00:19 . Memory (MB): peak = 1509.047 ; gain = 405.520 ; free physical = 513 ; free virtual = 5207

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Start Writing Synthesis Report

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Report BlackBoxes:

+------+----------------------------+----------+

| |BlackBox name |Instances |

+------+----------------------------+----------+

|1 |design\_1\_fifo\_generator\_0\_0 | 1|

|2 |design\_1\_fifo\_generator\_0\_1 | 1|

|3 |design\_1\_simple\_0\_0 | 1|

+------+----------------------------+----------+

Report Cell Usage:

+------+---------------------------------+------+

| |Cell |Count |

+------+---------------------------------+------+

|1 |design\_1\_fifo\_generator\_0\_0\_bbox | 1|

|2 |design\_1\_fifo\_generator\_0\_1\_bbox | 1|

|3 |design\_1\_simple\_0\_0\_bbox | 1|

|4 |IBUF | 69|

|5 |OBUF | 35|

+------+---------------------------------+------+

Report Instance Areas:

+------+---------+-------+------+

| |Instance |Module |Cells |

+------+---------+-------+------+

|1 |top | | 252|

+------+---------+-------+------+

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Finished Writing Synthesis Report : Time (s): cpu = 00:00:19 ; elapsed = 00:00:20 . Memory (MB): peak = 1509.047 ; gain = 405.520 ; free physical = 513 ; free virtual = 5207

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Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:15 ; elapsed = 00:00:15 . Memory (MB): peak = 1509.047 ; gain = 146.512 ; free physical = 569 ; free virtual = 5263

Synthesis Optimization Complete : Time (s): cpu = 00:00:19 ; elapsed = 00:00:20 . Memory (MB): peak = 1509.055 ; gain = 405.520 ; free physical = 569 ; free virtual = 5263

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 69 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

21 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth\_design completed successfully

synth\_design: Time (s): cpu = 00:00:21 ; elapsed = 00:00:21 . Memory (MB): peak = 1513.047 ; gain = 422.105 ; free physical = 532 ; free virtual = 5226

INFO: [Common 17-1381] The checkpoint '/opt/Xilinx/Vivado/2017.2/bin/project\_1\_sequence\_8\_march\_float\_1/project\_1\_sequence\_8\_march\_float\_1.runs/synth\_1/design\_1.dcp' has been generated.

report\_utilization: Time (s): cpu = 00:00:00.11 ; elapsed = 00:00:00.13 . Memory (MB): peak = 1513.051 ; gain = 0.000 ; free physical = 533 ; free virtual = 5227

INFO: [Common 17-206] Exiting Vivado at Thu Mar 8 12:43:26 2018...