Vivado Simulator 2017.2

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Running: /opt/Xilinx/Vivado/2017.2/bin/unwrapped/lnx64.o/xelab -wto 40ee5ae84ec34e199ccc006b7ebe43cd --debug typical --relax --mt 8 -L xbip\_utils\_v3\_0\_7 -L axi\_utils\_v2\_0\_3 -L xbip\_pipe\_v3\_0\_3 -L xbip\_dsp48\_wrapper\_v3\_0\_4 -L xbip\_dsp48\_addsub\_v3\_0\_3 -L xbip\_dsp48\_multadd\_v3\_0\_3 -L xbip\_bram18k\_v3\_0\_3 -L mult\_gen\_v12\_0\_12 -L floating\_point\_v7\_1\_4 -L xil\_defaultlib -L secureip -L xpm --snapshot design\_1\_wrapper\_behav xil\_defaultlib.design\_1\_wrapper -log elaborate.log

Using 8 slave threads.

Starting static elaboration

Completed static elaboration

Starting simulation data flow analysis

Completed simulation data flow analysis

Time Resolution for simulation is 1ps

Compiling package std.standard

Compiling package std.textio

Compiling package ieee.std\_logic\_1164

Compiling package unisim.vcomponents

Compiling package ieee.vital\_timing

Compiling package ieee.vital\_primitives

Compiling package unisim.vpkg

Compiling package ieee.numeric\_std

Compiling package ieee.std\_logic\_arith

Compiling package ieee.std\_logic\_signed

Compiling package ieee.std\_logic\_textio

Compiling package floating\_point\_v7\_1\_4.floating\_point\_v7\_1\_4\_viv\_comp

Compiling package xbip\_utils\_v3\_0\_7.xbip\_utils\_v3\_0\_7\_pkg

Compiling package axi\_utils\_v2\_0\_3.axi\_utils\_v2\_0\_3\_pkg

Compiling package floating\_point\_v7\_1\_4.floating\_point\_v7\_1\_4\_consts

Compiling package ieee.math\_real

Compiling package floating\_point\_v7\_1\_4.floating\_point\_v7\_1\_4\_exp\_table\_...

Compiling package mult\_gen\_v12\_0\_12.mult\_gen\_v12\_0\_12\_pkg

Compiling package floating\_point\_v7\_1\_4.floating\_point\_v7\_1\_4\_pkg

Compiling package floating\_point\_v7\_1\_4.flt\_utils

Compiling package xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv\_comp

Compiling architecture gnd\_v of entity unisim.GND [gnd\_default]

Compiling architecture vcc\_v of entity unisim.VCC [vcc\_default]

Compiling architecture lut3\_v of entity unisim.LUT3 [\LUT3(init="10111010")(0,7)\]

Compiling architecture carry4\_v of entity unisim.CARRY4 [carry4\_default]

Compiling architecture lut6\_v of entity unisim.LUT6 [\LUT6(init="11111100111100001111...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_0\_compare\_1 [design\_1\_fifo\_generator\_0\_0\_comp...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_0\_compare\_2 [design\_1\_fifo\_generator\_0\_0\_comp...]

Compiling architecture lut2\_v of entity unisim.LUT2 [\LUT2(init="0010")(0,3)\]

Compiling architecture fdse\_v of entity unisim.FDSE [fdse\_default]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_0\_rd\_status\_flags\_ss [design\_1\_fifo\_generator\_0\_0\_rd\_s...]

Compiling architecture lut1\_v of entity unisim.LUT1 [\LUT1(init="0001")(0,3)\]

Compiling architecture lut2\_v of entity unisim.LUT2 [\LUT2(init="0110")(0,3)\]

Compiling architecture lut3\_v of entity unisim.LUT3 [\LUT3(init="01111000")(0,7)\]

Compiling architecture lut4\_v of entity unisim.LUT4 [\LUT4(init="0111111110000000")(0...]

Compiling architecture lut5\_v of entity unisim.LUT5 [\LUT5(init="01111111111111111000...]

Compiling architecture lut6\_v of entity unisim.LUT6 [\LUT6(init="01111111111111111111...]

Compiling architecture lut6\_v of entity unisim.LUT6 [\LUT6(init="10000000000000000000...]

Compiling architecture fdre\_v of entity unisim.FDRE [fdre\_default]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_0\_rd\_bin\_cntr [design\_1\_fifo\_generator\_0\_0\_rd\_b...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_0\_rd\_logic [design\_1\_fifo\_generator\_0\_0\_rd\_l...]

Compiling architecture lut6\_v of entity unisim.LUT6 [\LUT6(init="11111111110000001111...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_0\_compare [design\_1\_fifo\_generator\_0\_0\_comp...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_0\_compare\_0 [design\_1\_fifo\_generator\_0\_0\_comp...]

Compiling architecture lut1\_v of entity unisim.LUT1 [\LUT1(init="0010")(0,3)\]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_0\_wr\_status\_flags\_ss [design\_1\_fifo\_generator\_0\_0\_wr\_s...]

Compiling architecture lut4\_v of entity unisim.LUT4 [\LUT4(init="1001000000001001")(0...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_0\_wr\_bin\_cntr [design\_1\_fifo\_generator\_0\_0\_wr\_b...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_0\_wr\_logic [design\_1\_fifo\_generator\_0\_0\_wr\_l...]

Compiling architecture rb36\_internal\_vhdl\_v of entity unisim.RB36\_INTERNAL\_VHDL [\RB36\_INTERNAL\_VHDL(init\_a="0000...]

Compiling architecture ramb36e1\_v of entity unisim.RAMB36E1 [\RAMB36E1(read\_width\_a=36,read\_w...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_0\_blk\_mem\_gen\_prim\_wrapper [design\_1\_fifo\_generator\_0\_0\_blk\_...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_0\_blk\_mem\_gen\_prim\_width [design\_1\_fifo\_generator\_0\_0\_blk\_...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_0\_blk\_mem\_gen\_generic\_cstr [design\_1\_fifo\_generator\_0\_0\_blk\_...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_0\_blk\_mem\_gen\_top [design\_1\_fifo\_generator\_0\_0\_blk\_...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_0\_blk\_mem\_gen\_v8\_3\_6\_synth [design\_1\_fifo\_generator\_0\_0\_blk\_...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_0\_blk\_mem\_gen\_v8\_3\_6 [design\_1\_fifo\_generator\_0\_0\_blk\_...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_0\_memory [design\_1\_fifo\_generator\_0\_0\_memo...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_0\_fifo\_generator\_ramfifo [design\_1\_fifo\_generator\_0\_0\_fifo...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_0\_fifo\_generator\_top [design\_1\_fifo\_generator\_0\_0\_fifo...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_0\_fifo\_generator\_v13\_1\_4\_synth [design\_1\_fifo\_generator\_0\_0\_fifo...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_0\_fifo\_generator\_v13\_1\_4 [design\_1\_fifo\_generator\_0\_0\_fifo...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_0 [design\_1\_fifo\_generator\_0\_0\_defa...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_1\_compare\_1 [design\_1\_fifo\_generator\_0\_1\_comp...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_1\_compare\_2 [design\_1\_fifo\_generator\_0\_1\_comp...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_1\_rd\_status\_flags\_ss [design\_1\_fifo\_generator\_0\_1\_rd\_s...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_1\_rd\_bin\_cntr [design\_1\_fifo\_generator\_0\_1\_rd\_b...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_1\_rd\_logic [design\_1\_fifo\_generator\_0\_1\_rd\_l...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_1\_compare [design\_1\_fifo\_generator\_0\_1\_comp...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_1\_compare\_0 [design\_1\_fifo\_generator\_0\_1\_comp...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_1\_wr\_status\_flags\_ss [design\_1\_fifo\_generator\_0\_1\_wr\_s...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_1\_wr\_bin\_cntr [design\_1\_fifo\_generator\_0\_1\_wr\_b...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_1\_wr\_logic [design\_1\_fifo\_generator\_0\_1\_wr\_l...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_1\_blk\_mem\_gen\_prim\_wrapper [design\_1\_fifo\_generator\_0\_1\_blk\_...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_1\_blk\_mem\_gen\_prim\_width [design\_1\_fifo\_generator\_0\_1\_blk\_...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_1\_blk\_mem\_gen\_generic\_cstr [design\_1\_fifo\_generator\_0\_1\_blk\_...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_1\_blk\_mem\_gen\_top [design\_1\_fifo\_generator\_0\_1\_blk\_...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_1\_blk\_mem\_gen\_v8\_3\_6\_synth [design\_1\_fifo\_generator\_0\_1\_blk\_...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_1\_blk\_mem\_gen\_v8\_3\_6 [design\_1\_fifo\_generator\_0\_1\_blk\_...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_1\_memory [design\_1\_fifo\_generator\_0\_1\_memo...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_1\_fifo\_generator\_ramfifo [design\_1\_fifo\_generator\_0\_1\_fifo...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_1\_fifo\_generator\_top [design\_1\_fifo\_generator\_0\_1\_fifo...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_1\_fifo\_generator\_v13\_1\_4\_synth [design\_1\_fifo\_generator\_0\_1\_fifo...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_1\_fifo\_generator\_v13\_1\_4 [design\_1\_fifo\_generator\_0\_1\_fifo...]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_fifo\_generator\_0\_1 [design\_1\_fifo\_generator\_0\_1\_defa...]

Compiling architecture muxcy\_v of entity unisim.MUXCY [muxcy\_default]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=7,length=0)\]

Compiling architecture struct of entity floating\_point\_v7\_1\_4.carry\_chain [\carry\_chain(c\_xdevicefamily="ki...]

Compiling architecture synth of entity floating\_point\_v7\_1\_4.compare\_eq\_im [\compare\_eq\_im(c\_xdevicefamily="...]

Compiling architecture xorcy\_v of entity unisim.XORCY [xorcy\_default]

Compiling architecture struct of entity floating\_point\_v7\_1\_4.carry\_chain [\carry\_chain(c\_xdevicefamily="ki...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(length=0)\]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=24,length=0,fast\_in...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=16,length=0)\]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=4,length=0)\]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=48,length=0)\]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=24,length=0)\]

Compiling architecture dsp48e1\_v of entity unisim.DSP48E1 [\DSP48E1(acascreg=0,adreg=0,alum...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.dsp48e1\_wrapper [\dsp48e1\_wrapper(a\_width=24,c\_wi...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_latency=...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [delay\_default]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=13,length=0)\]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=27,length=0)\]

Compiling architecture synth of entity floating\_point\_v7\_1\_4.align\_add\_dsp48e1\_sgl [\align\_add\_dsp48e1\_sgl(c\_xdevice...]

Compiling architecture lut5\_v of entity unisim.LUT5 [\LUT5(init="00000000000000001111...]

Compiling architecture lut5\_v of entity unisim.LUT5 [\LUT5(init="00000000000000000000...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=5,length=0)\]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.lead\_zero\_encode\_shift [\lead\_zero\_encode\_shift(ab\_fw=24...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=3,length=0)\]

Compiling architecture lut6\_v of entity unisim.LUT6 [\LUT6(init="11111110010101001011...]

Compiling architecture lut5\_v of entity unisim.LUT5 [\LUT5(init="00010001010111110000...]

Compiling architecture lut5\_v of entity unisim.LUT5 [\LUT5(init="11101110101000001111...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_latency=...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=2)\]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=25,length=0)\]

Compiling architecture dsp48e1\_v of entity unisim.DSP48E1 [\DSP48E1(adreg=0,alumodereg=0,ca...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.dsp48e1\_wrapper [\dsp48e1\_wrapper(a\_width=24,c\_wi...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.norm\_and\_round\_dsp48e1\_sgl [\norm\_and\_round\_dsp48e1\_sgl(c\_mu...]

Compiling architecture lut5\_v of entity unisim.LUT5 [\LUT5(init="10011001100110011001...]

Compiling architecture lut5\_v of entity unisim.LUT5 [\LUT5(init="11111111000000001111...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=9,length=0)\]

Compiling architecture struct of entity floating\_point\_v7\_1\_4.carry\_chain [\carry\_chain(c\_xdevicefamily="ki...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=8,length=0)\]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_latency=...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=10)\]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=4,length=0,fast\_inp...]

Compiling architecture fde\_v of entity unisim.FDE [fde\_default]

Compiling architecture struct of entity floating\_point\_v7\_1\_4.carry\_chain [\carry\_chain(c\_xdevicefamily="ki...]

Compiling architecture synth of entity floating\_point\_v7\_1\_4.compare\_eq\_im [\compare\_eq\_im(c\_xdevicefamily="...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_latency=...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(fast\_input=true)\]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.special\_detect [\special\_detect(a\_fw=24)(1,7)\]

Compiling architecture struct of entity floating\_point\_v7\_1\_4.carry\_chain [\carry\_chain(c\_xdevicefamily="ki...]

Compiling architecture synth of entity floating\_point\_v7\_1\_4.compare\_gt [\compare\_gt(c\_xdevicefamily="kin...]

Compiling architecture synth of entity floating\_point\_v7\_1\_4.compare [\compare(c\_xdevicefamily="kintex...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_latency=...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=8)\]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_latency=...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=9)\]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_latency=...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=2,length=2,fast\_inp...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_latency=...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(length=2,fast\_input=true)...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(length=0,fast\_input=true)...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=2,length=0,fast\_inp...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=12,length=0)\]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.flt\_add\_exp\_sp [\flt\_add\_exp\_sp(c\_xdevicefamily=...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_latency=...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=23)\]

Compiling architecture synth of entity floating\_point\_v7\_1\_4.flt\_dec\_op [\flt\_dec\_op(c\_xdevicefamily="kin...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.flt\_add\_dsp [\flt\_add\_dsp(c\_xdevicefamily="ki...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.flt\_add [\flt\_add(c\_xdevicefamily="kintex...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_latency=...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=32,length=0)\]

Compiling architecture xilinx of entity floating\_point\_v7\_1\_4.floating\_point\_v7\_1\_4\_viv [\floating\_point\_v7\_1\_4\_viv(c\_xde...]

Compiling architecture xilinx of entity floating\_point\_v7\_1\_4.floating\_point\_v7\_1\_4 [\floating\_point\_v7\_1\_4(c\_xdevice...]

Compiling architecture simple\_ap\_fadd\_3\_full\_dsp\_32\_arch of entity xil\_defaultlib.simple\_ap\_fadd\_3\_full\_dsp\_32 [simple\_ap\_fadd\_3\_full\_dsp\_32\_def...]

Compiling architecture arch of entity xil\_defaultlib.simple\_fadd\_32ns\_bkb [simple\_fadd\_32ns\_bkb\_default]

Compiling architecture behav of entity xil\_defaultlib.simple [simple\_default]

Compiling architecture design\_1\_simple\_0\_0\_arch of entity xil\_defaultlib.design\_1\_simple\_0\_0 [design\_1\_simple\_0\_0\_default]

Compiling architecture structure of entity xil\_defaultlib.design\_1 [design\_1\_default]

Compiling architecture structure of entity xil\_defaultlib.design\_1\_wrapper

Built simulation snapshot design\_1\_wrapper\_behav