Vivado Simulator 2017.2

Time resolution is 1 ps

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 100 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 100 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 100 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 100 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Warning: OPMODE Input Warning : The OPMODE 0110X0X with CARRYINSEL 000 to DSP48E1 instance is invalid.

Time: 100010 ps Iteration: 0 Process: /design\_1\_wrapper/design\_1\_i/simple\_0/U0/simple\_fadd\_32ns\_bkb\_U1/simple\_ap\_fadd\_3\_full\_dsp\_32\_u/U0/i\_synth/addsub\_op/ADDSUB/speed\_op/dsp/OP/dsp48e1\_body/ALIGN\_ADD/DSP2/DSP/prcs\_opmode\_drc File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/DSP48E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 200 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 200 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 200 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 200 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 300 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 300 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 300 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 300 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 400 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 400 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 400 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 400 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 500 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 500 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 500 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 500 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 600 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 600 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 600 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 600 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 700 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 700 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 700 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 700 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 800 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 800 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 800 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 800 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 900 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 900 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 900 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 900 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 1000 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 1 us Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 1000 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 1 us Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 1100 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 1100 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 1100 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 1100 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 1200 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 1200 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 1200 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 1200 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 1300 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 1300 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 1300 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 1300 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 1400 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 1400 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 1400 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 1400 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 1500 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 1500 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 1500 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 1500 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 1600 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 1600 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 1600 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 1600 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 1700 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 1700 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 1700 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 1700 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 1800 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 1800 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 1800 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 1800 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 1900 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 1900 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 1900 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 1900 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 2000 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 2 us Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 2000 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 2 us Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 2100 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 2100 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 2100 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 2100 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 2200 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 2200 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 2200 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 2200 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 2300 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 2300 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 2300 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 2300 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 2400 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 2400 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 2400 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 2400 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 2500 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 2500 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 2500 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 2500 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 2600 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 2600 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 2600 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 2600 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 2700 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 2700 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 2700 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 2700 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 2800 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 2800 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 2800 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 2800 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 2900 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 2900 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 2900 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 2900 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 3000 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 3 us Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 3000 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 3 us Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 3100 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 3100 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 3100 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 3100 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 3200 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 3200 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 3200 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 3200 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 3300 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 3300 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 3300 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 3300 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 3400 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 3400 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 3400 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 3400 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 3500 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 3500 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 3500 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 3500 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 3600 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 3600 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 3600 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 3600 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 3700 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 3700 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 3700 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 3700 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 3800 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 3800 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 3800 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 3800 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 3900 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 3900 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 3900 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 3900 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 4000 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 4 us Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 4000 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 4 us Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 4100 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 4100 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 4100 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 4100 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 4200 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 4200 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 4200 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 4200 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 4300 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 4300 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 4300 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 4300 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 4400 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 4400 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 4400 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 4400 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 4500 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 4500 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 4500 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 4500 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 4600 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 4600 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 4600 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 4600 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 4700 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 4700 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 4700 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 4700 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 4800 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 4800 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 4800 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 4800 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 4900 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 4900 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 4900 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 4900 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 5000 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 5 us Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 5000 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 5 us Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 5100 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 5100 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 5100 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 5100 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 5200 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 5200 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 5200 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 5200 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 5300 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 5300 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 5300 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 5300 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 5400 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 5400 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 5400 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 5400 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 5500 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 5500 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 5500 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 5500 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 5600 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 5600 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 5600 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 5600 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 5700 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 5700 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 5700 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 5700 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 5800 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 5800 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 5800 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 5800 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 5900 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 5900 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 5900 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 5900 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 6000 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 6 us Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 6000 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 6 us Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 6100 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 6100 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

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A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 6100 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 6200 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 6200 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 6200 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 6200 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 6300 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 6300 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 6300 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 6300 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 6400 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 6400 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

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A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 6400 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 6500 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 6500 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

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A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 6500 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

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A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 6600 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

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A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 6600 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

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A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 6700 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

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A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 6700 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

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A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 6800 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 6800 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 6800 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 6900 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 6900 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 6900 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 6900 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 7000 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 7 us Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 7000 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 7 us Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 7100 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 7100 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 7100 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 7100 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 7200 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 7200 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 7200 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 7200 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 7300 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 7300 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 7300 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 7300 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 7400 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 7400 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 7400 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 7400 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 7500 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 7500 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 7500 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 7500 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 7600 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 7600 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 7600 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 7600 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 7700 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 7700 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 7700 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 7700 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 7800 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 7800 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 7800 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 7800 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 7900 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 7900 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 7900 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 7900 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 8000 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 8 us Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 8000 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 8 us Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 8100 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 8100 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 8100 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 8100 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 8200 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 8200 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 8200 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 8200 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 8300 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 8300 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 8300 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 8300 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 8400 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 8400 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 8400 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 8400 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 8500 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 8500 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 8500 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 8500 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 8600 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 8600 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 8600 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 8600 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 8700 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 8700 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 8700 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 8700 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 8800 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 8800 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 8800 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 8800 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 8900 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 8900 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 8900 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 8900 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 9000 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 9 us Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 9000 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 9 us Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 9100 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 9100 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 9100 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 9100 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 9200 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 9200 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 9200 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 9200 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 9300 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 9300 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_1:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 9300 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 9300 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_1/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

Error: Memory Collision Error on RAMB36E1 ::design\_1\_wrapper:design\_1\_i:fifo\_generator\_0:U0:inst\_fifo\_gen:\gconvfifo.rf\:\grf.rf\:\gntv\_or\_sync\_fifo.mem\:\gbm.gbmg.gbmga.ngecc.bmg\:inst\_blk\_mem\_gen:\gnbram.gnativebmg.native\_blk\_mem\_gen\:\valid.cstr\:\ramloop[0].ram.r\:\prim\_noinit.ram\:\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\:tdp:RAMB36E1\_TDP\_inst: at simulation time 9400 ns.

A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 9400 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

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Time: 9500 ns Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

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A read was performed on address 801f (hex) of port B while a write was requested to the same address on port A. The write will be successful however the read value on port B is unknown until the next CLKB cycle.

Time: 10 us Iteration: 3 Process: /design\_1\_wrapper/design\_1\_i/fifo\_generator\_0/U0/inst\_fifo\_gen/\gconvfifo.rf\/\grf.rf\/\gntv\_or\_sync\_fifo.mem\/\gbm.gbmg.gbmga.ngecc.bmg\/inst\_blk\_mem\_gen/\gnbram.gnativebmg.native\_blk\_mem\_gen\/\valid.cstr\/\ramloop[0].ram.r\/\prim\_noinit.ram\/\DEVICE\_7SERIES.NO\_BMM\_INFO.SDP.SIMPLE\_PRIM36.ram\/tdp/RAMB36E1\_TDP\_inst/prcs\_clk File: /wrk/2017.2/nightly/2017\_06\_15\_1909853/data/vhdl/src/unisims/primitive/RAMB36E1.vhd

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