@I [SIM-47] Using XSIM for RTL simulation.

@I [SIM-14] Instrumenting C test bench ...

Build using "/opt/Xilinx/Vivado\_HLS/2017.2/lnx64/tools/gcc/bin/g++"

Compiling apatb\_simple.cpp

Compiling (apcc) add.c\_pre.c.tb.c

INFO: [HLS 200-10] Running '/opt/Xilinx/Vivado\_HLS/2017.2/bin/unwrapped/lnx64.o/apcc'

INFO: [HLS 200-10] For user 'root' on host 'drsatya-OptiPlex-990' (Linux\_x86\_64 version 3.8.0-38-generic) on Thu Mar 08 11:51:08 IST 2018

INFO: [HLS 200-10] On os Ubuntu 12.04.4 LTS

INFO: [HLS 200-10] In directory '/opt/Xilinx/Vivado\_HLS/2017.2/bin/sequence\_1\_8\_march/solution1/sim/wrapc'

clang: warning: argument unused during compilation: '-fno-builtin-isinf'

clang: warning: argument unused during compilation: '-fno-builtin-isnan'

INFO: [APCC 202-3] Tmp directory is /tmp/apcc\_db\_root/119781520490068460868

INFO: [APCC 202-1] APCC is done.

Compiling (apcc) add\_tb.c\_pre.c.tb.c

INFO: [HLS 200-10] Running '/opt/Xilinx/Vivado\_HLS/2017.2/bin/unwrapped/lnx64.o/apcc'

INFO: [HLS 200-10] For user 'root' on host 'drsatya-OptiPlex-990' (Linux\_x86\_64 version 3.8.0-38-generic) on Thu Mar 08 11:51:09 IST 2018

INFO: [HLS 200-10] On os Ubuntu 12.04.4 LTS

INFO: [HLS 200-10] In directory '/opt/Xilinx/Vivado\_HLS/2017.2/bin/sequence\_1\_8\_march/solution1/sim/wrapc'

clang: warning: argument unused during compilation: '-fno-builtin-isinf'

clang: warning: argument unused during compilation: '-fno-builtin-isnan'

INFO: [APCC 202-3] Tmp directory is /tmp/apcc\_db\_root/120311520490069239685

INFO: [APCC 202-1] APCC is done.

Generating cosim.tv.exe

@I [SIM-302] Starting C TB testing ...

@I [SIM-333] Generating C post check test bench ...

@I [SIM-12] Generating RTL test bench ...

@I [SIM-322] Starting VHDL simulation.

@I [SIM-15] Starting XSIM ...

@I [SIM-316] Starting C post checking ...

2.000000

4.000000

6.000000

8.000000

10.000000

12.000000

14.000000

16.000000

INFO: [XSIM 43-3496] Using init file passed via -initfile option "/opt/Xilinx/Vivado/2017.2/data/xsim/ip/xsim\_ip.ini".

Vivado Simulator 2017.2

Copyright 1986-1999, 2001-2016 Xilinx, Inc. All Rights Reserved.

Running: /opt/Xilinx/Vivado/2017.2/bin/unwrapped/lnx64.o/xelab xil\_defaultlib.apatb\_simple\_top -prj simple.prj -L axi\_protocol\_checker\_v1\_1\_12 -L axi\_protocol\_checker\_v1\_1\_13 -L axis\_protocol\_checker\_v1\_1\_11 -L axis\_protocol\_checker\_v1\_1\_12 --initfile /opt/Xilinx/Vivado/2017.2/data/xsim/ip/xsim\_ip.ini --lib ieee\_proposed=./ieee\_proposed -s simple

Multi-threading is on. Using 2 slave threads.

Determining compilation order of HDL files.

WARNING: [XSIM 43-3431] One or more environment variables have been detected which affect the operation of the C compiler. These are typically not set in standard installations and are not tested by Xilinx, however they may be appropriate for your system, so the flow will attempt to continue. If errors occur, try running fuse with the "-mt off -v 1" switches to see more information from the C compiler. The following environment variables have been detected:

LIBRARY\_PATH

INFO: [VRFC 10-163] Analyzing VHDL file "/opt/Xilinx/Vivado\_HLS/2017.2/bin/sequence\_1\_8\_march/solution1/sim/vhdl/AESL\_sim\_pkg.vhd" into library xil\_defaultlib

INFO: [VRFC 10-163] Analyzing VHDL file "/opt/Xilinx/Vivado\_HLS/2017.2/bin/sequence\_1\_8\_march/solution1/sim/vhdl/ip/xil\_defaultlib/simple\_ap\_fadd\_3\_full\_dsp\_32.vhd" into library xil\_defaultlib

INFO: [VRFC 10-307] analyzing entity simple\_ap\_fadd\_3\_full\_dsp\_32

INFO: [VRFC 10-163] Analyzing VHDL file "/opt/Xilinx/Vivado\_HLS/2017.2/bin/sequence\_1\_8\_march/solution1/sim/vhdl/simple.autotb.vhd" into library xil\_defaultlib

INFO: [VRFC 10-307] analyzing entity apatb\_simple\_top

INFO: [VRFC 10-163] Analyzing VHDL file "/opt/Xilinx/Vivado\_HLS/2017.2/bin/sequence\_1\_8\_march/solution1/sim/vhdl/AESL\_automem\_b.vhd" into library xil\_defaultlib

INFO: [VRFC 10-307] analyzing entity AESL\_automem\_b

INFO: [VRFC 10-163] Analyzing VHDL file "/opt/Xilinx/Vivado\_HLS/2017.2/bin/sequence\_1\_8\_march/solution1/sim/vhdl/simple\_fadd\_32ns\_bkb.vhd" into library xil\_defaultlib

INFO: [VRFC 10-307] analyzing entity simple\_fadd\_32ns\_bkb

INFO: [VRFC 10-163] Analyzing VHDL file "/opt/Xilinx/Vivado\_HLS/2017.2/bin/sequence\_1\_8\_march/solution1/sim/vhdl/AESL\_automem\_a.vhd" into library xil\_defaultlib

INFO: [VRFC 10-307] analyzing entity AESL\_automem\_a

INFO: [VRFC 10-163] Analyzing VHDL file "/opt/Xilinx/Vivado\_HLS/2017.2/bin/sequence\_1\_8\_march/solution1/sim/vhdl/AESL\_automem\_c.vhd" into library xil\_defaultlib

INFO: [VRFC 10-307] analyzing entity AESL\_automem\_c

INFO: [VRFC 10-163] Analyzing VHDL file "/opt/Xilinx/Vivado\_HLS/2017.2/bin/sequence\_1\_8\_march/solution1/sim/vhdl/simple.vhd" into library xil\_defaultlib

INFO: [VRFC 10-307] analyzing entity simple

Starting static elaboration

WARNING: [VRFC 10-1303] range is empty (null range) [/wrk/2017.2/nightly/2017\_06\_15\_1909853/packages/customer/vivado/data/ip/xilinx/mult\_gen\_v12\_0/hdl/mult\_gen\_v12\_0\_vh\_rfs.vhd:2255]

WARNING: [VRFC 10-1303] range is empty (null range) [/wrk/2017.2/nightly/2017\_06\_15\_1909853/packages/customer/vivado/data/ip/xilinx/mult\_gen\_v12\_0/hdl/mult\_gen\_v12\_0\_vh\_rfs.vhd:2240]

WARNING: [VRFC 10-1303] range is empty (null range) [/wrk/2017.2/nightly/2017\_06\_15\_1909853/packages/customer/vivado/data/ip/xilinx/floating\_point\_v7\_1/hdl/floating\_point\_v7\_1\_vh\_rfs.vhd:90362]

WARNING: [VRFC 10-1303] range is empty (null range) [/wrk/2017.2/nightly/2017\_06\_15\_1909853/packages/customer/vivado/data/ip/xilinx/xbip\_pipe\_v3\_0/hdl/xbip\_pipe\_v3\_0\_vh\_rfs.vhd:375]

WARNING: [VRFC 10-1303] range is empty (null range) [/wrk/2017.2/nightly/2017\_06\_15\_1909853/packages/customer/vivado/data/ip/xilinx/floating\_point\_v7\_1/hdl/floating\_point\_v7\_1\_vh\_rfs.vhd:12604]

WARNING: [VRFC 10-1303] range is empty (null range) [/wrk/2017.2/nightly/2017\_06\_15\_1909853/packages/customer/vivado/data/ip/xilinx/floating\_point\_v7\_1/hdl/floating\_point\_v7\_1\_vh\_rfs.vhd:12604]

WARNING: [VRFC 10-1303] range is empty (null range) [/wrk/2017.2/nightly/2017\_06\_15\_1909853/packages/customer/vivado/data/ip/xilinx/xbip\_pipe\_v3\_0/hdl/xbip\_pipe\_v3\_0\_vh\_rfs.vhd:375]

WARNING: [VRFC 10-1303] range is empty (null range) [/wrk/2017.2/nightly/2017\_06\_15\_1909853/packages/customer/vivado/data/ip/xilinx/xbip\_pipe\_v3\_0/hdl/xbip\_pipe\_v3\_0\_vh\_rfs.vhd:375]

WARNING: [VRFC 10-1303] range is empty (null range) [/wrk/2017.2/nightly/2017\_06\_15\_1909853/packages/customer/vivado/data/ip/xilinx/xbip\_pipe\_v3\_0/hdl/xbip\_pipe\_v3\_0\_vh\_rfs.vhd:375]

WARNING: [VRFC 10-1303] range is empty (null range) [/wrk/2017.2/nightly/2017\_06\_15\_1909853/packages/customer/vivado/data/ip/xilinx/xbip\_pipe\_v3\_0/hdl/xbip\_pipe\_v3\_0\_vh\_rfs.vhd:375]

WARNING: [VRFC 10-1303] range is empty (null range) [/wrk/2017.2/nightly/2017\_06\_15\_1909853/packages/customer/vivado/data/ip/xilinx/xbip\_pipe\_v3\_0/hdl/xbip\_pipe\_v3\_0\_vh\_rfs.vhd:375]

WARNING: [VRFC 10-1303] range is empty (null range) [/wrk/2017.2/nightly/2017\_06\_15\_1909853/packages/customer/vivado/data/ip/xilinx/xbip\_pipe\_v3\_0/hdl/xbip\_pipe\_v3\_0\_vh\_rfs.vhd:375]

WARNING: [VRFC 10-1303] range is empty (null range) [/wrk/2017.2/nightly/2017\_06\_15\_1909853/packages/customer/vivado/data/ip/xilinx/floating\_point\_v7\_1/hdl/floating\_point\_v7\_1\_vh\_rfs.vhd:12604]

WARNING: [VRFC 10-1303] range is empty (null range) [/wrk/2017.2/nightly/2017\_06\_15\_1909853/packages/customer/vivado/data/ip/xilinx/floating\_point\_v7\_1/hdl/floating\_point\_v7\_1\_vh\_rfs.vhd:12604]

WARNING: [VRFC 10-1303] range is empty (null range) [/wrk/2017.2/nightly/2017\_06\_15\_1909853/packages/customer/vivado/data/ip/xilinx/floating\_point\_v7\_1/hdl/floating\_point\_v7\_1\_vh\_rfs.vhd:12604]

WARNING: [VRFC 10-1303] range is empty (null range) [/wrk/2017.2/nightly/2017\_06\_15\_1909853/packages/customer/vivado/data/ip/xilinx/floating\_point\_v7\_1/hdl/floating\_point\_v7\_1\_vh\_rfs.vhd:12604]

WARNING: [VRFC 10-1303] range is empty (null range) [/wrk/2017.2/nightly/2017\_06\_15\_1909853/packages/customer/vivado/data/ip/xilinx/floating\_point\_v7\_1/hdl/floating\_point\_v7\_1\_vh\_rfs.vhd:13629]

WARNING: [VRFC 10-982] library name floating\_point\_v7\_1\_4 of instantiated unit conflicts with visible identifier [ip/xil\_defaultlib/simple\_ap\_fadd\_3\_full\_dsp\_32.vhd:189]

Completed static elaboration

Starting simulation data flow analysis

Completed simulation data flow analysis

Time Resolution for simulation is 1ps

Compiling package std.standard

Compiling package std.textio

Compiling package ieee.std\_logic\_1164

Compiling package ieee.std\_logic\_arith

Compiling package ieee.std\_logic\_unsigned

Compiling package ieee.numeric\_std

Compiling package ieee.std\_logic\_textio

Compiling package floating\_point\_v7\_1\_4.floating\_point\_v7\_1\_4\_viv\_comp

Compiling package xbip\_utils\_v3\_0\_7.xbip\_utils\_v3\_0\_7\_pkg

Compiling package axi\_utils\_v2\_0\_3.axi\_utils\_v2\_0\_3\_pkg

Compiling package floating\_point\_v7\_1\_4.floating\_point\_v7\_1\_4\_consts

Compiling package ieee.math\_real

Compiling package floating\_point\_v7\_1\_4.floating\_point\_v7\_1\_4\_exp\_table\_...

Compiling package mult\_gen\_v12\_0\_12.mult\_gen\_v12\_0\_12\_pkg

Compiling package ieee.std\_logic\_signed

Compiling package floating\_point\_v7\_1\_4.floating\_point\_v7\_1\_4\_pkg

Compiling package floating\_point\_v7\_1\_4.flt\_utils

Compiling package xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv\_comp

Compiling package unisim.vcomponents

Compiling package ieee.vital\_timing

Compiling package ieee.vital\_primitives

Compiling package unisim.vpkg

Compiling architecture muxcy\_v of entity unisim.MUXCY [muxcy\_default]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=7,length=0)\]

Compiling architecture struct of entity floating\_point\_v7\_1\_4.carry\_chain [\carry\_chain(c\_xdevicefamily="ar...]

Compiling architecture synth of entity floating\_point\_v7\_1\_4.compare\_eq\_im [\compare\_eq\_im(c\_xdevicefamily="...]

Compiling architecture xorcy\_v of entity unisim.XORCY [xorcy\_default]

Compiling architecture struct of entity floating\_point\_v7\_1\_4.carry\_chain [\carry\_chain(c\_xdevicefamily="ar...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(length=0)\]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=24,length=0,fast\_in...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=16,length=0)\]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=4,length=0)\]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=48,length=0)\]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=24,length=0)\]

Compiling architecture dsp48e1\_v of entity unisim.DSP48E1 [\DSP48E1(acascreg=0,adreg=0,alum...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.dsp48e1\_wrapper [\dsp48e1\_wrapper(a\_width=24,c\_wi...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_latency=...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [delay\_default]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=13,length=0)\]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=27,length=0)\]

Compiling architecture synth of entity floating\_point\_v7\_1\_4.align\_add\_dsp48e1\_sgl [\align\_add\_dsp48e1\_sgl(c\_xdevice...]

Compiling architecture lut5\_v of entity unisim.LUT5 [\LUT5(init="00000000000000001111...]

Compiling architecture lut5\_v of entity unisim.LUT5 [\LUT5(init="00000000000000000000...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=5,length=0)\]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.lead\_zero\_encode\_shift [\lead\_zero\_encode\_shift(ab\_fw=24...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=3,length=0)\]

Compiling architecture lut6\_v of entity unisim.LUT6 [\LUT6(init="11111110010101001011...]

Compiling architecture lut5\_v of entity unisim.LUT5 [\LUT5(init="00010001010111110000...]

Compiling architecture lut5\_v of entity unisim.LUT5 [\LUT5(init="11101110101000001111...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_latency=...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=2)\]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=25,length=0)\]

Compiling architecture dsp48e1\_v of entity unisim.DSP48E1 [\DSP48E1(adreg=0,alumodereg=0,ca...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.dsp48e1\_wrapper [\dsp48e1\_wrapper(a\_width=24,c\_wi...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.norm\_and\_round\_dsp48e1\_sgl [\norm\_and\_round\_dsp48e1\_sgl(c\_mu...]

Compiling architecture lut5\_v of entity unisim.LUT5 [\LUT5(init="10011001100110011001...]

Compiling architecture lut5\_v of entity unisim.LUT5 [\LUT5(init="11111111000000001111...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=9,length=0)\]

Compiling architecture struct of entity floating\_point\_v7\_1\_4.carry\_chain [\carry\_chain(c\_xdevicefamily="ar...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=8,length=0)\]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_latency=...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=10)\]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=4,length=0,fast\_inp...]

Compiling architecture fdre\_v of entity unisim.FDRE [fdre\_default]

Compiling architecture fde\_v of entity unisim.FDE [fde\_default]

Compiling architecture struct of entity floating\_point\_v7\_1\_4.carry\_chain [\carry\_chain(c\_xdevicefamily="ar...]

Compiling architecture synth of entity floating\_point\_v7\_1\_4.compare\_eq\_im [\compare\_eq\_im(c\_xdevicefamily="...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_latency=...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(fast\_input=true)\]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.special\_detect [\special\_detect(c\_xdevicefamily=...]

Compiling architecture struct of entity floating\_point\_v7\_1\_4.carry\_chain [\carry\_chain(c\_xdevicefamily="ar...]

Compiling architecture synth of entity floating\_point\_v7\_1\_4.compare\_gt [\compare\_gt(c\_xdevicefamily="art...]

Compiling architecture synth of entity floating\_point\_v7\_1\_4.compare [\compare(c\_xdevicefamily="artix7...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_latency=...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=8)\]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_latency=...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=9)\]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_latency=...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=2,length=2,fast\_inp...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_latency=...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(length=2,fast\_input=true)...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(length=0,fast\_input=true)...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=2,length=0,fast\_inp...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=12,length=0)\]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.flt\_add\_exp\_sp [\flt\_add\_exp\_sp(c\_xdevicefamily=...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_latency=...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=23)\]

Compiling architecture synth of entity floating\_point\_v7\_1\_4.flt\_dec\_op [\flt\_dec\_op(c\_xdevicefamily="art...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.flt\_add\_dsp [\flt\_add\_dsp(c\_xdevicefamily="ar...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.flt\_add [\flt\_add(c\_xdevicefamily="artix7...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_latency=...]

Compiling architecture synth of entity xbip\_pipe\_v3\_0\_3.xbip\_pipe\_v3\_0\_3\_viv [\xbip\_pipe\_v3\_0\_3\_viv(c\_has\_ce=1...]

Compiling architecture rtl of entity floating\_point\_v7\_1\_4.delay [\delay(width=32,length=0)\]

Compiling architecture xilinx of entity floating\_point\_v7\_1\_4.floating\_point\_v7\_1\_4\_viv [\floating\_point\_v7\_1\_4\_viv(c\_xde...]

Compiling architecture xilinx of entity floating\_point\_v7\_1\_4.floating\_point\_v7\_1\_4 [\floating\_point\_v7\_1\_4(c\_xdevice...]

Compiling architecture simple\_ap\_fadd\_3\_full\_dsp\_32\_arch of entity xil\_defaultlib.simple\_ap\_fadd\_3\_full\_dsp\_32 [simple\_ap\_fadd\_3\_full\_dsp\_32\_def...]

Compiling architecture arch of entity xil\_defaultlib.simple\_fadd\_32ns\_bkb [simple\_fadd\_32ns\_bkb\_default]

Compiling architecture behav of entity xil\_defaultlib.simple [simple\_default]

Compiling architecture behav of entity xil\_defaultlib.AESL\_automem\_a [aesl\_automem\_a\_default]

Compiling architecture behav of entity xil\_defaultlib.AESL\_automem\_b [aesl\_automem\_b\_default]

Compiling architecture behav of entity xil\_defaultlib.AESL\_automem\_c [aesl\_automem\_c\_default]

Compiling architecture behav of entity xil\_defaultlib.apatb\_simple\_top

Built simulation snapshot simple

\*\*\*\*\*\* Webtalk v2017.2 (64-bit)

\*\*\*\* SW Build 1909853 on Thu Jun 15 18:39:10 MDT 2017

\*\*\*\* IP Build 1909766 on Thu Jun 15 19:58:00 MDT 2017

\*\* Copyright 1986-2017 Xilinx, Inc. All Rights Reserved.

source /opt/Xilinx/Vivado\_HLS/2017.2/bin/sequence\_1\_8\_march/solution1/sim/vhdl/xsim.dir/simple/webtalk/xsim\_webtalk.tcl -notrace

INFO: [Common 17-206] Exiting Webtalk at Thu Mar 8 11:51:48 2018...

\*\*\*\*\*\* xsim v2017.2 (64-bit)

\*\*\*\* SW Build 1909853 on Thu Jun 15 18:39:10 MDT 2017

\*\*\*\* IP Build 1909766 on Thu Jun 15 19:58:00 MDT 2017

\*\* Copyright 1986-2017 Xilinx, Inc. All Rights Reserved.

source xsim.dir/simple/xsim\_script.tcl

# xsim {simple} -autoloadwcfg -tclbatch {simple.tcl}

Vivado Simulator 2017.2

Time resolution is 1 ps

source simple.tcl

## run all

Note: simulation done!

Time: 675 ns Iteration: 1 Process: /apatb\_simple\_top/generate\_sim\_done\_proc File: /opt/Xilinx/Vivado\_HLS/2017.2/bin/sequence\_1\_8\_march/solution1/sim/vhdl/simple.autotb.vhd

Failure: NORMAL EXIT (note: failure is to force the simulator to stop)

Time: 675 ns Iteration: 1 Process: /apatb\_simple\_top/generate\_sim\_done\_proc File: /opt/Xilinx/Vivado\_HLS/2017.2/bin/sequence\_1\_8\_march/solution1/sim/vhdl/simple.autotb.vhd

$finish called at time : 675 ns

## quit

INFO: [Common 17-206] Exiting xsim at Thu Mar 8 11:51:59 2018...

2.000000

4.000000

6.000000

8.000000

10.000000

12.000000

14.000000

16.000000

@I [SIM-1000] \*\*\* C/RTL co-simulation finished: PASS \*\*\*

@I [SIM-211] II is measurable only when transaction number is greater than 1 in RTL simulation. Otherwise, they will be marked as all NA. If user wants to calculate them, please make sure there are at least 2 transactions in RTL simulation.