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# xsim v2017.2 (64-bit)

# SW Build 1909853 on Thu Jun 15 18:39:10 MDT 2017

# IP Build 1909766 on Thu Jun 15 19:58:00 MDT 2017

# Start of session at: Thu Mar 8 11:51:49 2018

# Process ID: 12415

# Current directory: /opt/Xilinx/Vivado\_HLS/2017.2/bin/sequence\_1\_8\_march/solution1/sim/vhdl

# Command line: xsim -mode tcl -source {xsim.dir/simple/xsim\_script.tcl}

# Log file: /opt/Xilinx/Vivado\_HLS/2017.2/bin/sequence\_1\_8\_march/solution1/sim/vhdl/xsim.log

# Journal file: /opt/Xilinx/Vivado\_HLS/2017.2/bin/sequence\_1\_8\_march/solution1/sim/vhdl/xsim.jou

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source xsim.dir/simple/xsim\_script.tcl

# xsim {simple} -autoloadwcfg -tclbatch {simple.tcl}

Vivado Simulator 2017.2

Time resolution is 1 ps

source simple.tcl

## run all

Note: simulation done!

Time: 675 ns Iteration: 1 Process: /apatb\_simple\_top/generate\_sim\_done\_proc File: /opt/Xilinx/Vivado\_HLS/2017.2/bin/sequence\_1\_8\_march/solution1/sim/vhdl/simple.autotb.vhd

Failure: NORMAL EXIT (note: failure is to force the simulator to stop)

Time: 675 ns Iteration: 1 Process: /apatb\_simple\_top/generate\_sim\_done\_proc File: /opt/Xilinx/Vivado\_HLS/2017.2/bin/sequence\_1\_8\_march/solution1/sim/vhdl/simple.autotb.vhd

$finish called at time : 675 ns

## quit

INFO: [Common 17-206] Exiting xsim at Thu Mar 8 11:51:59 2018...