\*\*\* Running vivado

with args -log design\_1\_simple\_0\_0.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source design\_1\_simple\_0\_0.tcl

\*\*\*\*\*\* Vivado v2017.2 (64-bit)

\*\*\*\* SW Build 1909853 on Thu Jun 15 18:39:10 MDT 2017

\*\*\*\* IP Build 1909766 on Thu Jun 15 19:58:00 MDT 2017

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source design\_1\_simple\_0\_0.tcl -notrace

Command: synth\_design -top design\_1\_simple\_0\_0 -part xcku035-ffva1156-3-e -mode out\_of\_context

Starting synth\_design

Attempting to get a license for feature 'Synthesis' and/or device 'xcku035-ffva1156'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xcku035-ffva1156'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 32746

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Starting RTL Elaboration : Time (s): cpu = 00:00:04 ; elapsed = 00:00:04 . Memory (MB): peak = 1164.543 ; gain = 17.000 ; free physical = 370 ; free virtual = 4390

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INFO: [Synth 8-638] synthesizing module 'design\_1\_simple\_0\_0' [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ip/design\_1\_simple\_0\_0/synth/design\_1\_simple\_0\_0.vhd:100]

INFO: [Synth 8-3491] module 'simple' declared at '/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple.vhd:12' bound to instance 'U0' of component 'simple' [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ip/design\_1\_simple\_0\_0/synth/design\_1\_simple\_0\_0.vhd:185]

INFO: [Synth 8-638] synthesizing module 'simple' [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple.vhd:56]

INFO: [Synth 8-5534] Detected attribute (\* fsm\_encoding = "none" \*) [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple.vhd:70]

INFO: [Synth 8-5534] Detected attribute (\* fsm\_encoding = "none" \*) [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple.vhd:73]

INFO: [Synth 8-5534] Detected attribute (\* fsm\_encoding = "none" \*) [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple.vhd:76]

INFO: [Synth 8-3491] module 'simple\_fadd\_32ns\_bkb' declared at '/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple\_fadd\_32ns\_bkb.vhd:11' bound to instance 'simple\_fadd\_32ns\_bkb\_U1' of component 'simple\_fadd\_32ns\_bkb' [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple.vhd:106]

INFO: [Synth 8-638] synthesizing module 'simple\_fadd\_32ns\_bkb' [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple\_fadd\_32ns\_bkb.vhd:29]

INFO: [Synth 8-3491] module 'simple\_ap\_fadd\_2\_full\_dsp\_32' declared at '/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/ip/simple\_ap\_fadd\_2\_full\_dsp\_32.vhd:59' bound to instance 'simple\_ap\_fadd\_2\_full\_dsp\_32\_u' of component 'simple\_ap\_fadd\_2\_full\_dsp\_32' [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple\_fadd\_32ns\_bkb.vhd:56]

INFO: [Synth 8-638] synthesizing module 'simple\_ap\_fadd\_2\_full\_dsp\_32' [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/ip/simple\_ap\_fadd\_2\_full\_dsp\_32.vhd:72]

INFO: [Synth 8-3491] module 'floating\_point\_v7\_1\_4' declared at '/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/4a02/hdl/floating\_point\_v7\_1\_vh\_rfs.vhd:91604' bound to instance 'U0' of component 'floating\_point\_v7\_1\_4' [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/ip/simple\_ap\_fadd\_2\_full\_dsp\_32.vhd:197]

INFO: [Synth 8-256] done synthesizing module 'simple\_ap\_fadd\_2\_full\_dsp\_32' (18#1) [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/ip/simple\_ap\_fadd\_2\_full\_dsp\_32.vhd:72]

INFO: [Synth 8-256] done synthesizing module 'simple\_fadd\_32ns\_bkb' (19#1) [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple\_fadd\_32ns\_bkb.vhd:29]

INFO: [Synth 8-3491] module 'simple\_fadd\_32ns\_bkb' declared at '/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple\_fadd\_32ns\_bkb.vhd:11' bound to instance 'simple\_fadd\_32ns\_bkb\_U2' of component 'simple\_fadd\_32ns\_bkb' [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple.vhd:121]

INFO: [Synth 8-3491] module 'simple\_fadd\_32ns\_bkb' declared at '/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple\_fadd\_32ns\_bkb.vhd:11' bound to instance 'simple\_fadd\_32ns\_bkb\_U3' of component 'simple\_fadd\_32ns\_bkb' [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple.vhd:136]

INFO: [Synth 8-3491] module 'simple\_fadd\_32ns\_bkb' declared at '/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple\_fadd\_32ns\_bkb.vhd:11' bound to instance 'simple\_fadd\_32ns\_bkb\_U4' of component 'simple\_fadd\_32ns\_bkb' [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple.vhd:151]

INFO: [Synth 8-3491] module 'simple\_fadd\_32ns\_bkb' declared at '/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple\_fadd\_32ns\_bkb.vhd:11' bound to instance 'simple\_fadd\_32ns\_bkb\_U5' of component 'simple\_fadd\_32ns\_bkb' [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple.vhd:166]

INFO: [Synth 8-3491] module 'simple\_fadd\_32ns\_bkb' declared at '/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple\_fadd\_32ns\_bkb.vhd:11' bound to instance 'simple\_fadd\_32ns\_bkb\_U6' of component 'simple\_fadd\_32ns\_bkb' [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple.vhd:181]

INFO: [Synth 8-3491] module 'simple\_fadd\_32ns\_bkb' declared at '/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple\_fadd\_32ns\_bkb.vhd:11' bound to instance 'simple\_fadd\_32ns\_bkb\_U7' of component 'simple\_fadd\_32ns\_bkb' [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple.vhd:196]

INFO: [Synth 8-3491] module 'simple\_fadd\_32ns\_bkb' declared at '/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple\_fadd\_32ns\_bkb.vhd:11' bound to instance 'simple\_fadd\_32ns\_bkb\_U8' of component 'simple\_fadd\_32ns\_bkb' [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple.vhd:211]

WARNING: [Synth 8-6014] Unused sequential element ap\_ready\_reg was removed. [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple.vhd:287]

WARNING: [Synth 8-6014] Unused sequential element c\_0\_ap\_vld\_reg was removed. [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple.vhd:299]

WARNING: [Synth 8-6014] Unused sequential element c\_1\_ap\_vld\_reg was removed. [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple.vhd:310]

WARNING: [Synth 8-6014] Unused sequential element c\_2\_ap\_vld\_reg was removed. [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple.vhd:321]

WARNING: [Synth 8-6014] Unused sequential element c\_3\_ap\_vld\_reg was removed. [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple.vhd:332]

WARNING: [Synth 8-6014] Unused sequential element c\_4\_ap\_vld\_reg was removed. [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple.vhd:343]

WARNING: [Synth 8-6014] Unused sequential element c\_5\_ap\_vld\_reg was removed. [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple.vhd:354]

WARNING: [Synth 8-6014] Unused sequential element c\_6\_ap\_vld\_reg was removed. [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple.vhd:365]

WARNING: [Synth 8-6014] Unused sequential element c\_7\_ap\_vld\_reg was removed. [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple.vhd:376]

INFO: [Synth 8-256] done synthesizing module 'simple' (20#1) [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ipshared/5e80/hdl/vhdl/simple.vhd:56]

INFO: [Synth 8-256] done synthesizing module 'design\_1\_simple\_0\_0' (21#1) [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ip/design\_1\_simple\_0\_0/synth/design\_1\_simple\_0\_0.vhd:100]

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized45 has unconnected port CLK

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized45 has unconnected port CE

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized45 has unconnected port SCLR

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized45 has unconnected port SSET

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized45 has unconnected port SINIT

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized49 has unconnected port CLK

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized49 has unconnected port CE

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized49 has unconnected port SCLR

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized49 has unconnected port SSET

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized49 has unconnected port SINIT

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized47 has unconnected port CLK

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized47 has unconnected port CE

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized47 has unconnected port SCLR

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized47 has unconnected port SSET

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized47 has unconnected port SINIT

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized41 has unconnected port SCLR

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized41 has unconnected port SSET

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized41 has unconnected port SINIT

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized39 has unconnected port CLK

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized39 has unconnected port CE

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized39 has unconnected port SCLR

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized39 has unconnected port SSET

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized39 has unconnected port SINIT

WARNING: [Synth 8-3331] design carry\_chain\_\_parameterized3 has unconnected port B[8]

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized55 has unconnected port CLK

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized55 has unconnected port CE

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized55 has unconnected port SCLR

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized55 has unconnected port SSET

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized55 has unconnected port SINIT

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized53 has unconnected port CLK

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized53 has unconnected port CE

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized53 has unconnected port SCLR

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized53 has unconnected port SSET

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized53 has unconnected port SINIT

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized51 has unconnected port CLK

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized51 has unconnected port CE

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized51 has unconnected port SCLR

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized51 has unconnected port SSET

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized51 has unconnected port SINIT

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized35 has unconnected port SCLR

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized35 has unconnected port SSET

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized35 has unconnected port SINIT

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized43 has unconnected port SCLR

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized43 has unconnected port SSET

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized43 has unconnected port SINIT

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized23 has unconnected port SCLR

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized23 has unconnected port SSET

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized23 has unconnected port SINIT

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized37 has unconnected port SCLR

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized37 has unconnected port SSET

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized37 has unconnected port SINIT

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized3 has unconnected port CLK

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized3 has unconnected port CE

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized3 has unconnected port SCLR

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized3 has unconnected port SSET

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized3 has unconnected port SINIT

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized9 has unconnected port CLK

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized9 has unconnected port CE

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized9 has unconnected port SCLR

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized9 has unconnected port SSET

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized9 has unconnected port SINIT

WARNING: [Synth 8-3331] design carry\_chain\_\_parameterized2 has unconnected port CARRYS\_OUT[14]

WARNING: [Synth 8-3331] design carry\_chain\_\_parameterized2 has unconnected port CARRYS\_OUT[13]

WARNING: [Synth 8-3331] design carry\_chain\_\_parameterized2 has unconnected port CARRYS\_OUT[12]

WARNING: [Synth 8-3331] design carry\_chain\_\_parameterized2 has unconnected port CARRYS\_OUT[11]

WARNING: [Synth 8-3331] design carry\_chain\_\_parameterized2 has unconnected port CARRYS\_OUT[10]

WARNING: [Synth 8-3331] design carry\_chain\_\_parameterized2 has unconnected port CARRYS\_OUT[9]

WARNING: [Synth 8-3331] design carry\_chain\_\_parameterized2 has unconnected port CARRYS\_OUT[8]

WARNING: [Synth 8-3331] design carry\_chain\_\_parameterized2 has unconnected port CARRYS\_OUT[7]

WARNING: [Synth 8-3331] design carry\_chain\_\_parameterized2 has unconnected port CARRYS\_OUT[6]

WARNING: [Synth 8-3331] design carry\_chain\_\_parameterized2 has unconnected port CARRYS\_OUT[5]

WARNING: [Synth 8-3331] design carry\_chain\_\_parameterized2 has unconnected port CARRYS\_OUT[4]

WARNING: [Synth 8-3331] design carry\_chain\_\_parameterized2 has unconnected port CARRYS\_OUT[3]

WARNING: [Synth 8-3331] design carry\_chain\_\_parameterized2 has unconnected port CARRYS\_OUT[2]

WARNING: [Synth 8-3331] design carry\_chain\_\_parameterized2 has unconnected port CARRYS\_OUT[1]

WARNING: [Synth 8-3331] design carry\_chain\_\_parameterized2 has unconnected port CARRYS\_OUT[0]

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized11 has unconnected port CLK

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized11 has unconnected port CE

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized11 has unconnected port SCLR

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized11 has unconnected port SSET

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized11 has unconnected port SINIT

WARNING: [Synth 8-3331] design carry\_chain\_\_parameterized1 has unconnected port CARRYS\_OUT[2]

WARNING: [Synth 8-3331] design carry\_chain\_\_parameterized1 has unconnected port CARRYS\_OUT[1]

WARNING: [Synth 8-3331] design carry\_chain\_\_parameterized1 has unconnected port CARRYS\_OUT[0]

WARNING: [Synth 8-3331] design compare\_eq\_im\_\_parameterized0 has unconnected port CARRYS\_OUT[0]

WARNING: [Synth 8-3331] design special\_detect has unconnected port A[31]

WARNING: [Synth 8-3331] design flt\_add\_exp\_sp has unconnected port ZERO\_ALIGN

WARNING: [Synth 8-3331] design flt\_add\_exp\_sp has unconnected port ROUND\_EXP\_INC

WARNING: [Synth 8-3331] design flt\_add\_exp\_sp has unconnected port ADD\_MANT\_MSBS[1]

WARNING: [Synth 8-3331] design flt\_add\_exp\_sp has unconnected port ADD\_MANT\_MSBS[0]

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized33 has unconnected port CLK

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized33 has unconnected port CE

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized33 has unconnected port SCLR

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized33 has unconnected port SSET

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized33 has unconnected port SINIT

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized15 has unconnected port CLK

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized15 has unconnected port CE

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized15 has unconnected port SCLR

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized15 has unconnected port SSET

WARNING: [Synth 8-3331] design xbip\_pipe\_v3\_0\_3\_viv\_\_parameterized15 has unconnected port SINIT

INFO: [Common 17-14] Message 'Synth 8-3331' appears 100 times and further instances of the messages will be disabled. Use the Tcl command set\_msg\_config to change the current settings.

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Finished RTL Elaboration : Time (s): cpu = 00:00:07 ; elapsed = 00:00:08 . Memory (MB): peak = 1250.047 ; gain = 102.504 ; free physical = 363 ; free virtual = 4386

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Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

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Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:07 ; elapsed = 00:00:08 . Memory (MB): peak = 1250.047 ; gain = 102.504 ; free physical = 365 ; free virtual = 4388

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INFO: [Netlist 29-17] Analyzing 728 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Device 21-403] Loading part xcku035-ffva1156-3-e

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ip/design\_1\_simple\_0\_0/constraints/simple\_ooc.xdc] for cell 'U0'

Finished Parsing XDC File [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/ip/design\_1\_simple\_0\_0/constraints/simple\_ooc.xdc] for cell 'U0'

Parsing XDC File [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.runs/design\_1\_simple\_0\_0\_synth\_1/dont\_touch.xdc]

Finished Parsing XDC File [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.runs/design\_1\_simple\_0\_0\_synth\_1/dont\_touch.xdc]

Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:

A total of 104 instances were transformed.

DSP48E1 => DSP48E2 (DSP\_ALU, DSP\_A\_B\_DATA, DSP\_C\_DATA, DSP\_M\_DATA, DSP\_MULTIPLIER, DSP\_OUTPUT, DSP\_PREADD, DSP\_PREADD\_DATA): 16 instances

FDE => FDRE: 88 instances

Constraint Validation Runtime : Time (s): cpu = 00:00:00.22 ; elapsed = 00:00:00.26 . Memory (MB): peak = 1764.121 ; gain = 1.000 ; free physical = 110 ; free virtual = 3925

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Finished Constraint Validation : Time (s): cpu = 00:00:18 ; elapsed = 00:00:23 . Memory (MB): peak = 1764.125 ; gain = 616.582 ; free physical = 188 ; free virtual = 4004

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Start Loading Part and Timing Information

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Loading part: xcku035-ffva1156-3-e

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Finished Loading Part and Timing Information : Time (s): cpu = 00:00:18 ; elapsed = 00:00:23 . Memory (MB): peak = 1764.125 ; gain = 616.582 ; free physical = 188 ; free virtual = 4005

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Start Applying 'set\_property' XDC Constraints

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Applied set\_property DONT\_TOUCH = true for U0. (constraint file /opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.runs/design\_1\_simple\_0\_0\_synth\_1/dont\_touch.xdc, line 9).

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Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:19 ; elapsed = 00:00:23 . Memory (MB): peak = 1764.125 ; gain = 616.582 ; free physical = 187 ; free virtual = 4006

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INFO: [Synth 8-5546] ROM "exp\_all\_one\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "exp\_all\_zero\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "exp\_over\_int" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ip\_sig" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "exp\_over\_int" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ip\_sig" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5544] ROM "det\_state" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-4490] FSM extraction disabled for register 'ap\_CS\_fsm\_reg' through user attribute

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Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:19 ; elapsed = 00:00:24 . Memory (MB): peak = 1764.125 ; gain = 616.582 ; free physical = 174 ; free virtual = 3998

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INFO: [Synth 8-223] decloning instance 'simple\_fadd\_32ns\_bkb:/simple\_ap\_fadd\_2\_full\_dsp\_32\_u/U0/i\_synth/DELAY\_DIVIDE\_BY\_ZERO' (delay\_\_parameterized0) to 'simple\_fadd\_32ns\_bkb:/simple\_ap\_fadd\_2\_full\_dsp\_32\_u/U0/i\_synth/DELAY\_ACCUM\_OVERFLOW'

INFO: [Synth 8-223] decloning instance 'simple\_fadd\_32ns\_bkb:/simple\_ap\_fadd\_2\_full\_dsp\_32\_u/U0/i\_synth/DELAY\_DIVIDE\_BY\_ZERO' (delay\_\_parameterized0) to 'simple\_fadd\_32ns\_bkb:/simple\_ap\_fadd\_2\_full\_dsp\_32\_u/U0/i\_synth/DELAY\_ACCUM\_INPUT\_OVERFLOW'

INFO: [Synth 8-223] decloning instance 'simple\_fadd\_32ns\_bkb:/simple\_ap\_fadd\_2\_full\_dsp\_32\_u/U0/i\_synth/ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.ALIGN\_ADD/SUB\_DELAY' (delay\_\_parameterized0) to 'simple\_fadd\_32ns\_bkb:/simple\_ap\_fadd\_2\_full\_dsp\_32\_u/U0/i\_synth/ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.ALIGN\_ADD/SUB\_ADD\_IP\_DELAY'

Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

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Start RTL Component Statistics

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Finished RTL Component Statistics

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Start RTL Hierarchical Component Statistics

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Finished RTL Hierarchical Component Statistics

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Start Part Resource Summary

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Part Resources:

DSPs: 1700 (col length:120)

BRAMs: 1080 (col length: RAMB18 120 RAMB36 60)

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Finished Part Resource Summary

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Start Cross Boundary and Area Optimization

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INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_A/exp\_all\_one\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_A/exp\_all\_zero\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_B/exp\_all\_one\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_B/exp\_all\_zero\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/exp\_over\_int" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/ip\_sig" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_A/exp\_all\_one\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_A/exp\_all\_zero\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_B/exp\_all\_one\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_B/exp\_all\_zero\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/exp\_over\_int" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/ip\_sig" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_A/exp\_all\_one\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_A/exp\_all\_zero\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_B/exp\_all\_one\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_B/exp\_all\_zero\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/exp\_over\_int" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/ip\_sig" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_A/exp\_all\_one\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_A/exp\_all\_zero\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_B/exp\_all\_one\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_B/exp\_all\_zero\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/exp\_over\_int" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/ip\_sig" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_A/exp\_all\_one\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_A/exp\_all\_zero\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_B/exp\_all\_one\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_B/exp\_all\_zero\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/exp\_over\_int" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/ip\_sig" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_A/exp\_all\_one\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_A/exp\_all\_zero\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_B/exp\_all\_one\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_B/exp\_all\_zero\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/exp\_over\_int" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/ip\_sig" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_A/exp\_all\_one\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_A/exp\_all\_zero\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_B/exp\_all\_one\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_B/exp\_all\_zero\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/exp\_over\_int" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/ip\_sig" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_A/exp\_all\_one\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_A/exp\_all\_zero\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_B/exp\_all\_one\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/COND\_DET\_B/exp\_all\_zero\_ip" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/exp\_over\_int" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.EXP/ip\_sig" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-3332] Sequential element (i\_nd\_to\_rdy/opt\_has\_pipe.i\_pipe[2].pipe\_reg[2][0]) is unused and will be removed from module floating\_point\_v7\_1\_4\_viv\_\_1.

INFO: [Synth 8-3332] Sequential element (ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.NORM\_RND/FULL\_USAGE\_DSP.LOD/NORM\_DELAY/i\_pipe/opt\_has\_pipe.first\_q\_reg[0]) is unused and will be removed from module floating\_point\_v7\_1\_4\_viv\_\_1.

INFO: [Synth 8-3332] Sequential element (i\_nd\_to\_rdy/opt\_has\_pipe.i\_pipe[2].pipe\_reg[2][0]) is unused and will be removed from module floating\_point\_v7\_1\_4\_viv\_\_2.

INFO: [Synth 8-3332] Sequential element (ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.NORM\_RND/FULL\_USAGE\_DSP.LOD/NORM\_DELAY/i\_pipe/opt\_has\_pipe.first\_q\_reg[0]) is unused and will be removed from module floating\_point\_v7\_1\_4\_viv\_\_2.

INFO: [Synth 8-3332] Sequential element (i\_nd\_to\_rdy/opt\_has\_pipe.i\_pipe[2].pipe\_reg[2][0]) is unused and will be removed from module floating\_point\_v7\_1\_4\_viv\_\_3.

INFO: [Synth 8-3332] Sequential element (ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.NORM\_RND/FULL\_USAGE\_DSP.LOD/NORM\_DELAY/i\_pipe/opt\_has\_pipe.first\_q\_reg[0]) is unused and will be removed from module floating\_point\_v7\_1\_4\_viv\_\_3.

INFO: [Synth 8-3332] Sequential element (i\_nd\_to\_rdy/opt\_has\_pipe.i\_pipe[2].pipe\_reg[2][0]) is unused and will be removed from module floating\_point\_v7\_1\_4\_viv\_\_4.

INFO: [Synth 8-3332] Sequential element (ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.NORM\_RND/FULL\_USAGE\_DSP.LOD/NORM\_DELAY/i\_pipe/opt\_has\_pipe.first\_q\_reg[0]) is unused and will be removed from module floating\_point\_v7\_1\_4\_viv\_\_4.

INFO: [Synth 8-3332] Sequential element (i\_nd\_to\_rdy/opt\_has\_pipe.i\_pipe[2].pipe\_reg[2][0]) is unused and will be removed from module floating\_point\_v7\_1\_4\_viv\_\_5.

INFO: [Synth 8-3332] Sequential element (ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.NORM\_RND/FULL\_USAGE\_DSP.LOD/NORM\_DELAY/i\_pipe/opt\_has\_pipe.first\_q\_reg[0]) is unused and will be removed from module floating\_point\_v7\_1\_4\_viv\_\_5.

INFO: [Synth 8-3332] Sequential element (i\_nd\_to\_rdy/opt\_has\_pipe.i\_pipe[2].pipe\_reg[2][0]) is unused and will be removed from module floating\_point\_v7\_1\_4\_viv\_\_6.

INFO: [Synth 8-3332] Sequential element (ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.NORM\_RND/FULL\_USAGE\_DSP.LOD/NORM\_DELAY/i\_pipe/opt\_has\_pipe.first\_q\_reg[0]) is unused and will be removed from module floating\_point\_v7\_1\_4\_viv\_\_6.

INFO: [Synth 8-3332] Sequential element (i\_nd\_to\_rdy/opt\_has\_pipe.i\_pipe[2].pipe\_reg[2][0]) is unused and will be removed from module floating\_point\_v7\_1\_4\_viv\_\_7.

INFO: [Synth 8-3332] Sequential element (ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.NORM\_RND/FULL\_USAGE\_DSP.LOD/NORM\_DELAY/i\_pipe/opt\_has\_pipe.first\_q\_reg[0]) is unused and will be removed from module floating\_point\_v7\_1\_4\_viv\_\_7.

INFO: [Synth 8-3332] Sequential element (i\_nd\_to\_rdy/opt\_has\_pipe.i\_pipe[2].pipe\_reg[2][0]) is unused and will be removed from module floating\_point\_v7\_1\_4\_viv.

INFO: [Synth 8-3332] Sequential element (ADDSUB\_OP.ADDSUB/SPEED\_OP.DSP.OP/DSP48E1\_BODY.NORM\_RND/FULL\_USAGE\_DSP.LOD/NORM\_DELAY/i\_pipe/opt\_has\_pipe.first\_q\_reg[0]) is unused and will be removed from module floating\_point\_v7\_1\_4\_viv.

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Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:23 ; elapsed = 00:00:30 . Memory (MB): peak = 1764.129 ; gain = 616.586 ; free physical = 150 ; free virtual = 3980

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

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Start Applying XDC Timing Constraints

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Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:33 ; elapsed = 00:00:40 . Memory (MB): peak = 1944.141 ; gain = 796.598 ; free physical = 103 ; free virtual = 3669

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Start Timing Optimization

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Finished Timing Optimization : Time (s): cpu = 00:00:33 ; elapsed = 00:00:41 . Memory (MB): peak = 1962.152 ; gain = 814.609 ; free physical = 108 ; free virtual = 3660

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Technology Mapping

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Finished Technology Mapping : Time (s): cpu = 00:00:35 ; elapsed = 00:00:43 . Memory (MB): peak = 1972.168 ; gain = 824.625 ; free physical = 130 ; free virtual = 3658

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start IO Insertion

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Start Flattening Before IO Insertion

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Finished Flattening Before IO Insertion

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Start Final Netlist Cleanup

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Finished Final Netlist Cleanup

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---------------------------------------------------------------------------------

Finished IO Insertion : Time (s): cpu = 00:00:35 ; elapsed = 00:00:43 . Memory (MB): peak = 1972.168 ; gain = 824.625 ; free physical = 130 ; free virtual = 3657

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Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Renaming Generated Instances

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Finished Renaming Generated Instances : Time (s): cpu = 00:00:35 ; elapsed = 00:00:43 . Memory (MB): peak = 1972.168 ; gain = 824.625 ; free physical = 130 ; free virtual = 3657

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Rebuilding User Hierarchy

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Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:36 ; elapsed = 00:00:44 . Memory (MB): peak = 1972.168 ; gain = 824.625 ; free physical = 127 ; free virtual = 3655

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Start Renaming Generated Ports

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Finished Renaming Generated Ports : Time (s): cpu = 00:00:36 ; elapsed = 00:00:44 . Memory (MB): peak = 1972.168 ; gain = 824.625 ; free physical = 127 ; free virtual = 3655

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:36 ; elapsed = 00:00:44 . Memory (MB): peak = 1972.168 ; gain = 824.625 ; free physical = 126 ; free virtual = 3654

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Start Renaming Generated Nets

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Finished Renaming Generated Nets : Time (s): cpu = 00:00:36 ; elapsed = 00:00:44 . Memory (MB): peak = 1972.168 ; gain = 824.625 ; free physical = 126 ; free virtual = 3654

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Start Writing Synthesis Report

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Report BlackBoxes:

+-+--------------+----------+

| |BlackBox name |Instances |

+-+--------------+----------+

+-+--------------+----------+

Report Cell Usage:

+------+--------+------+

| |Cell |Count |

+------+--------+------+

|1 |DSP48E1 | 16|

|2 |LUT1 | 8|

|3 |LUT2 | 97|

|4 |LUT3 | 577|

|5 |LUT4 | 600|

|6 |LUT5 | 489|

|7 |LUT6 | 376|

|8 |MUXCY | 464|

|9 |XORCY | 136|

|10 |FDE | 88|

|11 |FDRE | 1523|

|12 |FDSE | 1|

+------+--------+------+

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Finished Writing Synthesis Report : Time (s): cpu = 00:00:36 ; elapsed = 00:00:44 . Memory (MB): peak = 1972.168 ; gain = 824.625 ; free physical = 126 ; free virtual = 3654

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Synthesis finished with 0 errors, 0 critical warnings and 416 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:28 ; elapsed = 00:00:33 . Memory (MB): peak = 1972.168 ; gain = 310.551 ; free physical = 148 ; free virtual = 3678

Synthesis Optimization Complete : Time (s): cpu = 00:00:36 ; elapsed = 00:00:44 . Memory (MB): peak = 1972.176 ; gain = 824.625 ; free physical = 148 ; free virtual = 3678

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 704 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

A total of 184 instances were transformed.

(CARRY4) => CARRY8: 80 instances

DSP48E1 => DSP48E2 (DSP\_ALU, DSP\_A\_B\_DATA, DSP\_C\_DATA, DSP\_MULTIPLIER, DSP\_M\_DATA, DSP\_OUTPUT, DSP\_PREADD\_DATA, DSP\_PREADD): 16 instances

FDE => FDRE: 88 instances

110 Infos, 109 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth\_design completed successfully

synth\_design: Time (s): cpu = 00:00:39 ; elapsed = 00:00:49 . Memory (MB): peak = 1998.801 ; gain = 863.840 ; free physical = 151 ; free virtual = 3652

INFO: [Common 17-1381] The checkpoint '/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.runs/design\_1\_simple\_0\_0\_synth\_1/design\_1\_simple\_0\_0.dcp' has been generated.