\*\*\* Running vivado

with args -log design\_1\_wrapper.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source design\_1\_wrapper.tcl

\*\*\*\*\*\* Vivado v2017.2 (64-bit)

\*\*\*\* SW Build 1909853 on Thu Jun 15 18:39:10 MDT 2017

\*\*\*\* IP Build 1909766 on Thu Jun 15 19:58:00 MDT 2017

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source design\_1\_wrapper.tcl -notrace

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1700] Loaded user IP repository '/opt/Xilinx/Vivado\_HLS/2017.2/bin/unroll\_float\_8\_march'.

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/opt/Xilinx/Vivado/2017.2/data/ip'.

Command: synth\_design -top design\_1\_wrapper -part xcku035-ffva1156-3-e

Starting synth\_design

Attempting to get a license for feature 'Synthesis' and/or device 'xcku035-ffva1156'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xcku035-ffva1156'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 27527

---------------------------------------------------------------------------------

Starting RTL Elaboration : Time (s): cpu = 00:00:03 ; elapsed = 00:00:04 . Memory (MB): peak = 1164.535 ; gain = 16.996 ; free physical = 753 ; free virtual = 5104

---------------------------------------------------------------------------------

INFO: [Synth 8-638] synthesizing module 'design\_1\_wrapper' [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/hdl/design\_1\_wrapper.v:12]

INFO: [Synth 8-638] synthesizing module 'design\_1' [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/hdl/design\_1.v:13]

INFO: [Synth 8-638] synthesizing module 'design\_1\_simple\_0\_0' [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.runs/synth\_1/.Xil/Vivado-27518-drsatya-OptiPlex-990/realtime/design\_1\_simple\_0\_0\_stub.v:6]

INFO: [Synth 8-256] done synthesizing module 'design\_1\_simple\_0\_0' (1#1) [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.runs/synth\_1/.Xil/Vivado-27518-drsatya-OptiPlex-990/realtime/design\_1\_simple\_0\_0\_stub.v:6]

WARNING: [Synth 8-350] instance 'simple\_0' of module 'design\_1\_simple\_0\_0' requires 39 connections, but only 30 given [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/hdl/design\_1.v:136]

INFO: [Synth 8-256] done synthesizing module 'design\_1' (2#1) [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/hdl/design\_1.v:13]

INFO: [Synth 8-256] done synthesizing module 'design\_1\_wrapper' (3#1) [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.srcs/sources\_1/bd/design\_1/hdl/design\_1\_wrapper.v:12]

---------------------------------------------------------------------------------

Finished RTL Elaboration : Time (s): cpu = 00:00:04 ; elapsed = 00:00:04 . Memory (MB): peak = 1204.043 ; gain = 56.504 ; free physical = 761 ; free virtual = 5114

---------------------------------------------------------------------------------

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:04 ; elapsed = 00:00:04 . Memory (MB): peak = 1204.043 ; gain = 56.504 ; free physical = 761 ; free virtual = 5114

---------------------------------------------------------------------------------

INFO: [Device 21-403] Loading part xcku035-ffva1156-3-e

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.runs/synth\_1/.Xil/Vivado-27518-drsatya-OptiPlex-990/dcp3/design\_1\_simple\_0\_0\_in\_context.xdc] for cell 'design\_1\_i/simple\_0'

Finished Parsing XDC File [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.runs/synth\_1/.Xil/Vivado-27518-drsatya-OptiPlex-990/dcp3/design\_1\_simple\_0\_0\_in\_context.xdc] for cell 'design\_1\_i/simple\_0'

Parsing XDC File [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.runs/synth\_1/dont\_touch.xdc]

Finished Parsing XDC File [/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.runs/synth\_1/dont\_touch.xdc]

Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 1641.977 ; gain = 0.000 ; free physical = 174 ; free virtual = 4699

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Finished Constraint Validation : Time (s): cpu = 00:00:13 ; elapsed = 00:00:14 . Memory (MB): peak = 1641.980 ; gain = 494.441 ; free physical = 205 ; free virtual = 4731

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---------------------------------------------------------------------------------

Start Loading Part and Timing Information

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Loading part: xcku035-ffva1156-3-e

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Finished Loading Part and Timing Information : Time (s): cpu = 00:00:13 ; elapsed = 00:00:15 . Memory (MB): peak = 1641.980 ; gain = 494.441 ; free physical = 205 ; free virtual = 4731

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Start Applying 'set\_property' XDC Constraints

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Applied set\_property DONT\_TOUCH = true for design\_1\_i. (constraint file auto generated constraint, line ).

Applied set\_property DONT\_TOUCH = true for design\_1\_i/simple\_0. (constraint file auto generated constraint, line ).

---------------------------------------------------------------------------------

Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:13 ; elapsed = 00:00:15 . Memory (MB): peak = 1641.980 ; gain = 494.441 ; free physical = 207 ; free virtual = 4732

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Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:13 ; elapsed = 00:00:15 . Memory (MB): peak = 1641.980 ; gain = 494.441 ; free physical = 206 ; free virtual = 4732

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start RTL Component Statistics

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Detailed RTL Component Info :

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Finished RTL Component Statistics

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---------------------------------------------------------------------------------

Start RTL Hierarchical Component Statistics

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Hierarchical RTL Component report

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Finished RTL Hierarchical Component Statistics

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---------------------------------------------------------------------------------

Start Part Resource Summary

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Part Resources:

DSPs: 1700 (col length:120)

BRAMs: 1080 (col length: RAMB18 120 RAMB36 60)

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Finished Part Resource Summary

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Start Cross Boundary and Area Optimization

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Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:13 ; elapsed = 00:00:15 . Memory (MB): peak = 1641.980 ; gain = 494.441 ; free physical = 197 ; free virtual = 4723

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Applying XDC Timing Constraints

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Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:22 ; elapsed = 00:00:25 . Memory (MB): peak = 1915.621 ; gain = 768.082 ; free physical = 119 ; free virtual = 4394

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---------------------------------------------------------------------------------

Start Timing Optimization

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---------------------------------------------------------------------------------

Finished Timing Optimization : Time (s): cpu = 00:00:22 ; elapsed = 00:00:25 . Memory (MB): peak = 1915.621 ; gain = 768.082 ; free physical = 119 ; free virtual = 4394

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Technology Mapping

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Finished Technology Mapping : Time (s): cpu = 00:00:22 ; elapsed = 00:00:25 . Memory (MB): peak = 1926.641 ; gain = 779.102 ; free physical = 118 ; free virtual = 4393

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start IO Insertion

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Start Flattening Before IO Insertion

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Finished Flattening Before IO Insertion

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Start Final Netlist Cleanup

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---------------------------------------------------------------------------------

Finished Final Netlist Cleanup

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Finished IO Insertion : Time (s): cpu = 00:00:23 ; elapsed = 00:00:25 . Memory (MB): peak = 1926.641 ; gain = 779.102 ; free physical = 118 ; free virtual = 4393

---------------------------------------------------------------------------------

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Renaming Generated Instances

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Finished Renaming Generated Instances : Time (s): cpu = 00:00:23 ; elapsed = 00:00:25 . Memory (MB): peak = 1926.641 ; gain = 779.102 ; free physical = 118 ; free virtual = 4393

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Rebuilding User Hierarchy

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Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:23 ; elapsed = 00:00:25 . Memory (MB): peak = 1926.641 ; gain = 779.102 ; free physical = 118 ; free virtual = 4393

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---------------------------------------------------------------------------------

Start Renaming Generated Ports

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Finished Renaming Generated Ports : Time (s): cpu = 00:00:23 ; elapsed = 00:00:25 . Memory (MB): peak = 1926.641 ; gain = 779.102 ; free physical = 118 ; free virtual = 4393

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:23 ; elapsed = 00:00:25 . Memory (MB): peak = 1926.641 ; gain = 779.102 ; free physical = 118 ; free virtual = 4393

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---------------------------------------------------------------------------------

Start Renaming Generated Nets

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Finished Renaming Generated Nets : Time (s): cpu = 00:00:23 ; elapsed = 00:00:25 . Memory (MB): peak = 1926.641 ; gain = 779.102 ; free physical = 118 ; free virtual = 4393

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---------------------------------------------------------------------------------

Start Writing Synthesis Report

---------------------------------------------------------------------------------

Report BlackBoxes:

+------+--------------------+----------+

| |BlackBox name |Instances |

+------+--------------------+----------+

|1 |design\_1\_simple\_0\_0 | 1|

+------+--------------------+----------+

Report Cell Usage:

+------+--------------------+------+

| |Cell |Count |

+------+--------------------+------+

|1 |design\_1\_simple\_0\_0 | 1|

|2 |IBUF | 515|

|3 |OBUF | 259|

+------+--------------------+------+

Report Instance Areas:

+------+-------------+---------+------+

| |Instance |Module |Cells |

+------+-------------+---------+------+

|1 |top | | 1073|

|2 | design\_1\_i |design\_1 | 299|

+------+-------------+---------+------+

---------------------------------------------------------------------------------

Finished Writing Synthesis Report : Time (s): cpu = 00:00:23 ; elapsed = 00:00:25 . Memory (MB): peak = 1926.641 ; gain = 779.102 ; free physical = 118 ; free virtual = 4393

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Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:18 ; elapsed = 00:00:19 . Memory (MB): peak = 1926.641 ; gain = 341.164 ; free physical = 137 ; free virtual = 4413

Synthesis Optimization Complete : Time (s): cpu = 00:00:23 ; elapsed = 00:00:25 . Memory (MB): peak = 1926.648 ; gain = 779.102 ; free physical = 137 ; free virtual = 4413

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 515 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

A total of 515 instances were transformed.

IBUF => IBUF (IBUFCTRL, INBUF): 515 instances

19 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth\_design completed successfully

synth\_design: Time (s): cpu = 00:00:24 ; elapsed = 00:00:28 . Memory (MB): peak = 1952.281 ; gain = 817.324 ; free physical = 168 ; free virtual = 4381

INFO: [Common 17-1381] The checkpoint '/opt/Xilinx/Vivado/2017.2/bin/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1/UNROLL\_FLOAT\_9\_MARCH\_NEW\_1\_2\_1.runs/synth\_1/design\_1\_wrapper.dcp' has been generated.

report\_utilization: Time (s): cpu = 00:00:00.11 ; elapsed = 00:00:00.50 . Memory (MB): peak = 1952.285 ; gain = 0.000 ; free physical = 165 ; free virtual = 4382

INFO: [Common 17-206] Exiting Vivado at Fri Mar 9 16:30:03 2018...