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File generated by Vivado(TM) HLS - High-Level Synthesis from C, C++ and SystemC

Version: 2017.2

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INFO: [SYN 201-201] Setting up clock 'default' with a period of 10ns.

WARNING: [HLS 200-40] Cannot find library '/opt/Xilinx/Vivado\_HLS/2017.2/common/technology/xilinx/null/null.lib'.

WARNING: [HLS 200-40] Cannot find library 'xilinx/null/null'.

INFO: [HLS 200-10] Setting target device to 'xcku035-ffva1156-3-e'

INFO: [HLS 200-10] Analyzing design file '../../../../../home/drsatya/neha/add.c' ...

INFO: [HLS 200-10] Validating synthesis directives ...

INFO: [HLS 200-111] Finished Checking Pragmas Time (s): cpu = 00:00:03 ; elapsed = 00:00:10 . Memory (MB): peak = 352.020 ; gain = 12.590 ; free physical = 176 ; free virtual = 3434

INFO: [HLS 200-111] Finished Linking Time (s): cpu = 00:00:03 ; elapsed = 00:00:11 . Memory (MB): peak = 352.020 ; gain = 12.590 ; free physical = 174 ; free virtual = 3434

INFO: [HLS 200-10] Starting code transformations ...

INFO: [HLS 200-111] Finished Standard Transforms Time (s): cpu = 00:00:03 ; elapsed = 00:00:11 . Memory (MB): peak = 352.020 ; gain = 12.590 ; free physical = 168 ; free virtual = 3434

INFO: [HLS 200-10] Checking synthesizability ...

INFO: [HLS 200-111] Finished Checking Synthesizability Time (s): cpu = 00:00:03 ; elapsed = 00:00:11 . Memory (MB): peak = 352.020 ; gain = 12.590 ; free physical = 168 ; free virtual = 3434

INFO: [XFORM 203-501] Unrolling loop 'Loop-1' (../../../../../home/drsatya/neha/add.c:10) in function 'simple' completely.

INFO: [XFORM 203-101] Partitioning array 'a' (../../../../../home/drsatya/neha/add.c:3) in dimension 1 completely.

INFO: [XFORM 203-101] Partitioning array 'b' (../../../../../home/drsatya/neha/add.c:3) in dimension 1 completely.

INFO: [XFORM 203-101] Partitioning array 'c' (../../../../../home/drsatya/neha/add.c:3) in dimension 1 completely.

INFO: [HLS 200-111] Finished Pre-synthesis Time (s): cpu = 00:00:03 ; elapsed = 00:00:11 . Memory (MB): peak = 480.016 ; gain = 140.586 ; free physical = 150 ; free virtual = 3417

INFO: [HLS 200-111] Finished Architecture Synthesis Time (s): cpu = 00:00:03 ; elapsed = 00:00:11 . Memory (MB): peak = 480.016 ; gain = 140.586 ; free physical = 158 ; free virtual = 3425

INFO: [HLS 200-10] Starting hardware synthesis ...

INFO: [HLS 200-10] Synthesizing 'simple' ...

INFO: [HLS 200-10] ----------------------------------------------------------------

INFO: [HLS 200-10] -- Implementing module 'simple'

INFO: [HLS 200-10] ----------------------------------------------------------------

INFO: [SCHED 204-11] Starting scheduling ...

INFO: [SCHED 204-11] Finished scheduling.

INFO: [HLS 200-111] Elapsed time: 11.44 seconds; current allocated memory: 0.318 MB.

INFO: [BIND 205-100] Starting micro-architecture generation ...

INFO: [BIND 205-101] Performing variable lifetime analysis.

INFO: [BIND 205-101] Exploring resource sharing.

INFO: [BIND 205-101] Binding ...

INFO: [BIND 205-100] Finished micro-architecture generation.

INFO: [HLS 200-111] Elapsed time: 0.06 seconds; current allocated memory: 0.318 MB.

INFO: [HLS 200-10] ----------------------------------------------------------------

INFO: [HLS 200-10] -- Generating RTL for module 'simple'

INFO: [HLS 200-10] ----------------------------------------------------------------

INFO: [RTGEN 206-500] Setting interface mode on port 'simple/a\_0' to 'ap\_none'.

INFO: [RTGEN 206-500] Setting interface mode on port 'simple/a\_1' to 'ap\_none'.

INFO: [RTGEN 206-500] Setting interface mode on port 'simple/a\_2' to 'ap\_none'.

INFO: [RTGEN 206-500] Setting interface mode on port 'simple/a\_3' to 'ap\_none'.

INFO: [RTGEN 206-500] Setting interface mode on port 'simple/a\_4' to 'ap\_none'.

INFO: [RTGEN 206-500] Setting interface mode on port 'simple/a\_5' to 'ap\_none'.

INFO: [RTGEN 206-500] Setting interface mode on port 'simple/a\_6' to 'ap\_none'.

INFO: [RTGEN 206-500] Setting interface mode on port 'simple/a\_7' to 'ap\_none'.

INFO: [RTGEN 206-500] Setting interface mode on port 'simple/b\_0' to 'ap\_none'.

INFO: [RTGEN 206-500] Setting interface mode on port 'simple/b\_1' to 'ap\_none'.

INFO: [RTGEN 206-500] Setting interface mode on port 'simple/b\_2' to 'ap\_none'.

INFO: [RTGEN 206-500] Setting interface mode on port 'simple/b\_3' to 'ap\_none'.

INFO: [RTGEN 206-500] Setting interface mode on port 'simple/b\_4' to 'ap\_none'.

INFO: [RTGEN 206-500] Setting interface mode on port 'simple/b\_5' to 'ap\_none'.

INFO: [RTGEN 206-500] Setting interface mode on port 'simple/b\_6' to 'ap\_none'.

INFO: [RTGEN 206-500] Setting interface mode on port 'simple/b\_7' to 'ap\_none'.

INFO: [RTGEN 206-500] Setting interface mode on port 'simple/c\_0' to 'ap\_vld'.

INFO: [RTGEN 206-500] Setting interface mode on port 'simple/c\_1' to 'ap\_vld'.

INFO: [RTGEN 206-500] Setting interface mode on port 'simple/c\_2' to 'ap\_vld'.

INFO: [RTGEN 206-500] Setting interface mode on port 'simple/c\_3' to 'ap\_vld'.

INFO: [RTGEN 206-500] Setting interface mode on port 'simple/c\_4' to 'ap\_vld'.

INFO: [RTGEN 206-500] Setting interface mode on port 'simple/c\_5' to 'ap\_vld'.

INFO: [RTGEN 206-500] Setting interface mode on port 'simple/c\_6' to 'ap\_vld'.

INFO: [RTGEN 206-500] Setting interface mode on port 'simple/c\_7' to 'ap\_vld'.

INFO: [RTGEN 206-500] Setting interface mode on function 'simple' to 'ap\_ctrl\_hs'.

INFO: [SYN 201-210] Renamed object name 'simple\_fadd\_32ns\_32ns\_32\_4\_full\_dsp' to 'simple\_fadd\_32ns\_bkb' due to the length limit 20

INFO: [RTGEN 206-100] Generating core module 'simple\_fadd\_32ns\_bkb': 8 instance(s).

INFO: [RTGEN 206-100] Finished creating RTL model for 'simple'.

INFO: [HLS 200-111] Elapsed time: 0.06 seconds; current allocated memory: 0.318 MB.

INFO: [HLS 200-111] Finished generating all RTL models Time (s): cpu = 00:00:04 ; elapsed = 00:00:12 . Memory (MB): peak = 480.016 ; gain = 140.586 ; free physical = 146 ; free virtual = 3421

INFO: [SYSC 207-301] Generating SystemC RTL for simple.

INFO: [VHDL 208-304] Generating VHDL RTL for simple.

INFO: [VLOG 209-307] Generating Verilog RTL for simple.

INFO: [HLS 200-112] Total elapsed time: 12.04 seconds; peak allocated memory: 0.318 MB.