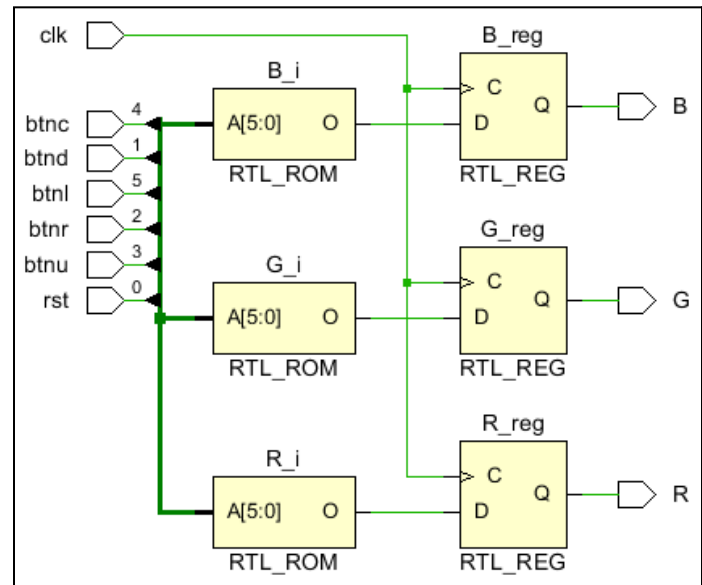


Assign Tri-color RGB LEDs control on the Nexys A7 Board

Verilog Module:

```
module rgb_led(
input clk, rst, btnl, btnc, btneu, btnr, btnd,
output reg R, G, B);
always@(posedge clk) begin
    case ({btnl, btnc, btneu, btnr, btnd, rst})
        6'b000000: begin R<=0; B<=0; G<=0; end
        6'b000001: begin R<=1; B<=0; G<=0; end
        6'b000010: begin R<=0; B<=0; G<=1; end
        6'b000100: begin R<=0; B<=1; G<=0; end
        6'b001000: begin R<=1; B<=0; G<=1; end
        6'b100000: begin R<=1; B<=1; G<=0; end
        6'b010000: begin R<=0; B<=1; G<=1; end
        default: begin R<=1; B<=1; G<=1; end
    endcase
end
endmodule
```



Constraint File

```
## Clock signal
set_property -dict { PACKAGE_PIN E3      IOSTANDARD LVCMOS33 } [get_ports { clk }]; #IO_L12P_T1_MRCC_35
Sch=clk100mhz
create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports {clk}];

## RGB LEDs
set_property -dict { PACKAGE_PIN R12      IOSTANDARD LVCMOS33 } [get_ports { B }]; #IO_L5P_T0_D06_14
Sch=led16_b
set_property -dict { PACKAGE_PIN M16      IOSTANDARD LVCMOS33 } [get_ports { G }]; #IO_L10P_T1_D14_14
Sch=led16_g
set_property -dict { PACKAGE_PIN N15      IOSTANDARD LVCMOS33 } [get_ports { R }]; #IO_L11P_T1_SRCC_14
Sch=led16_r
##CPU Reset Button
set_property -dict { PACKAGE_PIN C12      IOSTANDARD LVCMOS33 } [get_ports { rst }];
#IO_L3P_T0_DQS_AD1P_15 Sch=cpu_resethn

##Buttons
set_property -dict { PACKAGE_PIN N17      IOSTANDARD LVCMOS33 } [get_ports { btnc }]; #IO_L9P_T1_DQS_14
Sch=btnc
set_property -dict { PACKAGE_PIN M18      IOSTANDARD LVCMOS33 } [get_ports { btneu }]; #IO_L4N_T0_D05_14
Sch=btneu
set_property -dict { PACKAGE_PIN P17      IOSTANDARD LVCMOS33 } [get_ports { btnl }]; #IO_L12P_T1_MRCC_14
Sch=btnl
set_property -dict { PACKAGE_PIN M17      IOSTANDARD LVCMOS33 } [get_ports { btnr }]; #IO_L10N_T1_D15_14
Sch=btnr
set_property -dict { PACKAGE_PIN P18      IOSTANDARD LVCMOS33 } [get_ports { btnd }];
#IO_L9N_T1_DQS_D13_14 Sch=btnd
```