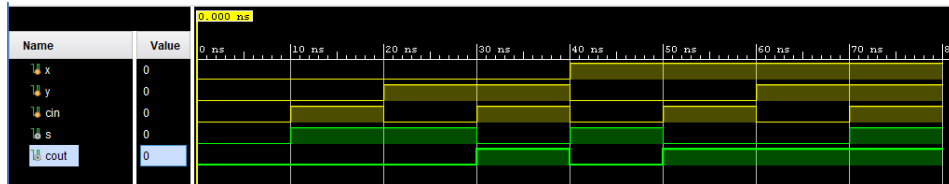
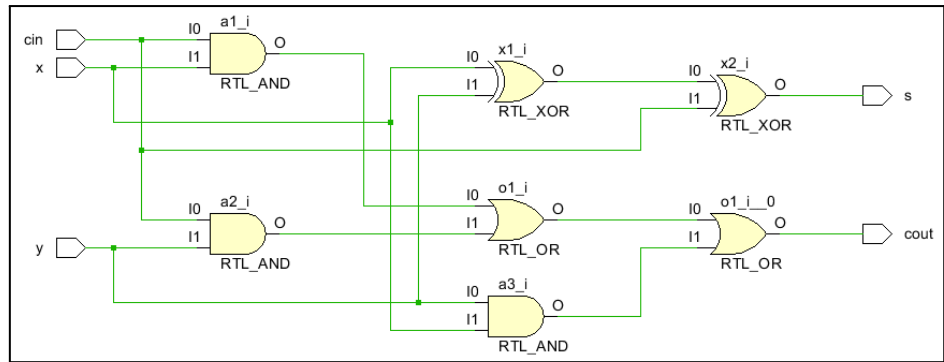


## DSD LAB SESSION 2

### Design & Simulate a Full Adder Circuit using Structural Modeling

#### Full Adder



Summary				
Resource	Utilization	Available	Utilization %	
LUT		1	63400	0.00
IO		5	210	2.38

LUT	1%				
IO	2%				

Utilization (%)

#### Full Subtractor

