Assignment 1

EE20MTECH14014
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Download the LaTex code from:

https://github.com/neharani289/FPGA−Lab/tree/main/Assignment1

1 Question

[ICSE 2017 Q5 (b)]
State the application of Half Adder. Draw the truth table and circuit diagram for a Half Adder

2 Solution

2.1 Application of Half Adder

1) Half Adder is a combinational logic circuit. It is used for the purpose of adding two single bit numbers.

2) Half adder is used to make full adder as a full adder requires 3 inputs, the third input being an input carry i.e. we will be able to cascade the carry bit from one adder to the other.

3) The ALU (arithmetic logic circuitry) of a computer uses half adder to compute the binary addition operation on two bits.

2.2 Truth Table of Half Adder

The truth table corresponding to sum and carry for various choices of input A, B is shown below:

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

2.3 Circuit Diagram

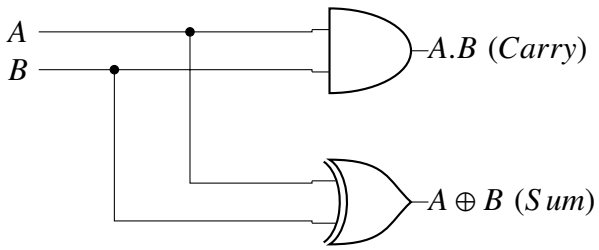

Fig. 1: Circuit Diagram of Half Adder

2.4 Implementation of Half Adder using NAND Gate

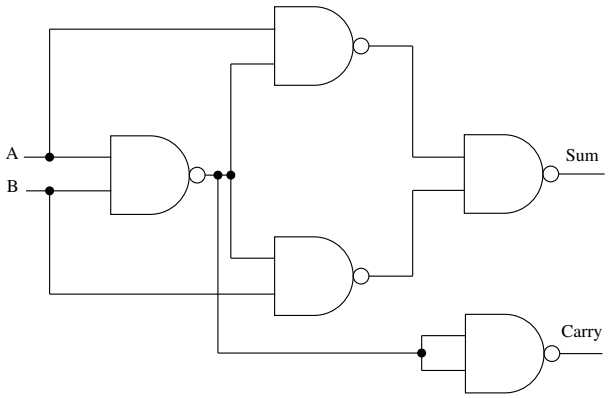

Fig. 2: Circuit Diagram of Half Adder using NAND Gate