NEHA RAVISHANKAR RAO

FPGA & Embedded Systems Engineer

nravish3@charlotte.edu ⋄ Charlotte, NC

linkedin.com/in/neharao ⋄ github.com/neharrao ⋄ neharrao.github.io

SUMMARY

Embedded systems engineer with expertise in FPGA development, digital design, and hardware acceleration. Skilled in VHDL, Python, and C++ with hands-on experience in FPGA architectures, including Pynq Z2, Basys 3, and Xilinx Vivado. Strong background in real-time data processing, communication protocols (UART, I2C, SPI), and embedded hardware design. Experienced in optimizing performance for hardware-based computing and developing scalable FPGA-based solutions.

TECHNICAL SKILLS

Programming Languages:	C, C++, Python, VHDL
FPGA and Embedded Dev.:	Pynq Z2, Basys 3, VCU128, Vivado, Vitis, Jupyter Notebook, MSP430, Raspberry Pi, Arduino, SparkFun RedBot
OS and Kernel Development:	Linux Kernel Debugging, Embedded OS, Secure Boot
Security & Networking:	CISCO ASA, Checkpoint, Wireshark, Splunk, InfoBlox, Tufin, DX NetOps, Spectrum
Testing & Automation:	Selenium, Cucumber, Jenkins, SoapUI
Mathematical Modeling:	MATLAB, Simulink

EDUCATION

Master of Science in Computer Engineering, University of North Carolina, Charlotte   August 2023 - May 2025
Relevant coursework: Computer Architecture, Embedded Operating Systems, Introduction to VHDL, Reconfig Computing, Data Communication and Networking, Model and Analysis for Communication Networks, Advanced Embedded Systems, Research Tools & Techniques   GPA: 3.5/4

Bachelor of Technology in Electronics and Communication Engineering, MITS, India   August 2017 - May 2021
Relevant coursework: Microprocessor & Microcontrollers, Embedded Systems, Computer Organization, Secure Communication, Digital Signal Processing.

EXPERIENCE

Teaching Assistant, UNCC, Charlotte, NC   January 2024 – May 2025

- **Logic System Design** (Jan 2025 – May 2025) - Led recitation sessions to reinforce key concepts, assigned and graded homework.

- **Computer Utilization in C++** (Aug 2024 – Dec 2024) - Conducted lab sessions, taught C++ fundamentals, guided students on coding, assigned projects, and graded exams.

- **Intro to Engineering Practice & Principles II** (Jul 2024 – Aug 2024) - Graded quizzes and provided detailed feedback.

- **Computer Engr Programming II** (Jul 2024 – Aug 2024) - Graded programming projects for accuracy and efficiency.

- **Logic & Networks Lab** (Jan 2024 – May 2024) - Conducted lab sessions, taught theoretical concepts, supervised experiments, and graded lab reports, notebooks, and practical exams.

Technical Consultant (Security Analyst), IBM, India   January 2022 – May 2023

- Managed firewall configurations, executing more than 200 change requests for CISCO ASA and Checkpoint firewalls, ensuring 99.9% uptime.
- Streamlined monitoring workflows, reducing troubleshooting time by 30%.
- Maintained firewall health using Spectrum, proactively identifying and resolving faults.
- Addressed network security incidents, resolving client issues efficiently.

Test Specialist Trainee, IBM, India   October 2021 – January 2022

- Demonstrated expertise in planning, designing, managing, executing, and reporting tests using testing tools and techniques.
- Produced key deliverables such as testing strategies, comprehensive test plans, test cases, test reports, and quality metrics.
- Created and executed test scenarios, focusing on software usability to ensure a seamless user experience.

Intern, Bharat Sanchar Nigam Limited, India   June 2018

- Gained valuable insights into telecommunication architecture, understanding the intricacies of network structures.
- Acquired knowledge of GSM technology, delving into the principles and protocols of mobile communication.
- Explored standard telephone exchange techniques, developing a foundational understanding of voice communication systems.

PROJECTS

- **Master's Thesis: Achieving Real-Time Dataflow and Parallelism in FPGA Systems Using Asynchronous Constructs in Python** - My research focuses on optimizing data movement in parallel computing environments by leveraging named memory segments and a hardware/software co-designed memory management system. This approach enables efficient data transfer scheduling, reducing memory bottlenecks in FPGA-based architectures equipped with High Bandwidth Memory (HBM). By incorporating hash-based memory addressing and asynchronous task execution, the framework enhances real-time data matching and parallelism in large-scale computations. The work has applications in network-on-chip (NoC) interconnects, AI accelerators, and high-performance FPGA computing.

- **Tic-Tac-Toe Gamepad** - Designed and implemented a two-player Tic-Tac-Toe game using MSP430G2553 microcontrollers, I2C OLED displays, and UART communication for real-time synchronization. Each player used a custom-built perfboard controller featuring tactile buttons for navigation and selection, an LED turn indicator, and a buzzer for move confirmation. Implemented a 3-foot wired communication interface to ensure stable data exchange between controllers. Optimized I2C communication for efficient LCD updates and utilized UART for board-to-board synchronization, ensuring seamless gameplay.

- **VHDL Microprocessor Design and Simulation** - Developed an 8-bit microprocessor in VHDL, implementing basic instructions like LDA, STA, ADD, JMP, and JNC. Expanded functionality with additional arithmetic operations, a pseudo-random number generator (PRNG) and jump to a subroutine (JSR).

- **Dual-Core Processor System on PYNQ Z2** - Developed a dual-core system on the PYNQ Z1/Z2, integrating ARM Cortex A9 and Xilinx MicroBlaze processors. Utilized shared AXI BRAM, custom VHDL synchronizer, and dual UARTs for inter-processor communication. Implemented C/C++ programs for data exchange and processing, showcasing embedded systems and FPGA development skills.

- **A Priority Based Pre-threaded Image Processing Server** - Developed a high-performance image processing server with a multi-threaded structure, achieving a 20% speed improvement and a 25% reduction in response time through superior thread prioritization. Implemented real-time scheduling for tasks completing in less than 5 milliseconds, handling 100+ simultaneous client requests without performance degradation. Integrated OpenCV, resulting in a 15% reduction in processing time for color-to-grayscale conversion. Demonstrated efficiency through live demos, showcasing the server's scalability and responsiveness under varying workloads.

- **Instruction Decoder and Pipelining Model of RISC-V Architecture C++** - Built a processor decoder in C++ that can decode RISC-V ISA instructions using the Von Neumann architecture. Each decoded instruction in the modeled and pipelined RISC-V processor updates registers as it passes through four pipeline stages. Data predictions for dangers and branching are verified by the module.

- **IoT Based Water Quality Monitoring System in Sea Cage Aquaculture** - Deployed an IoT-based water quality monitoring system for sea cage aquaculture achieving a 98% accuracy in real-time measurements for pH, dissolved oxygen, and temperature. The system operates with a monitoring frequency of every 15 minutes, responding to critical deviations within 2 minutes, ensuring optimal conditions. With a system uptime of 99.5%, it provides continuous monitoring, and advanced analytics algorithms improved data analysis efficiency by 20%, aiding in decision-making for aquatic organism health.

ACCOMPLISHMENTS

- Completed 5 years training in Indian Navy as Leading Sea Cadet and acquired rifle shooting, sailing, swimming and parade skills.

- Participated in India Innovation Challenge Design contest 2019 organized by AICTE and Texas Instruments.

- Participated in RoboRave India 2017 tournament organized by RoboRave International.

- Participated in Leadership Training Workshop in 2015 and 2013 as part of school senate.

LEADERSHIP

- Treasurer, IEEE Women in Engineering Student Chapter   Aug 2024 – Present